Silicon Turnkey eXpress

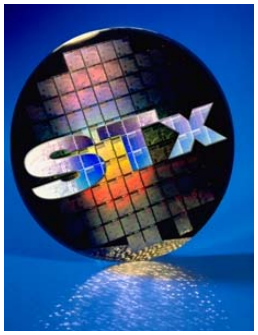
Original Design Manufacturer

Apollo5121

Wind River Tools

Freescale's ADS512101

User's Manual



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Revision History

Rev	Date	Comments
1.0	Mar 24, 2008	Release of user manual based on ADS512101UM rev 1.5 dated Jan 31, 2009

Welcome and Support:

In addition to the Freescale MPC5121e CPU and STx Apollo5121 development board, the kit includes a 30-day evaluation version of both the market leading VxWorks and Wind River Linux device software solutions. On the enclosed DVDs you will find Wind River Workbench, our Eclipse-based toolset and evaluation versions for Wind River Linux and VxWorks runtime, including board support packages specifically optimized for Freescale's MPC5121e chip.

During the evaluation period or anytime after, you may purchase a full system license. All you need to do is call 800-545-9463 (or +1 510-748-4100 for international customers), and we'll take care of the rest.

Your Apollo5121 kit comes with full support from STx, with the backing of Wind River's worldwide customer support operations staff, during the software evaluation period. If you have support questions during your software evaluation period, please send an email to Apollo5121@silicontkx.com or call +1 440-461-4700 ext. 182.

Additional support information may be found at www.silicontkx.com/support/index.php

Product Terminology:

Apollo5121 uses Freescale's Advanced Development System module, ADS512101 and Wind River Systems tools including a (preinstalled) Linux BSP for the ADS512101. All hardware or information about the module in this manual is based on the ADS512101 user's manual. All information regarding the module references the ADS512101. All information regarding Wind River System tools references the Apollo5121. Expect for the software tools provided or preinstalled the Apollo5121 and ADS512101 terminology is interchangeable.

Warranty:

To assure all future engineering notifications are communicated the enclosed warranty information must be completed.

NOTICE

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The following information is intended to alert the user to possible dangers and important information contained within this guide. The "**WARNINGS**", "**CAUTIONS**" and "**NOTES**" do not eliminate these dangers. Close attention to the information supplied along with "common sense" operation is the major accident prevention measure.

WARNING:	Failure to follow this warning may result in bodily injury.

CAUTION:	Failure to follow this caution may result in possible damage to the board.

NOTE:	Failure to follow this note may result in improper results from the board.

Reference Websites

Below is a list of websites that can be used to obtain additional information and details that may not be fully provided in this manual.

Abatron BDI2000 JTAG Emulator ..... www.ultsol.com/mfgs_emul_abtr.htm
Altera Quartus II…… ...www.altera.com
Wind River Probe ..... www.windriver.com

5 Volt Only Operation

CAUTION:	Failure to follow this caution may result in possible damage to the board.

The ADS512101 can operate from either 5 VDC only power supplies, such as the 15 watt wall mounted power supply included in this kit, or an ATX standard power supply. When the ADS512101 is operated with the 15W wall mounted power supply included with this kit normal operation will be LIMITED.

The 15 watt, 5 volts operation will NOT provide 12 volts required for peripherals or PCI. However all other ADS512101 function will be normal for worse case maximum power usage.

ATX power supplies supports all power for all peripherals and PCI. Follow the instructions in this manual for either 5 volts or ATX operation (see Section 3.2.6).

Media Access Control Address

Every ADS512101 has a unique MAC address saved in memory as part of the standard environment. A label on the backside of the PCB (under the STx logo) provides the PCB revision number, the serial number, and the MAC address. This same information will appear on a label on the CD container.

If the MAC address needs to be reloaded, use these steps:

1. ***Boot from main FLASH***
2. ***Type 'setenv ethaddr ' MAC Address as '00:1E:59:nn:nn:nn'***
3. ***If an incorrect MAC address is entered, U-Boot must be reloaded and a new MAC address can be entered.***

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List of Included Accessories

- User Manual (on CD)
- Schematic (on CD)
- 5V, 15W Wall Mount Power Supply
- Null Modem Cable
- USB Adaptor Mini B Male to A Female
- Wind River Evaluation Tools:
  - Wind River Workbench
  - Eclipse-based toolset
  - Wind River Linux
  - VxWorks runtime
- Wind River BSP specifically optimized for Freescale's MPC5121e

List of Optional Accessories

These accessories are available from Silicon Turnkey Express. See the enclosed order form or visit web site:

Accessories

- Cases with custom silkscreen
- Backplates/Custom silkscreen
- LCDs, Inverter, Touchscreen
- Monitors, Touchscreen
- USB 802.11 Radio
- MiniPCI WiMAX Radio
- DRAM Modules
- Memory Upgrades
- Hard Drive (IDE)
- Solid State Hard Drive (FLASH)
- CD-ROM or DVD Drive
- Wall Cube Power Supplies
- Internal Power Supplies
- PCI Riser Cards
- Peripherals inside the case
- Cables (All kinds & Customs)

Add-On Features

- Bluetooth ® Radio
- Camera/Image Capture
- Microphone
- GPS module
- WiFi module
- Profibus/Fieldbus

Software

- Operating Systems
- Graphic Solutions
- Cellular Connectivity
- GPS Location
- Touchscreen
- Bluetooth ® Technology
- Voice Recognition
- Wireless
- Database Client

1.0 General Description

The ADS512101 Advanced Development System is a mini-ITX form-factor reference and mother board based on Freescale's MPC5121e microprocessor. The board will provide on-board DDR SDRAM, NOR FLASH, NAND FLASH, (2) 4 wire RS232 ports, 2 CAN ports, USB 2.0, 10/100 Ethernet, Audio in/out/mic, SATA and PATA drive support, PCI, Micro-SD, 24bpp graphics, all powered from a standard ATX or 5 Volt wall mount power supply.

The board can be integrated into any configuration required by the addition of optional peripherals. These would include items such as enclosures, displays, HDD and numerous other mini-ITX accessories.

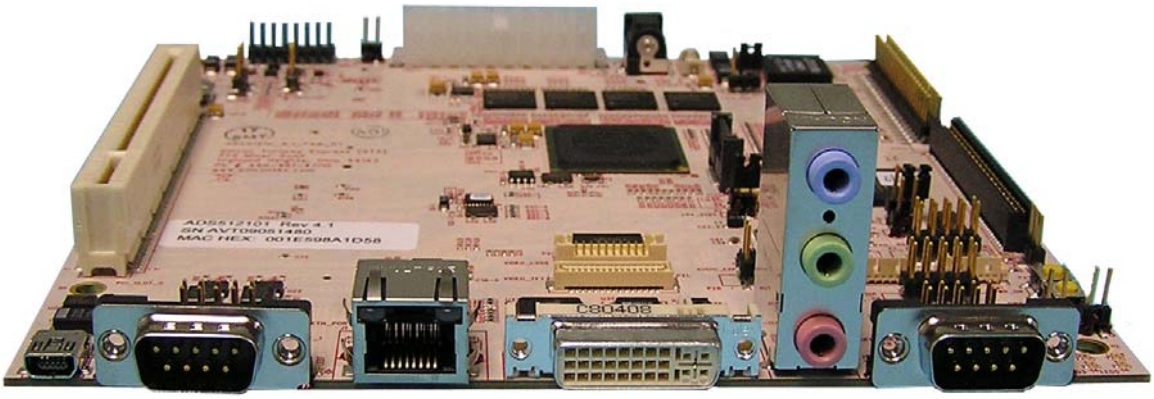


Figure 1 – ADS512101

Silicon Turnkey Express will work with your embedded systems engineers to integrate a final product that will give your end users the best performing and most cost effective embedded solution.

1.1 Device Placement and Functions

This section provides a description of the connectors, jumpers, switches and main components of the ADS512101 board. Refer to Figures 2 and 3 for location of the devices referenced below.

Additional descriptions of the functionality of switches and jumpers along with their recommended settings will be found in Section 3 of this manual.

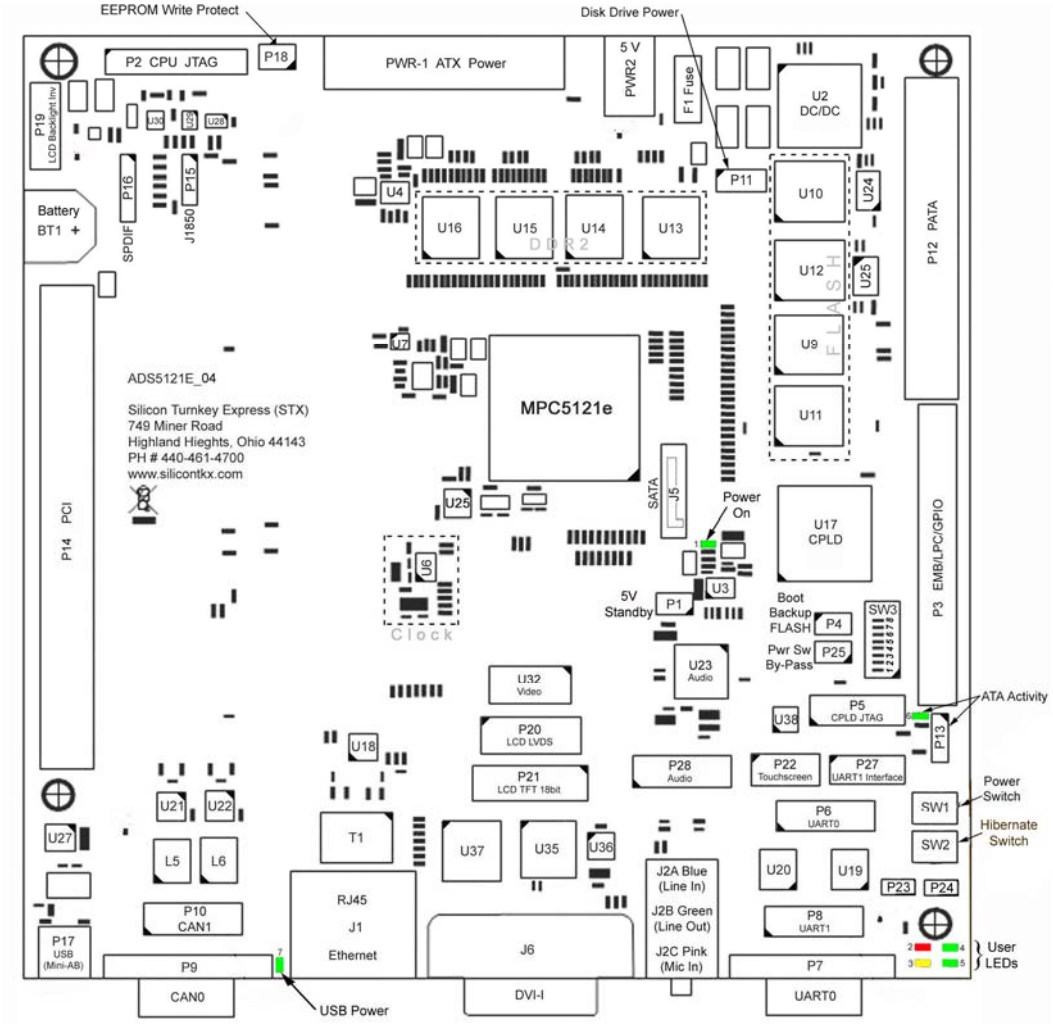


Figure 2 – ADS512101 Top Board Layout

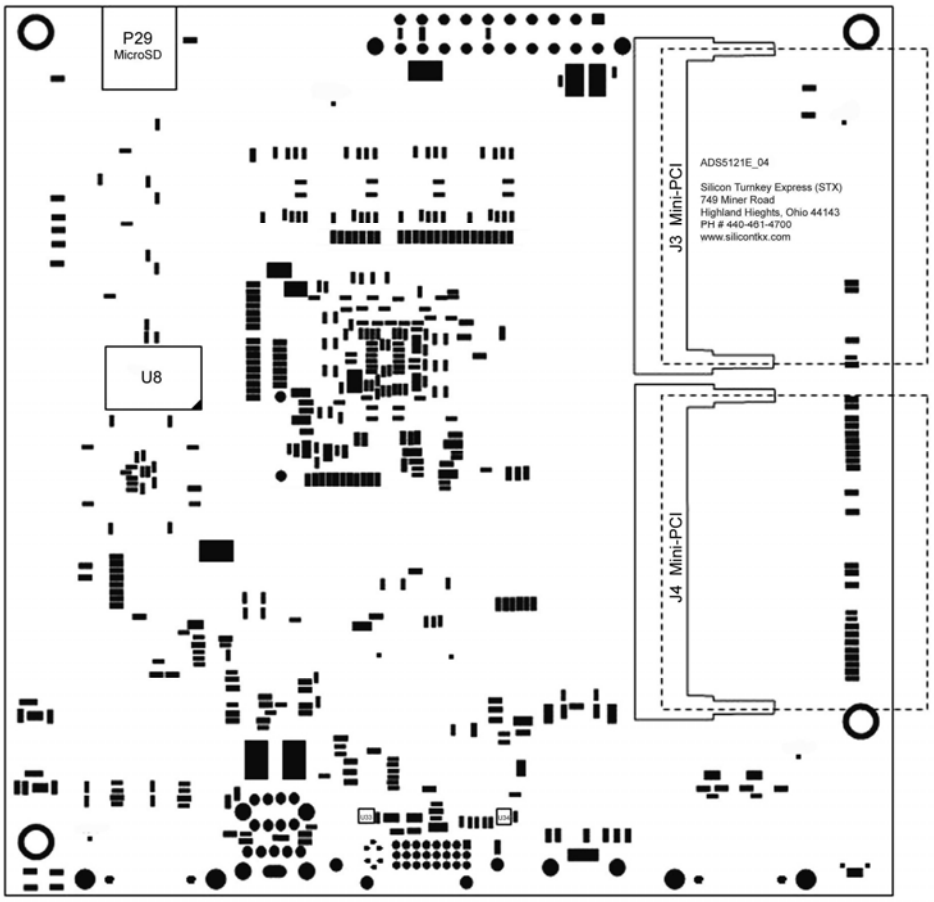


Figure 3 – ADS512101 Bottom Board Layout

1.1.01 BT1 – Battery

Use a 3 Volt Lithium button battery. PCB Rev 1.x and 2.x used type CR2032 or equivalent. PCB Rev 3.x or higher uses CR1220 or equivalent.

1.1.02 J01 – RJ45, 10/100 BaseT

J1 is a standard Ethernet input jack.

1.1.03 J02 – Audio Connectors

J2 has three stereo connection, J2A (Blue) is Line In; J2B (Green) is Line Out; J2C (Pink) is Aux In.

1.1.04 J03 – Mini-PCI Connector

(See Figure 3)

J3 is a Mini-PCI 32 bit connector with +3.3v that uses ID_SEL_AD22.

1.1.05 J04 – Mini-PCI Connector

(See Figure 3)

J4 is a Mini-PCI 32 bit connector with +3.3v that uses ID_SEL_AD23.

1.1.06 J05 – SATA Interface

J5 is the serial ATA interface connector.

1.1.07 J06 – DVI-I

J6 is the Digital Video Interface.

1.1.08 LED 1 – 5V Good

Indicates when 5 Volts is on.

1.1.09 LED 2 to 5 – CPLD

Is user definable by the CPLD.

1.1.10 LED 6 – ATA Activity

Indicates when ATA data fetches occur.

1.1.11 LED 7 – USB Power

Indicates when USB power is on.

1.1.12 P01 – 5V Only Operation

See Jumpers Section 3.2.6.

1.1.13 P02 – JTAG Connector

Connector P02 is a 16-pin header used for the COP/JTAG input. This port is made available to aid in the programming of the ADS512101.
The pin-outs for the connector are listed in Appendix A

A JTAG interface device, such as the Abatron's BDI2000 or Freescale's CW USB TAP or equivalent, should be used.

1.1.14 P03 – Expansion Bus

P03 provides signals for EMB, PLC, and GPIO. See Appendix C for pin out.

1.1.15 P04 – Back Up FLASH

Normally Open

A jumper is used to re-FLASH U-Boot to main FLASH. See Section 7.3, Re-Installing U-Boot Instructions.

1.1.16 P05 – CPLD

Header P05 is a CPLD JTAG port for programming and application debugging of the CPLD.

An Altera Quartus II with a Byteblaster cable or equivalent programming kit should be used.

1.1.18 P07 – RS232, UART 0

P7 is a 9-pin "D" style connector for serial communications.

1.1.19 P08 – RS232

P8 is a header connector for an additional RS232 connector. See Appendix B for pin out.

1.1.20 P09 – CAN 0

P9 is a 9-pin "D" style connector for Control Area Network.

1.1.21 P10 – CAN 1

P10 is a header connector for an additional CAN connector. See Appendix B for pin out.

1.1.22 P11 – ATA Drive Select

See Jumper Section 3.2.3.

1.1.23 P12 – PATA Connector

P12 is a 40 pin connector for attaching an optional parallel device.

1.1.24 P13 – Front Panel ATA LED

P13 is a 2-pin header used to enable the front panel LED.

1.1.25 P14 – PCI Connector

P14 is the standard PCI connector that uses ID_SEL_AD21.

1.1.26 P15 – J1850 Interface

P15 is a serial connection for J1850.

1.1.27 P16 – SPDIF Interface

P16 is a connection (header) for the SPDIF to the MPC5121e.

1.1.28 P17 – Mini USB

P17 is a USB mini AB connector that is compatible with the USB 2.0 format.

1.1.29 P18 – EEPROM WP

See Jumper Seciton 3.2.2.

1.1.30 P19 – LCD Backlight Inverter Power

This provides power and control signals to an LCD Inverter.

1.1.31 P20 – LCD Connector

This is a 20 pin LVD connector.

1.1.32 P21 – LCD Connector

This connector is for a TFT, 18bit LCD to accommodate Media5200 monitors.

1.1.34 P22 – Touch Screen Interface

This is an enhancement that may is not available on the standards ADS512101.

1.1.34 P23 – Front Panel Hardware Switch

P23 is a header to provide a connection for the Front Panel Hardware Reset switch SW 1.

Push once (momentary) causes a Power on Reset.

Push and hold for 5 seconds causes a power down.

1.1.35 P24 – Front Panel Hibernation Switch

P24 is a header to provide a connection for the Front Panel Hibernation mode switch SW2.

1.1.36 P25 – Power Switch By-Pass

This jumper is used to by pass the power switch to allow for remote access by applying power to the ADS512101.

1.1.37 P27 – RS232, UART 1

This is a 10 pin header to accommodate an external serial port.

1.1.38 P28 – Audio

This is a 10 pin header to accommodate external audio connections.

1.1.39 P29 – Micro-SD Socket

(See Figure 3)

P29 allows use of any Micro-SD memory.

1.1.40 PWR-1 – ATX Power Connector

PWR-1 is the main ATX power input connector for the ADS512101. It is designed to use a standard 20-pin ATX power supply.

1.1.41 PWR-2 – DC Power Input

PWR-2 is the 5VDC to the board. P01 needs to be installed to enable the on board power signal. See Section 3.2.1.

1.1.42 SW1 – Power Switch

See Switch Settings, Section 3.1.1

1.1.43 SW2 – Hibernate Switch

See Switch Settings, Section 3.1.2

1.1.44 SW3 – Mode Switch

See Switch Settings, Section 3.1.3

2.0 Hardware Design & Architecture

2.1 General Description

Some of the features of the ADS512101 are:

- Freescale Processor MPC5121e
- DDR2 RAM module- capacity 256Mbyte to 2 Gbytes
- JTAG and control CPLD
- LVDS 24-bit (LCD) or CMOS (Rev3)
- RS-232 and CAN port
- USB A, B and OTG
- NOR, NAND and backup FLASH
- Local bus IO connector
- Stereo Audio (AC97)
- PATA (IDE) or Micro-SD
- PCI/mini-PCI (radio slots)

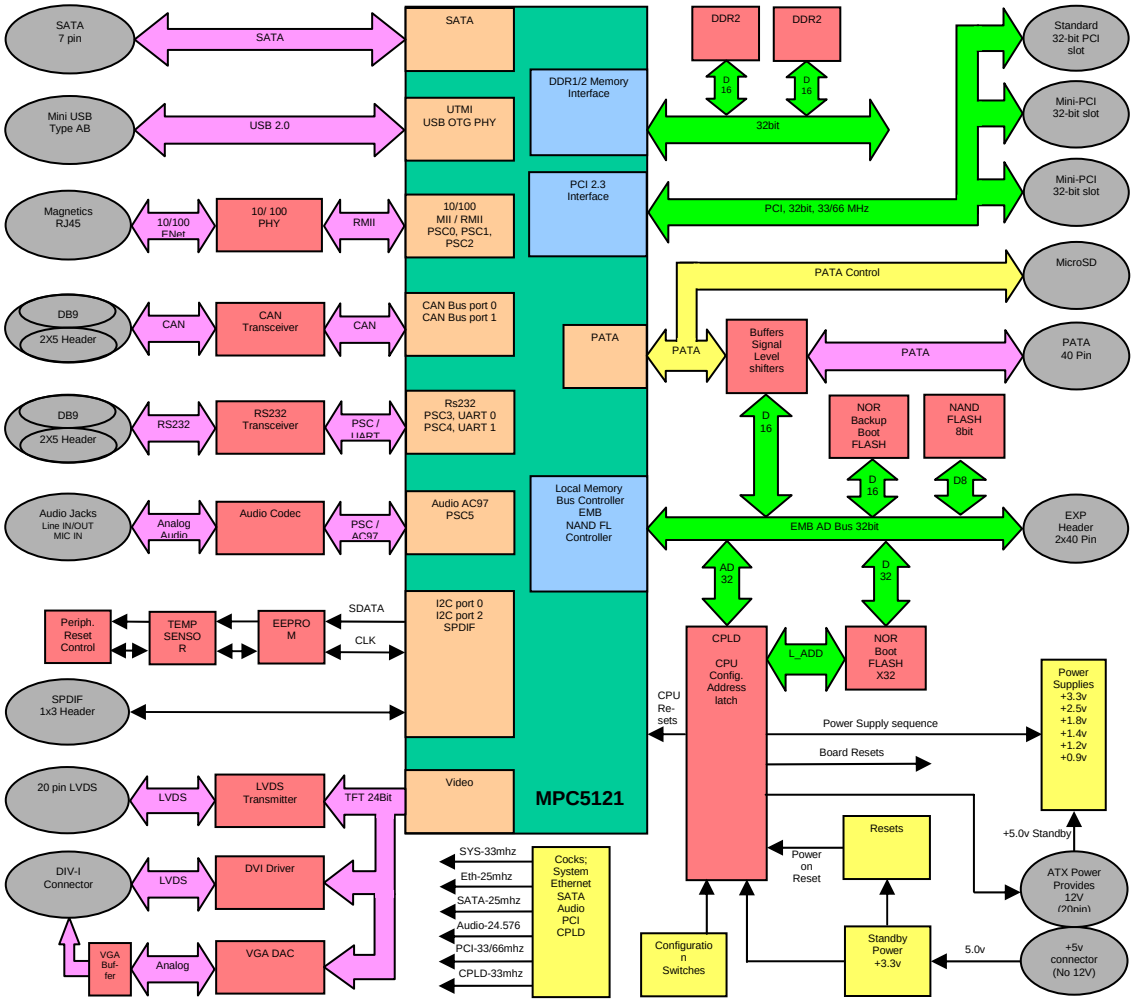


Figure 4- Block Diagram of ADS512101 Board

2.2 Physical Specifications

This section contains general information on the ADS512101's physical characteristics.

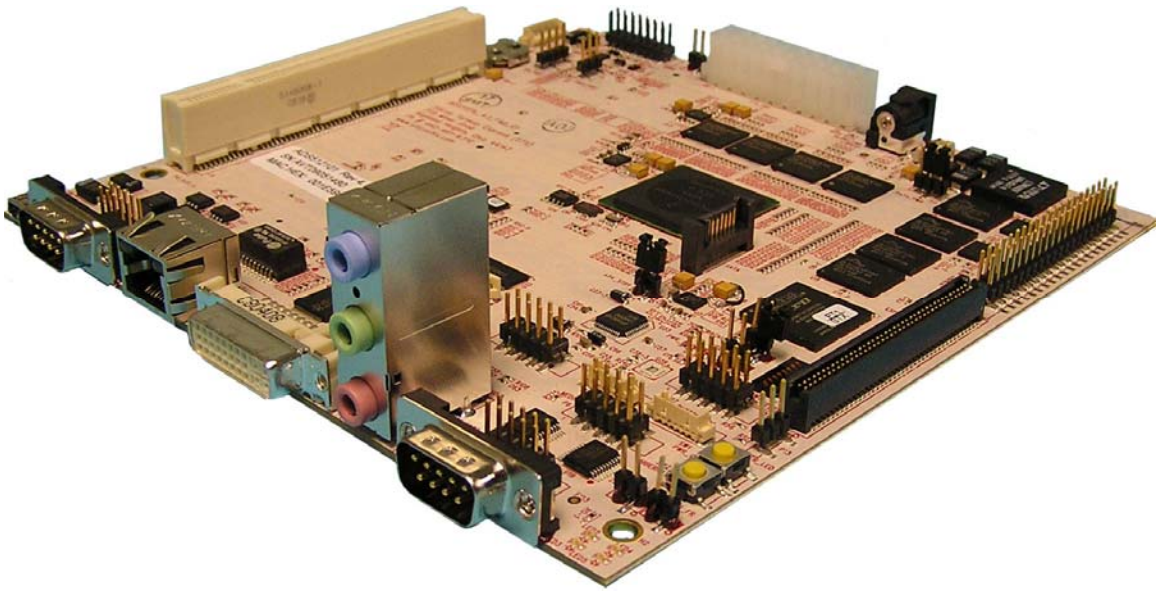


Figure 5 – ADS512101 Side View

Board Size.....mini-ITX (170mm x 170mm)
Power Requirement ..... ATX or 5VDC
Operating Temperature
Standard Version.....0^0 to $+70^0$C
Industrial Version.....-40^0 to $+85^0$C
Weight.....200g
RoHS.....Compliant

3.0 Control & Configuration

This section contains general set-up information about the various jumpers, switches, and LEDs found on the ADS512101 board. Section 3.1 describes the function and recommended switch settings. Section 3.2 describes the function and recommended jumpers on the board. Section 3.3 describes the LED indicator function.

3.1 Switch Settings

This section provides a brief description of the functionality and recommended settings for the switches located on the ADS512101.

Refer to Figure 2 for the locations of these switches.

3.1.1 SW1 – Power On Reset

SW1 is a push button that provides a power on reset signal for the hardware on the ADS512101. The push button can be remotely locate with connector P27.

Push once to power on board and push and hold for five seconds to power down board.

3.1.2 SW2 – Hibernation Mode

SW2 provide a hibernation request to the ADS512101.

Push once to put ADS512101 in hibernation mode. Push again to bring ADS512101 out of hibernation.

3.1.3 SW3 – Boot Mode

CAUTION:	Failure to follow this caution may result in possible damage to the board. For proper operation these switches should be left in the factory default position.

SW3 Boot Mode (Continued)

SW3 is the ***CPLD Boot Configuration Reset functions*** of the ADS512101. Refer to CPLD Register 18, Section 5.19 for additional information.

SW3 is a single-pole single-throw (SPDT) 8-position switch used to configure the CPLD for booting the ADS512101 during power-up.

All switches should be set to factory default, normal operation, 'ON'.

Pos.	State	Function
1[1]	ON	High Boot
1[1]	OFF	Low Boot
2	ON	NOR Boot
2	OFF	NAND Boot
3	ON	PCI = 33MHz
3	OFF	PCI = 66MHZ[2]
4	ON	Watchdog Disabled
4	OFF	Undefined
5	ON	Core PLL = 1.5x
5	OFF	Core PLL = 2x
6-7	OFF-OFF	DDR2 = 200MHz
6-7	ON-OFF	DDR2 = 166.67MHz
6-7	OFF-ON	DDR2 = 133.33MHz
6-7	ON-ON	DDR2 = 133.33MHz
8	ON	Reserved
8	OFF	Reserved

[1]***Permanently wired in High Boot***
[2]***M66en must also be high for 66mhz***

3.2 Jumper Settings

This section provides a brief description of the functionality and recommended settings for the jumpers located on the ADS512101. Refer to Figure 2 for the locations of these jumpers.

3.2.1 P01 – ATX Power Supply Operation

Default Open

This jumper must be installed to use an external 5volt power supply connected to PWR-2. It must be removed to use an ATX power supply.

3.2.2 P04 – Boot Backup FLASH

Default Open

When this jumper is installed powering the ADS512101 will launch U-Boot in a protected back up FLASH and reinstall U-Boot to main FLASH.

3.2.3 P11 – ATA Drive Voltage Select

CAUTION:	Failure to follow this caution may result in possible damage to the board. Be sure to select the correct voltage setting for the drive used prior to turning the power on to the board.

Default +3.3 Volts, Pins 1&2

Jumper P21 selects the appropriate power setting (+3.3 or +5.0) per the ATA specification for the drive in use.

Pin No	Description
1 - 2	PATA 3V PWR
2 - 3	PATA 5V PWR

3.2.4 P18 – EEPROM_WP

Default Open

With this jumper installed the EEPROM can be accessed allowing it to be programmed or erased as needed. When the jumper is removed the EEPROM cannot be programmed.

3.2.5 P25 – Power By-Pass

Default Open

With this jumper iinstalled the Power On switch is by-passed. The ADS512101 will launch U-Boot when power is applied.

3.3 LED Indicators

This section provides a list of functions for the LEDs on the ADS512101 board. Refer to Figure 2 for the locations of these LEDs.

See CPLD Register 17, Section 5.18, for additional information.

LED	Function	Color
1	5VDC GOOD	GREEN
2	USER DEFINED	RED
3	USER DEFINED	YELLOW
4	USER DEFINED	GREEN
5	USER DEFINED	GREEN
6	ATA ACTIVITY	GREEN

3.4 BT1 Battery

Use only a 3 Volt Lithium battery, properly sized for the socket. The battery is used for the Real Time Clock. The Real Time Clock in conjunction with the CPLD releases the Power Rail Regulators. See Section 6.2.1 for more information.

4.0 Schematic

The schematic and basic assembly information in a portable document format for the ADS512101 can be located on the CD in the STx Engineering Document Folder supplied with the board.

The ADS512101 design can be customized for optional flexibility and custom interfaces so the embedded systems engineer can obtain a lower overall parts cost using a variety of fixed and user selectable options.

These options inherently are contained in connectors, jumpers and switches on the board.

The schematic provides guidelines for using the already installed as well as user modifiable options available on the present design.

5.0 CPLD Configuration

The configuration CPLD controls the MPC5121e hard reset configuration word. The hardware configuration is controlled by switches SW3 to SW5 (see section 3.1.3 through 3.1.7) and documented in the following CPLD table. If all switches are set to ON, then the CPLD will drive the default configuration word.

Other functions of the CPLD are driven by or read by internal registers that are memory mapped at the base address 0x6000_0000. The CPLD uses the MPC5121e's chip select 2 on the local bus as its chip select and address decodes the lower 5 address bits. See the following table of CPLD registers descriptions for additional information.

5.01 CPLD Register 0

Board ID 1, used along with register 1

Base + 0x00

Bit #	A distinct board ID is assign to the board, 16bits 0x0001 = ADS5121e rev 04	Value at reset	Ability R/ W
7-0	Upper byte of Board ID	0x00	Read only

5.02 CPLD Register 1

Board ID 0, used along with register 0

Base + 0x01

Bit #	Bit description	Value at reset	Ability R/ W
7-0	Upper byte of Board ID	0x04	Read only

5.03 CPLD Register 2

CPLD Revision

Base + 0x02

Bit #	CPLD rev	Value at reset	Ability R/ W
7-0	CPLD rev info Writing a sequence of AA then 55 then 96	0x01	Read only

5.04 CPLD Register 3

Configuration word bits 33..32

Base + 0x03; 0x1010_1000 = default, CPLD drives Reset Configuration Word

Bit #	This register is reserved	Value at reset	Ability R/ W
7-2	Reserved	101010	Read / Write
1	RST_CONF_EMB_AX2	CFG_word_33	Read only
0	RST_CONF_EMB_AX3	CFG_word_32	Read only

5.05 CPLD Register 4

Configuration word bits 31..24

Base + 0x04**;** 0x0000_0001 = default, CPLD drives Reset Configuration Word

Bit #	Ability to read Configuration switches through software Switch definitions are from 5121 user manual HRW	Value at reset	Ability R/ W
7	RST_CONF_SYSDIV, EMB_AX0 driven 0	CFG_word_31	Read only
6	RST_CONF_SYSDIV System PLL divider	CFG_word_30	Read only
5	RST_CONF_SYSDIV	CFG_word_29	Read only
4	RST_CONF_SYSDIV	CFG_word_28	Read only
3	RST_CONF_SYSPLL System PLL Multiply factor	CFG_word_27	Read only
2	RST_CONF_SYSPLL	CFG_word_26	Read only
1	RST_CONF_SYSPLL	CFG_word_25	Read only
0	RST_CONF_SYSPLL	CFG_word_24	Read only

5.06 CPLD Register 5

Configuration switch settings (EMB_AD[23:16])

Base + 0x05; 0x1000_1101 = default, CPLD drives Reset Configuration Word

Bit #	Ability to read Configuration switches by software Switch definitions from 5121 user manual HRW	Value at reset	Ability R/ W
7	RST_CONF_SYSPLL System PLL Multiply factor	CFG_word_23	Read only
6	RST_CONF_CKS_IN Checkstop disabled	CFG_word_23	Read only
5	RST_CONF_NFC_DBW NAND data port 8bit	CFG_word_21	Read only
4	RST_CONF_NFC_PS NAND FLASH page size 2Kbytes	CFG_word_20	Read only
3	RST_CONF_LPC_DBW LPC DATA port 11 =32 bit	CFG_word_19	Read only
2	RST_CONF_LPC_DBW	CFG_word_18	Read only
1	Reserved, not mentioned in manual	CFG_word_17	Read only
0	RST_CONF_LPC_MX LPC Multiplexed mode	CFG_word_16	Read only

5.07 CPLD Register 6

Configuration switch settings (EMB_AD[15:8])

Base **+** 0x06; 0x0101_0000 = default, CPLD drives Reset Configuration Word

Bit #	Ability to read Configuration switches through software Switch definitions are from 5121 user manual HRW	Value at reset	Ability R/ W
7	RST_CONF_PCIARB enable PCI arbiter	CFG_word_15	Read only
6	RST_CONF_PCIHOST PCI Host mode	CFG_word_14	Read only
5	RST_CONF_COREPLL Core PLL Multiply factor	CFG_word_13	Read only
4	RST_CONF_COREPLL Core PLL Multiply factor	CFG_word_12	Read only
3	RST_CONF_COREPLL Core PLL Multiply factor	CFG_word_11	Read only
2	RST_CONF_COREPLL Core PLL Multiply factor	CFG_word_10	Read only
1	RST_CONF_LPC_AX No LPC Address Extension	CFG_word_09	Read only
0	RST_CONF_LPC_AX No LPC Address Extension	CFG_word_08	Read only

5.08 CPLD Register 7

Configuration switch settings (EMB_AD[7:0])

Base + 0x07; 0x0010_0000 = default, CPLD drives Reset Configuration Word

Bit #	Ability to read Configuration switches by software Switch definitions from 5121 user manual HRW	Value at reset	Ability R/ W
7	RST_CONF_PCI66EN M66EN signal, 1 = 66	CFG_word_07	Read only
6	RST_CONF_TLE Little ENDIAN	CFG_word_06	Read only
5	RST_CONF_BMS boot high	CFG_word_05	Read only
4	RST_CONF_COREDIS Core Disable mode (normal)	CFG_word_04	Read only
3	RST_CONF_TPR factory test mode disabled	CFG_word_03	Read only
2	RST_CONF_SWEN watchdog timer disabled at reset	CFG_word_02	Read only
1	RST_CONFIG_ROM_LOC LPC boot	CFG_word_01	Read only
0	RST_CONFIG_ROM_LOC LPC boot	CFG_word_00	Read only

5.09 CPLD Register 8

NOR FLASH Control

Base + 0x08

0x00000000 = default configuration, CPLD drives Reset Configuration Word

Bit #		Value at reset	Ability R/ W
7	Back up FLASH Write Protect 1 = (Full) write protected Write enable signal held high	1	Read / Write
6	Back up FLASH sector write protect	1	Read / Write
5	Boot FLASH Write Protect 1 = (Full) write protected Write enable signal held high	1	Read / Write
4	Boot FLASH sector write protect	1	Read / Write
3	NOR_FL_RDY	1	Read only
2	Boot or Backup FLASH status, 0 = Backup; 1 = Boot Dependant on P4 Jumper, jumper installed = Backup	x	Read only
	Or if 0xAA is written to register 2, R/W Control is immediate		Read/Write
1	Backup NOR FLASH reset, will be released from reset, at power up, if configuration is set for Backup FLASH	0	Read / Write
0	Boot NOR FLASH reset will be released from reset, at power up, if configuration is set for Backup FLASH	1	Read / Write

5.10 CPLD Register 9

NAND FLASH, CAN, MEDIA_GPIO Control

Base + 0x09

Bit #	Currently only NAND chip select 0 is used, chip select 1-3 are for future expansion.	Value at reset	Ability R/ W
7	MEDIA_GPIO	0	Read only
6	Reserved	0	Read / Write
5	Reserved	0	Read / Write
4	CAN Shut Down 0=Shut Down	0	Read / Write
3	NAND FLASH CE3 # enable 0=enabled	1	Read / Write
2	NAND FLASH CE2 # enable 0=enabled	1	Read / Write
1	NAND FLASH CE1 # enable 0=enabled	1	Read / Write
0	NAND FLASH CE0 # enable 0=enabled	0	Read / Write

5.11 CPLD Register 10

PCI Interrupt Masking

Base + 0x0A

Bit #	1 = interrupt is masked	Value at reset	Ability R/ W
7	PCI_INTB_SLOT3	1	Read / Write
6	PCI_INTA_SLOT3	1	Read / Write
5	PCI_INTB_SLOT2	1	Read / Write
4	PCI_INTA_SLOT2	1	Read / Write
3	PCI_INTD_SLOT1	1	Read / Write
2	PCI_INTC_SLOT1	1	Read / Write
1	PCI_INTB_SLOT1	1	Read / Write
0	PCI_INTA_SLOT1	1	Read / Write

5.12 CPLD Register 11

PCI Interrupt Status

Base + 0x0B

Bit #	PCI interrupts are received at the CPU on the PCI_INTN signal, this is a dedicated input on the CPU, 0 = pending, corresponding mask bit also must be cleared	Value at reset	Ability R/ W
7	PCI_INTB_SLOT3	1	Read only
6	PCI_INTA_SLOT3	1	Read only
5	PCI_INTB_SLOT2	1	Read only
4	PCI_INTA_SLOT2	1	Read only
3	PCI_INTD_SLOT1	1	Read only
2	PCI_INTC_SLOT1	1	Read only
1	PCI_INTB_SLOT1	1	Read only
0	PCI_INTA_SLOT1	1	Read only

5.13 CPLD Register 12

Interrupt Routing Selection between CPU IRQ0 or IRQ1

Base + 0x0C

Bit #	Controls which IRQ is used for the listed IRQs 0 = CPU_IRQ0, 1 = CPU_IRQ1	Value at reset	Ability R/ W
7	SW1_HIBERNATE#	0	Read / Write
6	Secure Digital Card (SD_CD#)	0	Read / Write
5	TOUCH_SCR_BUSYN	0	Read / Write
4	TOUCH_SCR_IRQN (off board)	0	Read / Write
3	FEC_PHY_INTN	0	Read / Write
2	TEMP_MON_INT	0	Read / Write
1	PCI Interrupts	0	Read / Write
0	RTC_INT#	0	Read / Write

5.14 CPLD Register 13

Interrupt Masking

Base + 0x0D

Bit #	1 = interrupt is masked	Value at reset	Ability R/ W
7	SW1_HIBERNATE#, writing 0 clears INT in register 14	1	Read / Write
6	Secure Digital Card (SD_CD#)	1	Read / Write
5	TOUCH_SCR_BUSYN	1	Read / Write
4	TOUCH_SCR_IRQN (off board)	1	Read / Write
3	FEC_PHY_INTN	1	Read / Write
2	TEMP_MON_INT	1	Read / Write
1	ALL PCI INT MASKING to CPU	1	Read / Write
0	RTC_INT#	1	Read / Write

5.15 CPLD Register 14

Interrupt Status

Base + 0x0E

Bit #		Value at reset	Ability R/ W
7	SW1_HIBERNATE# Must be cleared by writing value ‘0’ to register 13 bit 0	1	Read/Write
6	Secure digital card (SD)CD#)	1	Read/Write
5	Reserved	1	Read/Write
4	TOUCH_SCR_IRQN (off board)	1	Read/Write
3	FEC_PHY_INTN	1	Read/Write
2	TEMP_MON_INT	1	Read only
1	PCI INT, read CPLD register 11 for which PCI interrupt is asserted	1	Read/Write
0	RTC_INT#	1	Read/Write

5.16 CPLD Register 15

MISC Control 0

Base + 0x0F

Bit #		Value at reset	Ability R/ W
7	Hibernation event, must write '0' to clear this bit. This was removed and needs to be read within the CPU. See Hibernation Section 6.2.3 for detailed explanation.	0	Read / Write
6	TOUCH_RESET# (on board touch screen U38) rev 4 only	0	Read / Write
5	UART0_FOFF#	1	Read / Write
4	UART1_FOFF# ADS5121e_Rev 4 only	1	Read / Write
3	TOUCH_1_IRQ#_MASKING (on board touch screen U38) rev 4 only	1	Read only
2	TOUCH_1_IRQ# STATUS (on board touch screen U38) rev 4 only. CPU IRQ Routing is the same as set for the off board touch screen controller. Register 12 bit 4	1	Read only
1	PATA_RESET	1	Read only
0	FEC_PHY_RSTN	1	Read only

5.17 CPLD Register 16

Video Control 1

Base + 0x010

Bit #		Value at reset	Ability R/ W
7	LCD_LVDS_FRAME_RATE	0	Read / Write
6	Reserved	0	Read / Write
5	DVI_MSEN	0	Read only
4	LCD_LVDS_SDIRn	0	Read / Write
3	Reserved	0	Read only
2	DVI_DAC_PWRDNn	0	Read only
1	VGA_DAC_PWRDNn	0	Read only
0	LCD_PWR_DWNn	0	Read only

5.18 CPLD Register 17

User LED

Base + 0x011

Bit #		Value at reset	Ability R/ W
7	LED 3 Control, 0=LED0=Reset Status; 1=User Control register 17 (0)	0	Read / Write
6	LED 2 Control, 0=LED0=Reset Status; ; 1=User Control register 17 (0)	0	Read / Write
5	LED 1 Control, 0=LED0=Reset Status; ; 1=User Control register 17 (0)	0	Read / Write
4	LED 0 Control, 0=LED0=Reset Status; ; 1=User Control register 17 (0)	0	Read / Write
3	LED 3	0	Read / Write
2	LED 2	0	Read / Write
1	LED 1	0	Read / Write
0	LED 0	0	Read / Write

5.19 CPLD Register 18

Configuration Switch Settings, SW3

Base + 0x012

Bit #	SW3 Position	Function	Description	Value at reset 0 = OFF	Ability R/W
7	8	Reserved		0	Read only
5-6	7 & 6	cfg_sys_pll	00 = 200mhz DDR2 clock 01 = 166.67mhz DDR2 clock 10 = 133.33mhz DDR2 clock	00	Read only
4	5	cfg_core_pll	0 = 2x 1= 1.5x	0	Read only
3	4	cfg_watchdog	0 = disabled	0	Read only
2	3	cfg_PCI_speed	0 = 33mhz 0 = disabled M66en signal also must be high for 66mhz	0	Read only
1	2	cfg_NOR_boot	0 = NOR boot	0	Read only
0	1	cfg_LOW_boot	0 = high boot	0	Read only

6.0 Operation

All information contain this section is from STx's Design Requirements revision 4.0 dated August 27, 2008. For additional information or clarifications visit web site: www.silicontkx.com/support/index.php or email ADS512101@silicontkx.com.

6.1 Central Processing Unit

The ADS512101's MPC5121e is configured to run at a 33 Mhz system clock, and asynchronous mode 66 Mhz/33 Mhz PCI clock frequency. The initial configuration is driven from the main CPLD reading the configuration of switch SW3. The boot strap options will be selectable from a configuration dip switch read by the CPLD, the actual boot strap pins will be driven by the CPLD during reset only. The switch setting can also be read from the CPLD, see CPLD register 18.

The MPC5121 will be responsible for the PCI arbitration and interrupt controller.

The MCP5121 provides te interface to local on board resources including: NOR FLASH memory, NAND FLASH memory, DDR2-SDRAM memory, CPLD, MII (10/100 Fast Ethernet Controller), I2C (EEPROM, STM), PSC (programmable serial controller) for RS232 and AC97 (audio), Interrupt controller, USB 2.0 (ULPI), PCI bus, PCI controller, Graphics (on chip MBX) controller, PATA controller, SATA controller and Micro-SD.

See MPC5121e user manual for detail descriptions for each interface.

6.2 Power supplies

The ADS512101 board requires a mini-ATX power supply (20 pins connector can be used) or a 5v external power supply. When using a 5v external power supply functions requiring 12v will not operate. If a 5v external power supply is used jumper P1 is required. The jumper connects the 5v with the 5v-stby voltage which is required for the power up circuitry.

6.2.1 Power Rails

The ADS512101 board requires several power rails that are provided on board, and include:

+1.4v @ TBD for the CPU Core voltage.
+1.2v @ 0.5A for the CPU Core voltage.
+1.8v @ 4A for the CPU Core voltage.
+0.9v @ 3.3A for the CPU Core voltage.
+3.3v @ 2.0A for the CPLD, reset circuitry, clocks. CPU I/O, and peripheral logic.
+12v @ 2A (direct input from off-board power supply) for disk drive power and LCD.

Power Rails (continued)

The power enables for each of the regulators are used to sequence the power supplies. These will not release if the CPLD is not powered properly and the RTC clock are not running. These are open drain signals and work in tandem with the SS RC time constants of the regulators. They are used to Power-down the regulators in 0 time but allow the time constants of SS for Power-up.

6.2.2 Power Sequencing

Power sequencing rules require that the IO voltage rail is powered before the Core Voltages. This is controlled by the SS time constants of the Core regulators are longer than that of the IO regulators. During “sequenced” power down the CPLD will disable the Core regulators first and then disable the IO Regulators.

The normal controlled power down sequence will be (on SW1 Toggle).

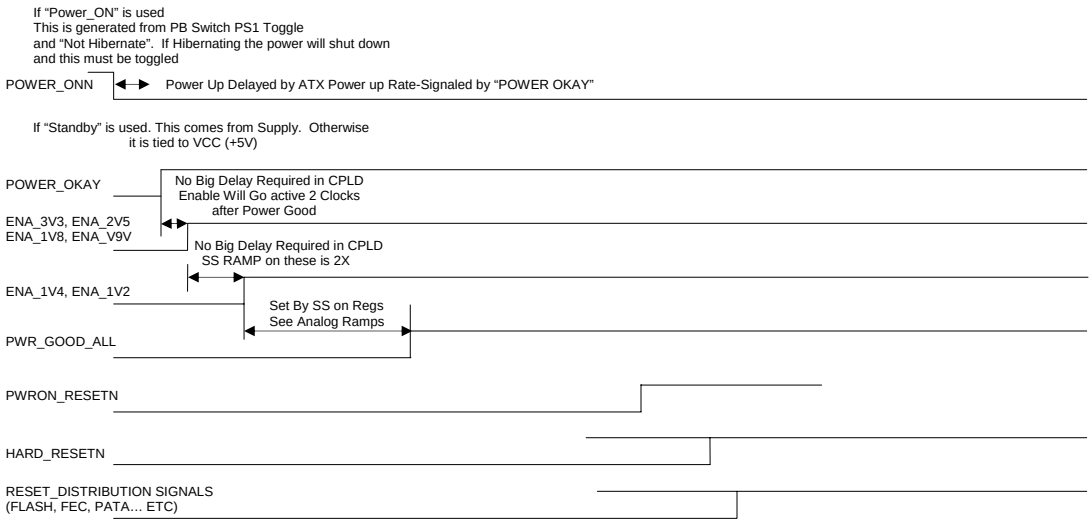
1: Assert PON_RESET (via MASTER_RESETN).
2: De-assert core Power - ENA_1V4, ENA1V2.
3: Wait some time.
4: De-assert IO Power - ENA_3V3, ENA2V5….etc.
5: De-assert (ATX)-POWER_ONN.

The Normal Power-UP sequence will be (on SW1 Toggle).

1: Assert (ATX)-POWER_ONN.
2: Assert IO Power - ENA_3V3, ENA2V5….etc.
3: Wait some time.
4: Assert core Power - ENA_1V4, ENA1V2.
5: Assert PON_RESET (via MASTER_RESETN).

The CPLD and the 8bit I/O expander control the power up and power down of the entire board.

Power On Sequencing



6.2.3 Hibernation Mode

Hibernate (Not Operational in Revision 1 or Revision 2 of ADS512101)

The Hibernate Pin from the CPU will shut down all of the regulators and devices that allow the MPC5121E to go into deep low power mode (Still TBD). Hibernate can wake or sleep per MPC5121E spec.

For controlled entry into the hibernate mode, the CPU must prepare the MPC5121e in anticipation of entering the hibernate mode, that is, having the power supply removed. The CPU must first write a value to the time target register that will give the MPC5121e enough time to complete all bus transactions in progress and shut down any other processes that must be terminated in an orderly manner and cause the MPC5121e to enter the hibernation mode before the HIB_MODE pin is asserted which will turn off the external power sources.

The external signals SET_WU_SRC[0:5] are used as external wakeup signals. See Chapter 32, Real Time Clock RTC, of the mpc5121e user manual.

SW2 is used as an external hibernate IRQ. See CPLD registers 12, 13, and 14.

After the CPU is in hibernation mode SW2 will generate an assertion of GPI31 signal which is a non-maskable wake from hibernation mode signal.

Hardware test can be performed as follows using the U-Boot command prompt.

DDR2 self refresh mode must be enabled.

Values can be written to DDR2 memory.

Location 0x0000_0000.

Read and confirm the RTC actual time counter is counting, register (offset 0x24).

Read location 0x80000a24

Write to the RTC keep Alive register and enable the hibernation mode.

Write to location 0x80000a28 the value 0x00000005.

To assert the CPU_HIB_Mode write to the RTC target time register. This will turn off the power supplies except for DDR and standby power.

Write to location 0x80000a20 the value 0xffffffff.

When SW2 button is pushed to power the board back up verify the CPU recognizes the GPI31 signal.

Read location 0x80000a28, bit 16 should be set to a 1, writing a 1 clears this bit.

The contents of the RTC target timer register (offset 20) should be cleared before clearing the set sticky bit, otherwise the CPU will perform another hibernate.

The contents of DDR can be verified that it is the same as prior to going into hibernate mode.

6.3 Resets

Two reset switches provide the on board resets.

Reset signal SW1_TOGGLE is connected to the power sequence (PS) CPLD and is the main “on/off” switch. This signal is used within the PS CPLD to enable or disable the on board power supplies. The PS CPLD will also enable all on board power supplies properly, and driving the MASTER_RESETN signal to the main power on reset and watchdog timer IC. Reset signal SOFT_RESETN is connected to:

The main CPLD for use by this device.
The CPU for the soft reset function.
The COP JTAG port, the COP JTAG can also drive this signal.

The main reset and watchdog timer device IC is held in reset until the PS CPLD has released the MASTER_RESETN signal. It then releases the PWRON_RESETN signal once an internal time delay (about 210ms) has been met. The PWRON_RESETN signal is used by the Configuration CPLD and clears its internal registers. It also is used by the CPU for its power on reset.

6.4 Clocks

The main clock driver is a programmable clock synthesizer IC. The SYS_CLK is the main processor clock (33.0 Mhz). The SYS_CLK_CPLD is used by the Configuration CPLD for synchronization to the CPU’s input clock and internal functions. The USB_CLK_24M000M is used by the CPU’s internal USB circuitry. The FEC_CLK_25M000M is used by both the CPU’s internal fast Ethernet circuitry and the Ethernet PHY. The SATA_CLK_25M000M is used by the CPU’s internal SATA drive circuitry. The CPLD_CLK_BASIC is used by the Configuration CPLD for internal functions. The AUD_CLK_24M576M is used by the Audio Codec U26.

6.5 CPU Configuration

The CPU configuration is completely user selectable by the bank of configuration switches SW3 to SW6. All 32 configuration signals are driven by the CPLD during power on reset only, and correspond to the 32 independent switch positions.

```
cfg_default_word <= '0' &    -- System Oscillator mode
                             (by-pass = 0 mode for Osc in, non xtal)
                             1 = sys osc mode

"000000" & -- System PLL divider (ax03, bits 31-27) = 0 00110 0011 = 33LPC, 100 DDR

  "0010"   & -- test as rev 2 -- System PLL Multiply factor (0010 = 12)(bits 26-23)

  "0101"   & -- System PLL Multiply factor (0010 = 12)(bits 26-23)
```

CPU Configuration (continued)

Default configuration: see table 7-3 Reset Configuration Word with in the MPC5121e user manual.

```
'0'      & -- bit22 Checkstop disabled
'0'      & -- bit21 NAND data port 8bit
'1'      & -- bit20 NAND FLASH page size 2Kbytes
"11"     & -- bit19-18 LPC DATA port =32 bit 11=x32, 01=x16
'0'      & -- bit17 not mentioned in table
'1'      & -- bit16 LPC Multiplexed mode
'0'      & -- bit15 enable PCI arbiter
'1'      & -- bit14 PCI Host mode
"0100"   & -- bit13-10 Core PLL Multiply factor
"00"     & -- bit09-08 No LPC address Extension
'0'      & --PCI_M66EN & -- bit07 M66EN signal, 1 = 66
'0'      & -- bit06 1 = Little ENDIAN, CFG_SW bit 1
'1'      & -- bit05 1 = boot high, CFG_SW bit 0
'0'      & -- bit04 Core Disable mode (normal), manual seems incorrect.
                    1 = disable (normal) but only 0 works
'0'      & -- bit03 0 = factory test mode disabled
'0'      & -- bit02 0 = watchdog timer disabled at reset
"00"     ; -- bit01-00 00 = LPC boot
```

6.6 Interrupts

The CPU has 2 interrupt sources; CPU_IRQ0 and CPU_IRQ1.

The EPIC can receive 56 separate interrupts from three different interrupt domains as follows:

- 2 external—off-chip interrupt signals sources are IRQ[1:0]
- 57 internal—on-chip interrupt signals sources are:
  - DDR MEMC, LPC, NFC, PATA, PCI, DMA, MU, FEC, PSC, FIFOC, USB, CSB arbiter, CAN, BDLC, DIU, AXE, SPDIF, SDHC, RTC, GTM, I2C, GPIO, GPT, SATA, MBX, TEMP, IIM and PMC.
- 1 external and 5 internal—off-chip interrupt signal source is IRQ0. On-chip MCP interrupt signals sources are
  - software watchdog timer (WDT), PCI, temperature sensor and system bus arbiter (SBA)

Interrupts (continued)

The CPLD accepts all other on board interrupts, and multiplexes these interrupts onto the CPU's IRQ signals. These will be user selectable, see CPLD registers 12 to 15.

PCI_INTN; PCI_INTC_SLOT1; FEC_PHY_INTN; PCI_INTD_SLOT1; PCI_INTA_SLOT2; PCI_INTB_SLOT2; PCI_INTA_SLOT3; PCI_INTB_SLOT3; PCI_INTA_SLOT1; PCI_INTB_SLOT1; PWR_CPLD_INT; WATCHDOG_BARK; TOUCH_SCR_IRQN; TOUCH_SCR_BUSYN; TEMP_MON_INT

6.7 Memory

6.7.1 DDR2 SDRAM

The dedicated DDR2 memory bus is 32 bits data, 200 MHz maximum, no ECC. It uses the MPC5121e DDR2 SDRAM controller and is directly connected to the MPC5121e.

6.7.2 NOR FLASH

The FLASH memory is 64 Mbytes total, 16 bits wide, and its interface consists of 3 devices; 2 banks of main FLASH and 1 bank of BOOT Flash. The FLASH uses the chip select LPC_CS0#. This chip select is connected to the CPLD, and the CPLD directs the appropriate NOR_FLx_CSN signal to the correct FLASH.

6.7.3 NAND FLASH

(Not operational in Revision 1 or Revision 2 of ADS512101)

Dedicated NAND FLASH memory is 1 GB and directly connected to the MPC5121e.

6.8 I/O Function

See Appendix B for pin definitions

6.8.01 10/100 Ethernet

The 10/100 Ethernet port uses the Freescale MPC5121e MII interface and a standard RJ45 connector with indicator LEDs and a 10/100 Ethernet PHY. The Port 0 PHY address is 00001.

6.8.02 RS232 Port (4-wire)

PSC (programmable serial controller) ports can be configured as UART, RS232 4 wire port. The PSC is configured within the MPC5121e, see user MPC5121e manual for details on setting up PSC. Transceivers are directly connected to both the CPU, a 9 pin D, DB9 connector and a 10 pin header.

6.8.03 CAN BUS

Two Individual Controller Area Network Buses are a 2 wire interface used mainly by the automotive industry. The CAN specification defines the Data Link Layer; ISO 11898 defines the Physical Layer. The CAN bus [CAN bus] is a balanced (differential) 2-wire interface running over either a Shielded Twisted Pair (STP), Un-shielded Twisted Pair (UTP), or Ribbon cable. Each node is connected to a male 9 pin D connector and a 10 pin header. The Bit Encoding used is: Non Return to Zero (*NRZ*) encoding (with bit-stuffing) for data communication on a differential two wire bus. The use of NRZ encoding ensures compact messages with a minimum number of transitions and high resilience to external disturbance.

Both CAN buses are directly connected to the MPC5121e's dedicated CAN bus and use a transceiver.

6.8.04 I2C Bus

Two I2C ports use Port 0 and Port 2.

Port 0 (I2C0) is used for:
Serial EEPROM with address set to binary 1, 0, 1, 0, A2, A1, A0, R/W, or 0xA0.
Temperature monitor with address set to binary 1, 0, 0, 1, A2, A1, A0, R/W, or 0x90.
Remote 8-bit I/O expander with address set to 0x70.
RTC with address hard coded at 0xD0. A battery backup is provided and is automatically switched within the device.
The RTC provides a square wave output:

RTC_CLK_OUT is connected to the CFG CPLD.
RTC_CLK_OUT is connected to the PS CPLD.
RTC_CLK_OUT is connected to the CPU as an optional input, instead of the XTAL X1

Port 2 (I2C2) is used for:

Digital potentiometer with address is hard coded to 0x5C.
Digital Transmitter with address is set to 0x70 read, 0x71 write.

6.8.05 AUDIO and Touch Screen controller

The MPC5121e use a PSC (programmable serial controller) set for the AC97 communication protocol. The audio codec is controlled by the AC97 controller and provides LINE IN, LINEOUT and MIC IN.

6.8.06 VIDEO

The MPC5121e has an integrated graphics engine, the PowerVR® MBX Lite IP core.
The MBX controller is directly connected to:
A 24-bit LVDS transceiver.
A Triple 8 bit video DAC with whose output is high speed video buffered then connected to the DVI-I connector.
A Digital transmitter that is connected to the DVI-I connector.

6.8.07 LCD Backlight

The LCD backlight has a circuit that could use a digital potentiometer, U31, to control the LCD backlight and is designed to be controlled directly from the CPU's I2C interface and addressed at 0x5C. However all revision 4.1 PCB uses a resistor to fix the LCD backlight brightness.

6.8.08 SATA Drive Interface

The MPC5121e directly connects to the SATA drive connector J5.

6.8.09 PATA Drive Interface

The PATA drive circuitry uses the MPC5121e PATA bus interface. The MPC5121 PATA interface connects to signal level translator ICs to convert from the CPU's +3.3v signal level to the PATA +5.0v signal level. The level translated signals are then connected to the PATA connector. The drive signal level voltage is selected with jumper P11. See section 3.2.2 for additional information.

The PATA power is enabled by an regulator and is controlled by the CPU's I2C0 bus. The signal PATA_PWR_ENABN enables the PATA_12V_PWR supplying the necessary +12v power to the PATA power connector.

6.8.10 PCI

The PCI slot is compliant to PCI2.3, 32 bit bus. It can either 33 MHz or 66 MHz which is determined by selectable clock with the Mode Switch, SW3. This is 3.3 volts only.

6.8.11 Mini-PCI

Two Mini-PCI slots are compliant to PCI2.3, 32 bit bus. It can either 33 MHz or 66 MHz which is determined by selectable clock with the Mode Switch, SW3. This is 3.3 volts only.

6.8.12 Micro-SD

A Micro-SD slot is available and is directly connected to the MPC5121e ATA controller.

7.0 U-Boot

7.1 Standard Commands

```
?                - alias for 'help'
askenv           - get environment variables from stdin
autoscr          - run script from memory
base             - print or set address offset
bdinfo           - print Board Info structure
boot             - boot default, i.e., run 'bootcmd'
bootd            - boot default, i.e., run 'bootcmd'
bootm            - boot application image from memory
bootp            - boot image via network using BootP/TFTP protocol
clocks           - print clock configuration
cmp              - memory compare
coninfo          - print console devices and information
cp               - memory copy
crc32            - checksum calculation
date             - get/set/reset date & time
dhcp             - invoke DHCP client to obtain IP/boot params
diufb init | addr - Init or Display BMP file
echo             - echo args to console
eeprom           - EEPROM sub-system
erase            - erase FLASH memory
exit             - exit script
fdt              - flattened device tree utility commands
flinfo           - print FLASH memory information
go               - start application at address 'addr'
help             - print online help
i2c              - I2C sub-system
icrc32           - checksum calculation
iloop            - infinite loop on address range
imd              - i2c memory display
iminfo           - print header information for application image
imls             - list all images found in flash
imm              - i2c memory modify (auto-incrementing)
imw              - memory write (fill)
imxtract         - extract a part of a multi-image
inm              - memory modify (constant address)
iprobe           - probe to discover valid I2C chip addresses
itest            - return true/false on integer compare
loadb            - load binary file over serial line (kermit mode)
loads            - load S-Record file over serial line
loady            - load binary file over serial line (ymodem mode)
loop             - infinite loop on address range
md               - memory display
mii              - MII utility commands
mm               - memory modify (auto-incrementing)
mtest            - simple RAM test
mw               - memory write (fill)
nfs              - boot image via network using NFS protocol
nm               - memory modify (constant address)
pci              - list and access PCI Configuration Space
ping             - send ICMP ECHO_REQUEST to network host
printenv         - print environment variables
protect          - enable or disable FLASH write protection
rarpboot         - boot image via network using RARP/TFTP protocol
reginfo          - print register information
reset            - Perform RESET of the CPU
run              - run commands in an environment variable
```

```
saveenv      - save environment variables to persistent storage
setenv             - set environment variables
sleep              - delay execution for some time
test               - minimal test like /bin/sh
tftpboot           - boot image via network using TFTP protocol
version            - print monitor version
```

7.2 Start Up Display

```
U-Boot 2008.10 (Dec 18 2008 - 13:33:44) MPC512X


CPU:   MPC5121e rev. 2.0, Core e300c4 at 399.999 MHz, CSB at 199 MHz
Board: ADS5121 rev. 0x0400 (CPLD rev. 0x06)
I2C:   ready
DRAM:  512 MB
FLASH: 64 MB
NAND:  1024 MiB
PCI:   Bus Dev VenId DevId Class Int
In:    serial
Out:   serial
Err:   serial
Net:   FEC ETHERNET

Type "run jffs2boot" to boot Linux
=> run jffs2boot
```

Figure 6 – U-Boot Start Screen

7.2.1 Linux Boot:

If Wind River's Linux has been pre-loaded in the ADS512101, it can be launched by typing:

=> run jffs2boot.

7.2.2 Environment Variables set by U-Boot

```
baudrate=115200
loads_echo=1
hostname=ads5121
bootfile=ads5121/uImage
u-boot_addr_r=200000
kernel_addr_r=600000
fdt_addr_r=880000
ramdisk_addr_r=900000
u-boot_addr=FFF00000
fdt_addr=FFEC0000
ramdisk_addr=FC040000
ramdiskfile=ads5121/uRamdisk
u-boot=ads5121/u-boot.bin
bootfile=ads5121/uImage
fdtfile=ads5121/ads5121.dtb
consdev=ttyPSC0
```

```
nfsargs=setenv bootargs root=/dev/nfs rw nfsroot=${serverip}:${rootpath}
${othbootargs}
ramargs=setenv bootargs root=/dev/ram rw ${othbootargs}
jffs2args=setenv bootargs root=/dev/mtdblock1 rw rootfstype=jffs2 ${othbootargs}
addip=setenv bootargs ${bootargs}
ip=${ipaddr}:${serverip}:${gatewayip}:${netmask}:${hostname}:${netdev}:off
panic=1
addtty=setenv bootargs ${bootargs} console=${consdev},${baudrate}
flash_nfs=run nfsargs addip addtty;bootm ${kernel_addr} - ${fdt_addr}
flash_self=run ramargs addip addtty;bootm ${kernel_addr} ${ramdisk_addr}
${fdt_addr}
net_nfs=tftp ${kernel_addr_r} ${bootfile};tftp ${fdt_addr_r} ${fdtfile};run
nfsargs addip addtty;bootm ${kernel_addr_r} - ${fdt_addr_r}
net_self=tftp ${kernel_addr_r} ${bootfile};tftp ${ramdisk_addr_r}
${ramdiskfile};tftp ${fdt_addr_r} ${fdtfile};run ramargs addip addtty;bootm
${kern
el_addr_r} ${ramdisk_addr_r} ${fdt_addr_r}
flash_jffs2=run jffs2args addtty;bootm ${kernel_addr} - ${fdt_addr}
load=tftp ${u-boot_addr_r} ${u-boot}
update=protect off ${u-boot_addr} +${filesize};era ${u-boot_addr}
+${filesize};cp.b ${u-boot_addr_r} ${u-boot_addr} ${filesize}
upd=run load update
ethaddr=00:1E:59:89:A8:14
kernel_addr=0xff900000
fdtflashaddr=0xffec0000
kernelflashaddr=0xffc40000
bmp_addr=0xffe40000
jffs2boot=set bootargs console=${consoledev},${baudrate} root=/dev/mtdblock1 rw
rootfstype=jffs2 ${othbootargs};cp.b ${fdtflashaddr} 0x3000000 0x200
000;bootm ${kernelflashaddr} - 3000000
bootcmd=run jffs2boot
loadaddr=1000000
dtbaddr=3000000
netdev=eth0
consoledev=ttyPSC0
targetname=MPC5121E_ADS
bootdelay=-1
othbootargs=diufb=15M video=fslfb:1024x768-32@60,monitor=0
rootpath=/export/5121
ethact=FEC ETHERNET
rootpath=/export/5121
nfsboot=setenv bootargs root=/dev/nfs rw nfsroot=192.168.170.102:/export/5121
ip=192.168.170.110:192.168.170.102::255.255.255.0:MPC5121E_ADS:eth0:of
f console=ttyPSC0,115200 diufb=15M video=fslfb:1024x768-32@60,monitor=0
filesize=1F4394
fileaddr=1000000
netmask=255.255.255.0
ipaddr=192.168.170.110
serverip=192.168.170.102
dtbfile=ads5121/mpc5121ads.dtb
root=/dev/mtdblock1 rw
rootfstype=jffs2
bootargs=root=/dev/mtdblock1 rw rootfstype=jffs2
ip=192.168.170.110:192.168.170.102::255.255.255.0:MPC5121E_ADS:eth0:off
console=ttyPSC0,115200 diuf
b=15M video=fslfb:1024x768-32@60,monitor=0
preboot=echo;echo Type \"bootm \$loadaddr - \$dtbaddr\" to boot Linux
stdin=serial
stdout=serial
stderr=serial
```

7.3 Re-Install U-Boot Instructions

The ADS512101 has a protected back up FLASH memory for U-Boot. If U-Boot should become corrupt for any reason, U-Boot can be re-installed. Please follow these instructions to re-flash U-Boot to the main memory.

1 – Remove power from the ADS512101

2 – Install a jumper on the 'Back Up Flash' Header, P4

3 – Reconnect power to the ADS5121 and use SW1 to launch U-Boot.

– This process will write the back up U-Boot to main memory.

– Follow the on screen instructions.

4 – Remove power from the ADS512101

5 – Remove the jumper from header P4.

6 – Reconnect power to the ADS512101 and use SW1 to launch U-Boot.

See Figure 7 for display text.

Re-install U-Boot display:

```
U-Boot 1.3.4 (Aug 27 2008 - 11:00:02) MPC512X


CPU:   MPC5121e rev. 2.0, Core e300c4 at 399.999 MHz, CSB at 199 MHz
Board: ADS5121 rev. 0x0400 (CPLD rev. 0x05)
I2C:   ready
DRAM:  512 MB
FLASH: 64 MB
PCI:   Bus Dev VenId DevId Class Int
In:    serial
Out:   serial
Err:   serial
Net:   FEC ETHERNET

BOOTING FROM BACKUP FLASH
RECOVERY MODE PROCESS STARTING AT AUTOBOOT...
Hit any key to stop autoboot:  0
Copy u-boot main flash image to dram
CRC32 for ff800000 ... ff832f3f ==> a3072f67
Switching to MAIN flash
Un-Protect Flash Bank # 1

.. done
Erased 2 sectors
PROGRAMMING MAIN FLASH

. done
Erased 1 sectors
Copy to Flash... done
CRC32 for fff00000 ... fff32f3f ==> a3072f67
Copy to Flash... done
Protected 2 sectors
SETTING UP NEW ENVIRONMENT in MAIN FLASH
SETTING BOOT PARAMETERS
SAVING ENVIRONMENT in MAIN FLASH
Saving Environment to Flash...
Un-Protected 1 sectors
Un-Protected 1 sectors
Erasing Flash...
. done
Erased 1 sectors
Writing to Flash... done
Protected 1 sectors
Protected 1 sectors
Saving Environment to Flash...
Un-Protected 1 sectors
Un-Protected 1 sectors
Erasing Flash...
. done
Erased 1 sectors
Writing to Flash... done
Protected 1 sectors
Protected 1 sectors

SELECT MAIN FLASH BY REMOVING JUMPER at P4

CYCLE POWER NOW -- Rebooting in 10 Seconds
```

Figure 7 –U-Boot Re-Installing Screen

8.0 Linux

8.1 Wind River Linux BSP

For current versions of Wind River's Linux visit www.windriver.com/products/bsp_web.

8.2 Linux Boot Display:

```
## Booting kernel from Legacy Image at ffc40000 ...
   Image Name:   Linux-2.6.27.18-WR3.0bg_standard
   Created:      2009-03-28   4:19:27 UTC
   Image Type:   PowerPC Linux Kernel Image (gzip compressed)
   Data Size:    2482754 Bytes =  2.4 MB
   Load Address: 00000000
   Entry Point:  00000000
   Verifying Checksum ... OK
## Flattened Device Tree blob at 03000000
   Booting using the fdt blob at 0x3000000
   Uncompressing Kernel Image ... OK
   Loading Device Tree to 007fb000, end 007ffe5c ... OK
Using MPC5121 ADS machine description
Linux version 2.6.27.18-WR3.0bg_standard (sgooch@utah) (gcc version 4.3.2 (Wind River
Linux Sourcery G++ 4.3-85) ) #1 PREEMPT Fri Mar 27 22:19:00 MDT 2009
MPC5121 ADS board from Freescale Semiconductor
Found FSL PCI host bridge at 0x0000000080008500. Firmware bus number: 0->0
PCI host bridge /pci@80008500 (primary) ranges:
 MEM 0x00000000a0000000..0x00000000afffffff -> 0x00000000a0000000 Prefetch
 MEM 0x00000000b0000000..0x00000000bfffffff -> 0x00000000b0000000
  IO 0x0000000084000000..0x0000000084ffffff -> 0x0000000000000000
Zone PFN ranges:
  DMA      0x00000000 -> 0x00020000
  Normal   0x00020000 -> 0x00020000
Movable zone start PFN for each node
early_node_map[1] active PFN ranges
    0: 0x00000000 -> 0x00020000
Built 1 zonelists in Zone order, mobility grouping on.  Total pages: 129920
Kernel command line: console=ttyPSC0,115200 root=/dev/mtdblock1 rw rootfstype=jffs2
diufb=15M video=fslfb:1024x768-32@60,monitor=0
IPIC (128 IRQ sources) at fcff7c00
PID hash table entries: 2048 (order: 11, 8192 bytes)
clocksource: timebase mult[5000002] shift[22] registered
Console: colour dummy device 80x25
console [ttyPSC0] enabled
Dentry cache hash table entries: 65536 (order: 6, 262144 bytes)
Inode-cache hash table entries: 32768 (order: 5, 131072 bytes)
Memory: 432000k/524288k available (5132k kernel code, 92088k reserved, 152k data, 150k
bss, 244k init)
SLUB: Genslabs=10, HWalign=32, Order=0-3, MinObjects=0, CPUs=1, Nodes=1
Calibrating delay loop... 99.84 BogoMIPS (lpj=199680)
Security Framework initialized
Mount-cache hash table entries: 512
Initializing cgroup subsys debug
Initializing cgroup subsys ns
Initializing cgroup subsys cpuacct
Initializing cgroup subsys memory
Initializing cgroup subsys bio
Initializing cgroup subsys devices
Initializing cgroup subsys memrlimit
```

```
Initializing cgroup subsys tc
net_namespace: 784 bytes
NET: Registered protocol family 16
Could not initialize clk spdif_txclk without a calc routine
Could not initialize clk spdif_rxclk without a calc routine
Reserved irq 66(0x42) for MBX
mapped ioctl to e1004000 and gpioctl to e1006100
hwtimer: Added mpc512x hwtimer (MPC512x General-purpose timer) at index=0
WDT driver for MPC8xxx/MPC512x initialized. mode:reset timeout=65535 (64 seconds)
PCI: Probing PCI hardware
bus: 00 index 0 io port: [0, ffffff]
bus: 00 index 1 mmio: [a0000000, afffffff]
bus: 00 index 2 mmio: [b0000000, bfffffff]
SCSI subsystem initialized
usbcore: registered new interface driver usbfs
usbcore: registered new interface driver hub
usbcore: registered new device driver usb
NET: Registered protocol family 2
IP route cache hash table entries: 16384 (order: 4, 65536 bytes)
TCP established hash table entries: 65536 (order: 7, 524288 bytes)
TCP bind hash table entries: 65536 (order: 6, 262144 bytes)
TCP: Hash tables configured (established 65536 bind 65536)
TCP reno registered
NET: Registered protocol family 1
Registering unionfs 2.2-mm
JFFS2 version 2.2. (NAND) © 2001-2006 Red Hat, Inc.
msgmni has been set to 844
io scheduler noop registered
io scheduler anticipatory registered
io scheduler deadline registered
io scheduler cfq registered (default)
LTT : ltt-relay init
Freescale DIU driver
Console: switching to colour frame buffer device 128x48
fb0: Panel0 fb device registered successfully.
fb1: Panel1 AOI0 fb device registered successfully.
fb2: Panel1 AOI1 fb device registered successfully.
fb3: Panel2 AOI0 fb device registered successfully.
fb4: Panel2 AOI1 fb device registered successfully.
Serial: MPC52xx PSC UART driver
80011300.serial: ttyPSC0 at MMIO 0x80011300 (irq = 40) is a MPC52xx PSC
80011400.serial: ttyPSC1 at MMIO 0x80011400 (irq = 40) is a MPC52xx PSC
brd: module loaded
console [netcon0] enabled
netconsole: network logging started
eth0: fs_enet: 00:00:1e:59:89:80
FEC MII Bus: probed
i2c /dev entries driver
Uniform Multi-Platform E-IDE driver
fc000000.flash: Found 2 x16 devices at 0x0 in 32-bit bank
 Amd/Fujitsu Extended Query Table at 0x0040
fc000000.flash: CFI does not contain boot bank location. Assuming top.
number of CFI chips: 1
cfi_cmdset_0002: Disabling erase-suspend-program due to code brokenness.
RedBoot partition parsing not available
Creating 5 MTD partitions on "fc000000.flash":
0x00000000-0x00040000 : "protected"
0x00040000-0x03c40000 : "filesystem"
0x03c40000-0x03ec0000 : "kernel"
0x03ec0000-0x03f00000 : "device-tree"
0x03f00000-0x04000000 : "u-boot"
MPC5121 MTD nand Driver 0.2
NAND device: Manufacturer ID: 0xad, Chip ID: 0xdc (Hynix NAND 512MiB 3,3V 8-bit)
```

```
2 NAND chips detected
mpc5121r2nfc 40000000.nfc: Using OF partition info
Creating 1 MTD partitions on "NAND":
0x00000000-0x40000000 : "nand"
mice: PS/2 mouse device common for all mice
rtc-m41t80 0-0068: chip found, driver version 0.06
rtc-m41t80 0-0068: rtc core: registered m41t62 as rtc0
mpc5121-rtc 80000a00.rtc: rtc core: registered mpc5121-rtc as rtc1
md: linear personality registered for level -1
md: raid0 personality registered for level 0
md: raid1 personality registered for level 1
md: raid10 personality registered for level 10
md: multipath personality registered for level -4
md: faulty personality registered for level -5
device-mapper: ioctl: 4.14.0-ioctl (2008-04-23) initialised: dm-devel@redhat.com
Freescale(R) MPC5121 DMA Engine found, 64 channels
fsldma: Self-test copy successfully
usbcore: registered new interface driver usbhid
usbhid: v2.6:USB HID core driver
Advanced Linux Sound Architecture Driver Version 1.0.17.
Freescale MPC5121 ADS ALSA SoC fabric driver
AC97 SoC Audio Codec 0.6
asoc: AC97 HiFi <-> psc5 mapping ok
ALSA device list:
  #0: MPC5121 ADS (AC97)
TCP cubic registered
NET: Registered protocol family 17
RPC: Registered udp transport module.
RPC: Registered tcp transport module.
rtc-m41t80 0-0068: hctosys: invalid date/time
md: Autodetecting RAID arrays.
md: Scanned 0 and added 0 devices.
md: autorun ...
md: ... autorun DONE.
VFS: Mounted root (jffs2 filesystem).
Freeing unused kernel memory: 244k init
init started: BusyBox v1.11.1 (2009-03-27 22:37:06 MDT)
starting pid 931, tty '': '/etc/init.d/rcS'
NET: Registered protocol family 10
[954] Jan 01 00:00:06 Running in background

Welcome to Wind River Linux

Please press Enter to activate this console.
starting pid 955, tty '': '-/bin/sh'


BusyBox v1.11.1 (2009-03-27 22:37:06 MDT) built-in shell (ash)
Enter 'help' for a list of built-in commands.

#
```

Appendix A – Memory Map

The following memory map isonly an example, refer to the MCP5121e user manual for specific memory map configurations, many of these memory map settings are user defined.

Function	Bytes	32 Bit Address		CS#	Size
	Reserved	Start	End		
IMMRBAR Default setting at reset FF40 0000 Move after boot		8000 0000	803F FFFF		1M Recommend. 4M For future revs
DDR SDRAM	256MB	0x0000 0000	0x0FFF FFFF	DDR_MCSN	256MB
BOOT Space EBC NOR FLASH Boot High	64MB	0xFC00 0000	0xFFFF FFFF	LPC_CS0N	64MB
NAND FLASH Upto 2GB	1MB	0x4000 0000	0x400F FFFF		1MB
PCI Memory PCILAWBAR0-2	256MB 256MB 256MB 256MB	0xA000 0000 0xB000 0000 0xC000 0000 0xD000 0000	0xAFFF FFFF 0xBFFF FFFF 0xCFFF FFFF 0xDFFF FFFF		1GB
SRAM	256KB	0x3000 0000	0x3001 FFFF		128KB
CPLD	32B	0x8200 0000	0x820F FFFF	LPC_CS2N	32B
MBX (graphics)	16MB	0x2000 0000	0x20FF FFFF		16MB
USB ULPI 2.0 Device	4KB	IMMR_0x3000	IMMR_3FFF		4KB
PATA Drive		IMMR_0x1 0200	IMMR_0x1 02FF		
SATA Drive		IMMR_0x2 0000	IMMR_0x2 1FFF		
Local Configuration Registers	1KB	IMMR_0x0 0000	IMMR_0xF FFFF		64B
RS232 A	PSC3	IMMR_0x1 1300	IMMR_0x1 13FF		
RS232 B	PSC4	IMMR_0x1 1400	IMMR_0x1 14FF		
Audio (AC97)	PSC5	IMMR_0x1 1500	IMMR_0x1 15FF		
CAN A		IMMR_0x0 1300	IMMR_0x0 137F		
CAN B		IMMR_0x0 1380	IMMR_0x0 13FF		
IIC0		IMMR_0x0 1700	IMMR_0x0 171F		32B
IIC2		IMMR_0x0 1740	IMMR_0x0 17FF		32B
Fast Ethernet Controller		IMMR_0x0 2800	IMMR_0x0 2FFF		256B

Appendix B – Connector Pin Assignments

J01 – Ethernet

Pin No	Description
1	TCT
2	TDP
3	TDN
4	RDP
5	RDN
6	RCT
7	LD1C
8	LD1A
9	LD2C
10	LD2A
1G	G1
2G	G2

J02– Audio Jack

Pin No	Description
1	SHIELD GND
J2C	Microphone
2	RIGHT MIC 2 (OUTER)
3	AGND
4	LEFT MIC 1 (INNER)
5	AGND
J2B	Line Out
22	RIGHT HP OUT (OUTER)
23	AGND
24	LEFT HP OUT (INNER)
25	AGND
J2A	Line In
32	RIGHT LINE IN (OUTER)
33	AGND
34	LEFT LINE IN (INNER)
35	AGND

J3/J4 – Mini PCI 2/3

Pin No	Description
1	TIP
2	RNG
3	8PMJ3
4	8PMJ1
5	8PMJ6
6	8PMJ2

J3/J4 – Mini PCI 2/3 continued

Pin No	Description
7	8PMJ7
8	8PMJ4
9	8PMJ8
10	8PMJ5
11	LED1P
12	LED2P
13	LED1N
14	LED2N
15	CHSGND
16	Reserved1
17	(not)INTB
18	5V1
19	3.3V1
20	(not)INTA
21	Reserved2
22	Reserved3
23	GND1
24	3.3VAUX1
25	CLK
26	(not)RST
27	GND2
28	3.3V2
29	(not)REQ
30	(not)GNT
31	3.3V3
32	GND3
33	AD31
34	(not)PME
35	AD29
36	Reserved4
37	GND4
38	AD30
39	AD27
40	3.3V4
41	AD25
42	AD28
43	RSVD5
44	AD26
45	C (not)BE3
46	AD24
47	AD23
48	IDSEL

J3/J4 – Mini PCI 2/3 continued

Pin No	Description
49	3.3V5
50	GND6
51	AD21
52	AD22
53	AD19
54	AD20
55	GND7
56	PAR
57	AD17
58	AD18
59	C (not)BE2
60	AD16
61	(not)IRDY
62	GND8
63	3.3V6
64	(not)FRAME
65	(not)CLKRUN
66	(not)TRDY
67	(not)SERR
68	(not)STOP
69	GND9
70	3.3V7
71	PERR N
72	(not)DEVSEL
73	C (not)BE1
74	GND10
75	AD14
76	AD15
77	GND11
78	AD13
79	AD12
80	AD11
81	AD10
82	GND12
83	GND13
84	AD9
85	AD8
86	C (not)BE0
87	AD7
88	3.3V8
89	3.3V9
90	AD6
91	AD5
92	AD4
93	Reserved6

J3/J4 – Mini PCI 2/3 continued

Pin No	Description
94	AD2
95	AD3
96	AD0
97	5V2
98	Reserved WIP1
99	AD1
100	Reserved WIP2
101	GND14
102	GND15
103	AC SYNC
104	(not)M66E
105	AC SDIN
106	AC SDOUT
107	AC BCLK
108	AC CODEC IO
109	AC CODECID1
110	(not)AC RESET
111	MOD AUDIO MON
112	Reserved7
113	AUDIO GND1
114	GND16
115	AUDIO OUT
116	AUDIO IN
117	AOUT GND
118	AIN GND
119	AUDIO GND2
120	AUDIO GND3
121	Reserved8
122	(not)MPCIACT
123	5VANA
124	3.3VAUX2

J06 – DVI-I

Pin No	Description
C1	ANALOG RED
C2	ANALOG GRN
C3	ANALOG BLUE
C4	ANALOG H-SYNC
C5_1	ANALOG RTN1
C5_2	ANALOG RTN2
1	TX2-
2	TX2+
3	TX2/4 SHLD
4	TX4-

J06 – DVI-I continued

Pin No	Description
5	TX4+
6	DDC CLK
7	DDC DATA
8	ANALOG V-SYNC
9	TX1-
10	TX1+
11	TX1/3 SHLD
12	TX3-
13	TX3+
14	5VDC
15	GND
16	TX0-
17	HP DETECT
18	TX0+
19	TX0/5 SHLD
20	TX5-
21	TX5+
22	TSC SHLD
23	TXC+
24	TXC-
25	SHELL1
26	SHELL2

P02 – MPC5121e JTAG

(16 pin Header)

Pin No	Description
1	5121E JTAG COP TDO
2	5121E JTAG COP QACKN
3	5121E JTAG COP TDI
4	COP CON TRSTN
5	TP110 JTAG COP HALTED
6	3.3VDC
7	5121E JTAG COP TCK
8	NC
9	5121E JTAG COP TMS
10	NC
11	SOFT RESET N
12	GND
13	HARD RESET N
14	NC
15	5121 CPU CHKSTP OUT
16	GND

P03 – Expansion Bus

Pin No	Description
1	GND
2	GND
3	EMB AD0
4	EMB AD1
5	EMB AD2
6	EMB AD3
7	EMB AD4
8	EMB AD5
9	EMB AD6
10	EMB AD7
11	3.3VDC
12	3.3VDC
13	EMB AD8
14	EMB AD9
15	EMB AD10
16	EMB AD11
17	EMB AD12
18	EMB AD13
19	EMB AD14
20	EMB AD15
21	GND
22	GND
23	EMB AD16
24	EMB AD17
25	EMB AD18
26	EMB AD19
27	EMB AD20
28	EMB AD21
29	EMB AD22
30	EMB AD23
31	3.3VDC
32	3.3VDC
33	EMB AD24
34	EMB AD25
35	EMB AD26
36	EMB AD27
37	EMB AD28
38	EMB AD29
39	EMB AD30
40	EMB AD31

P03 – Expansion Bus continued

Pin No	Description
41	GND
42	GND
43	LPC CS2N
44	EMB AX3
45	LPC ACKN
46	EMB AX2
47	LPC OEN
48	EMB AX1
49	LPC R WN
50	EMB AX0
51	PWR ON RESET N
52	TP117
53	HARD RESET N
54	TP118
55	GND
56	TIP116
57	LPC CLK
58	TP119
59	GND
60	GND
61	CPU GPIO14
62	TP115
63	CPU GPIO15
64	TP120
65	CPU GPIO28
66	TP114
67	CPU GPIO29
68	TP121
69	CPU GPIO30
70	TP113
71	CPU GPIO31
72	TP112
73	3.3VDC
74	3.3VDC
75	TP123
76	TP111
77	TP122
78	TP109
79	GND
80	GND

P05 – CPLD JTAG

(10 pin Header)

Pin No	Description
1	CPLD_TCK
2	GND
3	CPLD_TDO
4	5V_STANDBY
5	CPLD_TMS
6	NC
7	NC
8	NC
9	CPLD_TDI
10	GND

P06 – UART 0

(10 pin Header)

Pin No	Description
1	+3.3V
2	GND
3	CPU UART0 RTS
4	MEDIA GPIO 6
5	CPU UART0 TXD
6	TOUCH_0_IRO # 6
7	CPU UART0 RXD
8	CPU UART0 CTS
9	GND
10	+5.0V

P07 – UART 0

Pin No	Description
1	TP003
2	CSER UART0 RXD
3	CSER UART0 TXD
4	TP005
5	GND
6	TP004
7	CSER UART0 RTS
8	CSER UART0 CTS
9	TP006

P08 – UART 1

(10 pin Header)

Pin No	Description
1	NC
2	NC
3	UART1 RXD
4	UART1 RTX
5	UART1 TXD
6	UART1 CTS
7	NC
8	NC
9	GND
10	NC

P09 – CAN 0

Pin No	Description
1	TP011
2	CANL
3	GND
4	TP014
5	SIG GND
6	TP012
7	CANH
8	TP013
9	TP015

P10 – CAN 1

(10 pin Header)

Pin No	Description
1	NC
2	CANL
3	GND
4	NC
5	SIG GND
6	NC
7	CANH
8	NC
9	NC
10	NC

P12 – PATA Connector

Pin No	Description
1	PATA CON RESET
2	GND
3	PATA CON AD7
4	PATA CON AD98
5	PATA CON AD6
6	PATA CON AD9
7	PATA CON AD5
8	PATA CON AD10
9	PATA CON AD4
10	PATA CON AD11
11	PATA CON AD3
12	PATA CON AD12
13	PATA CON AD2
14	PATA CON AD13
15	PATA CON AD1
16	PATA CON AD14
17	PATA CON AD0
18	PATA CON AD15
19	GND
20	NC
21	PATA CON DRQ
22	GND
23	PATA CON IOWN
24	GND
25	PATA CON IORN
26	GND
27	PATA CON IOCHRDY
28	GND
29	PATA CON DACK
30	GND
31	PATA CON INTRQ
32	PATA CON IOCS16N
33	PATA CON DA1
34	NC
35	PATA CON DA0
36	PATA CON DA2
37	PATA CON CS0N
38	PATA CON CS1N
39	PATA CON DASPN
40	GND

P13 – ATA Activity

(2 pin Header)

Pin No	Pin Name
1	SIGNAL (PATA IO PWR + PATA CON DASPN
2	GND

P14 – PCI

Pin No	Pin Name
B1	-12V
A1	(not)TRST
B2	TCK
A2	12V
B3	GND0
A3	TMS
B4	TDO
A4	TDI
B5	5V 1
A5	5V
B6	5V 2
A6	(not)INTA
B7	(not)INTB
A7	(not)INTC
B8	(not)INTD
A8	5V 5
B9	(not)PRSNT1
A9	Reserved3
B10	Reserved1
A10	3.3V (I/O)
B11	(not)PRSNT2
A11	Reserved4
B12	--
A12	--
B13	--
A13	--
B14	Reserved2
A14	3.3v (AUX)
B15	GND1
A15	(not)RST
B16	CLK
A16	3.3V (I/O) 3
B17	GND2
A17	GNT
B18	(not)REQ
A18	GND9
B19	3.3V (I/O) 1
A19	(not)PME

P14 – PCI continued

Pin No	Pin Name
B20	AD31
A20	AD30
21B	AD29
A21	3.3V 7
B22	GND19
A22	AD28
B23	AD27
A23	AD26
B24	AD25
A24	GND10
B25	3.3V 1
A25	AD24
B26	C/(not)BE3
A26	IDSEL
B27	AD23
A27	3.3V 8
B28	GND20
A28	AD22
B29	AD21
A29	AD20
N30	AD19
A30	GND11
B31	3.3V 2
A31	AD18
B32	AD17
A32	AD16
B33	C/(not)BE2
A33	3.3V 9
B34	GND3
A34	(not)FRAME
B35	(not)IRDY
A35	GND12
B36	3.3V 3
A36	(not)TRDY
B37	(not)DEVSEL
A37	GND13
B38	GND4
A38	(not)STOP
B39	(not)LOCK
A39	3.3V 10
B40	(not)PERR
A40	Reserved5
B41	3.3V 4
A41	Reserved6
B42	(not)SERR

P14 – PCI continued

Pin No	Pin Name
A42	GND14
B43	3.3V 5
A43	PAR
B44	C/(not)BE1
A44	AD15
B45	AD14
A45	3.3V 11
B46	GND5
A46	AD13
B47	AD12
A47	AD11
B48	AD10
A48	GND15
B49	M66EN
A49	AD09
B50	GND6
A50	GND16
B51	GND7
A51	GND17
B52	AD08
A52	C/(not)BE0
B53	AD07
A53	3.3V 12
B54	3.3V 6
A54	AD06
B55	AD05
A55	AD04
B56	AD03
A56	GND18
B57	GND8
A57	AD02
B58	AD01
A58	AD00
B59	3.3V (I/O) 2
A59	3.3 (I/O) 4
B60	(not)ACK64
A60	(not)REQ64
B61	5V 3
A61	5V 6
B62	5V 4
A62	5V 7

P15 – J1850

(3 pin Header)

Pin No	Pin Name
1	CPU J1850 TX
2	CPU J1850 RX
3	GND

P16 – SPDIF

(4 pin Header)

Pin No	Pin Name
1	SPDIF TXCLK
2	SPDIF TX
3	SPDIF RX
4	GND

P17 – USB Mini AB Connector

Pin No	Pin Name
1	USB CONMB PWR
2	USB CONMB DN
3	USB CONMB DP
4	USB CONMB ID
5	GND
6	SHIELD GND
7	SHIELD GND
8	SHIELD GND
9	SHIELD GND

P19 – LCD Backlight

Pin No	Pin Name
1	12VDC
2	12VDC
3	GND
4	GND
5	LCD PWRDNN
6	B (DIGITAL POT 10K)
7	W (DIGITAL POT 10K)
8	NC

P20 – LCD (LVDS) Connector

Pin No	Description
1	D3+
2	D3-
3	DPS
4	FRC
5	GND1
6	CK+
7	CK-
8	GND2
9	D2+
10	D2-
11	GND3
12	D1+
13	D1-
14	GND4
15	D0+
16	D0-
17	GND5
18	GND6
19	VCC1
20	VCC2

P21 – LCD (TFT 18bit)

Pin No	Pin Name
1	GND
2	VID_CLK_0
3	VID_HSYNC
4	VID_VSYNC
5	GND
6	VID_RED0
7	VID_RED1
8	VID_RED2
9	VID_RED3
10	VID_RED4
11	VID_RED5
12	GND
13	VID_GREEN0
14	VID_GREEN1
15	VID_GREEN2
16	VID_GREEN3
17	VID_GREEN4
18	VID_GREEN5
19	GND
20	VID_BLUE0
21	VID_BLUE1
22	VID_BLUE2

P21 – LCD (TFT 18bit) continued

Pin No	Pin Name
23	VID_BLUE3
24	VID_BLUE4
25	VID_BLUE5
26	GND
27	VID_BLANK#
28	+LCD_TFT
29	+LCD_TFT
30	SCANDIR1
31	SCANDIR2
32	NC
33	NC

P22 – LCD Touchscreen

Pin No	Pin Name
1	TS_XP
2	TS_YP
3	TS_XM
4	TS_YM
5	GND

P23 – Power Switch

(2 pin Header)

Pin No	Pin Name
1	SW1 TOGGLEN (PULSE, DEBOUCE)
2	GND

P24 – Hibernate Switch

(2 pin Header)

Pin No	Pin Name
1	SW2_TOGGLEN
1	GND

P27 – UART 1 Interface

Pin No	Pin Name
1	3.3 V
2	5 V
3	GND
4	GND
5	UART1_TXD
6	UART1_RXD
7	NC
8	NC

P28 – Audio

(10 pin Header)

Pin No	Pin Name
1	AUD_C_AUX_R
2	AUD_C_AUX_L
3	GND
4	GND
5	AUD_C_LOUT_R
6	AUD_C_LOUT_L
7	AUD_C_CD_GND
8	AUD_C_CD_GND
9	AUD_C_CD_INR
10	AUD_C_CD_INL

P29 – Micro-SD

Pin No	Pin Name
1	NC/DAT2
2	CPU_PATA_DACK#/CD_DAT3
3	CPU_PATA_IOW#/CMD
4	3.3v/Vcc
5	CPU_PATA_IOR#/CLOCK
6	GND/GND
7	CPU_PATA_IOCHRDY/DAT0
8	CPU_PATA_INTRQ/DAT1
9	NC/NC1
10	NC/NC2
11	NC/NC3
12	SD-CD#/CD_SW1
13	GND/CD_SW2
14	GND/GND1
15	GND/GND2
16	GND/GND3
17	GND/GND4

P01 – 5Volt Stand-By

(2 pin Header)

Pin No	Pin Name
1	5V
2	5V Standby

PWR-1 – ATX Power Connector

Pin No	Description
1	3.3VDC (FUSED - F2)
2	3.3VDC (FUSED - F2)
3	GND
4	5V, ONLY (WALL PS OR 4PIN CONNECTOR)
5	GND
6	5V, ONLY (WALL PS OR 4PIN CONNECTOR)
7	GND
8	POWER OK
9	5V STANDBY
10	12VDC
11	3.3VDC (FUSED - F2)
12	-12VDC
13	GND
14	POWER_ONN
15	GND
16	GND
17	GND
18	NC
19	5VDC
20	5VDC

PWR-2 – 5V Power Connector

Pin No	Pin Name
1	5V
2	GND
3	Pwer_Basrrel 6
4	5V

Acronyms

Below is a list of common terms and acronyms you may find incorporated in this manual.

AC97 ..... Audio Codec driver
ATX ..... Advanced Technology Extended (mother board form factor)
AXE ..... 32-bit RISC Audio Acceleration Engine
BDLC ..... Byte Data Link Controller
CAN ..... Controller Area Network
COP ..... Debug Port
CPLD ..... Complex Programmable Logic Device
CPU ..... Central Processor Unit
DDR ..... Double Data Rate (RAM)
DMA ..... Direct Memory Access
DSP ..... Digital Signal Processor
DVI ..... Digital Video Interface/Input
EMB ..... External Memory Bus
FEC ..... Fast Ethernet Controller
GIGE ..... Gigabit Ethernet
GMII ..... Gigabit Media Independent Interface
GPIO ..... General Purpose Input/Output
GPT ..... General Purpose Timers
HDD ..... Hard Disk Drive
I^2C (IIC) ..... Inter-Integrated Circuit
J1850 ..... CAN Protocol (Ford, GM, Chrysler)
IPIC ..... Integrated Programmable Interrupt
JTAG ..... Test Port per IEEE 1149
LCD ..... Liquid Crystal Display
LPC ..... LocalPlus Bus
LVDS ..... Low Voltage Differential Signaling
MBX ..... Power VR® MBX Lite IP (Intergrated Graphics Engine by Imagination Technologies)
MDIO ..... Management Data Input/Output
Mini-ITX ..... Low Power Motherboard Standard (17cm x 17cm form factor)
NFC ..... NAND Flash Controller
OTG ..... On The Go (USB)
PATA ..... Parallel AT Attachment
PCI ..... Peripheral Component Interconnect
PMC ..... Power Management Control
PSC ..... Programmable Serial Channel
RAM ..... Random Access Memory
RGMII ..... Reduced Gigabit Media Independent Interface
RMII ..... Reduced Media Independent Interface
RTC ..... Real Time Clock
SAP ..... System Access Port
SATA ..... Serial Advanced Technology Attachment
SPDIF ..... Sony-Philips Digital-audio Interface Format
TLM ..... Tap Linking Module
TPM ..... Test Port to Magenta Module
TSEC ..... Triple Speed Ethernet Controller
USB ..... Universal Serial Bus
VBAT ..... Battery Voltage
WDT ..... Watchdog Timer
WP ..... Write Protect