New Design of Capillaries for Multi-Tier Wire Bonding

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Abstract: - The demand for increased computing power and more complex integrated circuit devices with increased functions per chip results in high lead-count integrated circuit packages. With the shrinkage in integrated circuit sizes towards smaller packages, and the decrease in pad pitch, the trend is moving from the current ultra-fine-pitch volume production of 50 µm to even lower pad pitches. However, the various concerns for 50-µm pitch bonding, such as low production yield, reliability issues, etc, have forced many customers to re-visit the feasibility of utilising the robust fine pitch bonding to handle the high lead-count packages. This paper reports the new development of bonding tools to handle the multi-tier wire bonding requirement with a maximum loop height of 475 µm. With the increase in the loop height of the wires, the bottleneck height of the capillary needs to be increased accordingly to prevent touching the adjacent wire during bonding. The increase in bottleneck height can influence the efficient transfer of the ultrasonic energy from the bonding tool to the bond interface and affect bond quality. In addition, the longer bottleneck height of the capillary also increases the risk of tip breakage during bonding. In this study, the external profile of the capillary is simulated with respect to the looping profile during bonding using a customised software package. In addition, finite element simulation is also utilised to analyse the difference in stress level with different bonding tool designs. The results of the simulations are then used to correlate with the actual bonding responses.

Key-Words: - Wire bonding, integrated circuit, capillary, design, fine pitch, stress.

1 Introduction

Historically, flip chip has the advantage over wire bonding process in terms of the number of I/Os. For a given chip size, the possible number of I/Os depends on the pad size, pad pitch and pad arrangement. A flip chip process using area array pad arrangement typically has about 4 times the number of I/Os of a conventional wire bonding process using peripheral pad arrangement for a 7 mm × 7 mm chip size [1-5].

Although a wire bonding process is limited by the number of I/Os, it is a matured technology and the process is well understood. In addition, the process is flexible whereby changes in chip size and new package design can easily be accommodated. However, to increase the number of I/Os, the bond pad pitch needs to be reduced to a finer pitch with smaller bond pads. This increases the level of difficulty during bonding due to the requirement for higher bond placement accuracy and improved bondability with a smaller deformed ball size.

Stack die packaging and multi-tier bonding were developed recently to handle such high lead-count packages. Such packages were mostly wire-bonded using the standard 70-µm pitch technology, which has proven to be reliable. In fact, multi-tier bonding is not new in the industry. Currently, two-tier (staggered) and tri-tier bonding has been the main stream of the sub-cons. Recent development to increase the layer of bonding from tri-tier to quad tier to further increase the lead count is currently in progress and expected to be in volume production in 2004. Figure 1 shows an example of tri-tier wire bonding using a 70-µm pitch.

2 Capillary Design Consideration

In multi-tier bonding, rows of wires protrude from the integrated circuit pads to provide connectivity to other parts of the package. The different rows of wires are isolated by different loop heights thus creating a vertical gap between the rows of wires in addition to the x-y separation to prevent shorting of the wires and the effect of mould sweep. Depending on the number of rows of wires, the loop height at the most inner row can be as high as 475 µm for a quad-tier bonding algorithm.

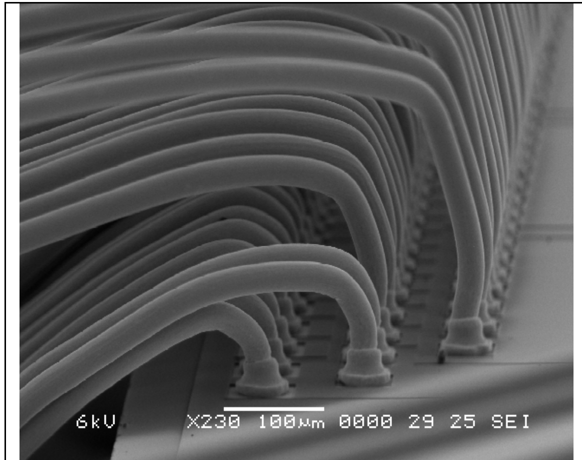


Fig. 1. Example of tri-tier wire bonding using a 70-µm pitch.

In this study, the capillary design needs to be altered to prevent the Main Taper Angle (MTA) of the capillary from hitting the adjacent wires during bonding. There are three key elements in the capillary design that are considered critical to prevent wire shorting during bonding: transition profile at the main taper/bottle neck angle, Bottleneck Height (BNH) and the tip diameter of the capillary.

2.1 Transition Profile

In this study, three different types of transition profile were considered. Design A has a sharp transition profile from the MTA to the Bottleneck Angle (BNA). Design B has a small radius transition while design C has a large radius transition of more than 200 µm. Two different transition profiles are shown in Figure 2. The different transition profiles can influence the ultrasonic energy transfer and tip breakage during bonding.

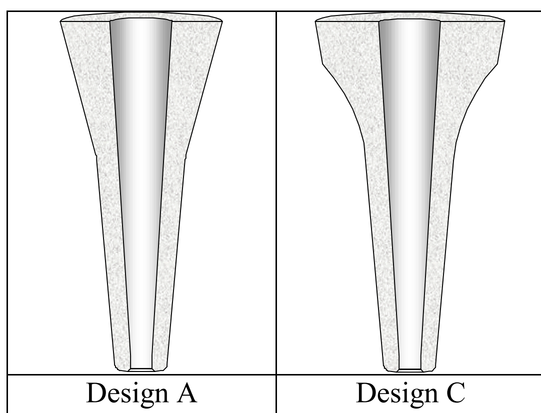


Fig. 2. Design A and design C.

2.2 Bottleneck Height/Tip Diameter

For fine pitch wire bonding, due to the close proximity of wires, the bottleneck of the capillary is used commonly to provide the necessary clearance between adjacent wires during bonding. In this study, the BNH of the capillary is controlled to be 350 µm with a tip diameter of 80 µm.

Selection for the other dimensions of the capillary was based on the bonding application for the 70-µm bond pad pitch, quad-tier pad arrangement using a wire size of 25 µm.

3 Capillary Profile Analysis

The capillary profile analysis was performed based on the looping profile as shown in Figure 3 with a maximum loop height of 475 µm at the inner row.

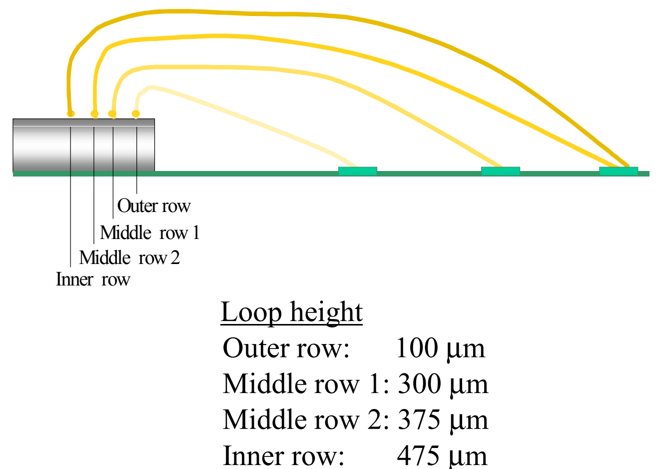


Fig. 3. Looping profile for quad-tier wire bonding.

The capillary profile and dimensions with the loop profile were input into a customised excel software package. This software allows the user to match the actual looping profile for the wire bonding application. In addition, the various capillary profiles can also be created into the software based on the critical dimension requirements. The interaction between the capillary profile and the looping profile can be analysed.

The analysis reveals that both design A and design C with a BNH of 350 µm are sufficient to clear a maximum loop height of 475 µm (indicated with the dotted lines in Figure 4) without any wire interference. However, it was found that the neck angle of the loop shapes significantly affect the performance of the looped wire. For multi-tier wire

bonding, the neck angle is normally controlled to be less than 10° to reduce the moulding wire sweep effect. On the contrary, the reduced neck angle can cause the interference of the adjacent wires during bonding. Based on the analysis, the minimum neck angle is determined to be 5°.

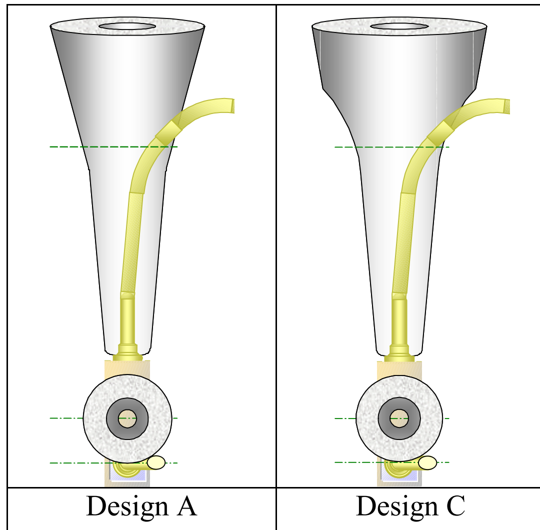


Fig. 4. Capillary profile analysis of design A and design C.

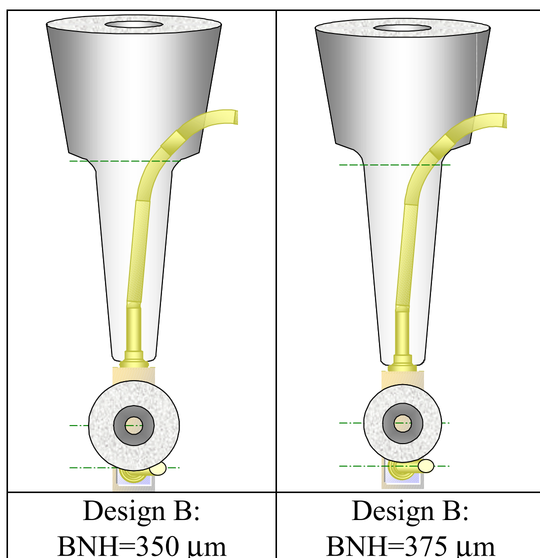


Fig. 5. Capillary profile analysis of design B.

For design B, it requires a BNH of 375 µm to prevent any interference with the adjacent wire. This is illustrated in Figure 5.

4 Finite Element Analysis

In this study, a technique for the bonding tool design was developed using FEA. The main objective is to study the stress level at the tip and the transition profile for different capillary designs. This analysis is crucial as the increase in the BNH dimension of the capillary can increase the risk of capillary breakage during production runs. Most of the time, the breakage occurs at the transition profile of the capillary.

The stress analysis of the capillary was performed using a software package "ANSYS". The considerations include:

- Critical capillary dimensions. These dimensions include BNH, BNA, transition profile and the tip diameter T, shown in Figure 6.
- Capillary. For the simulation, a ceramics-based zirconia composite capillary was used.

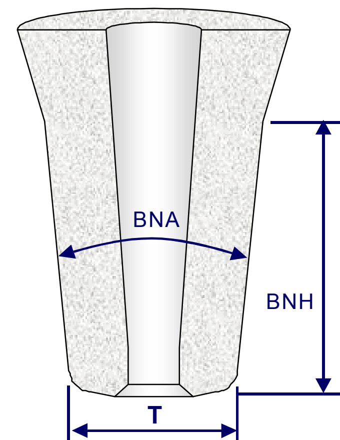
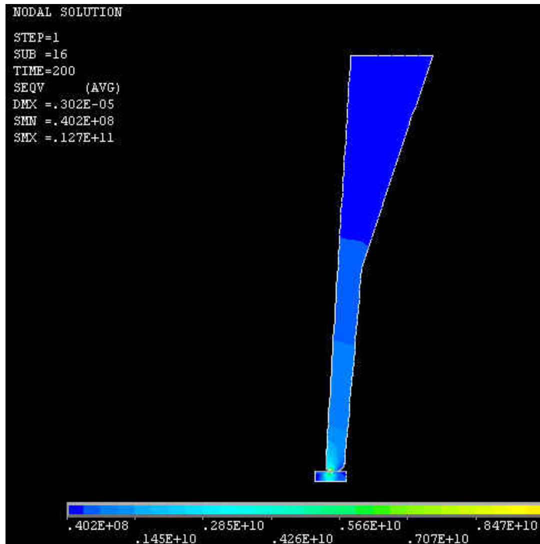
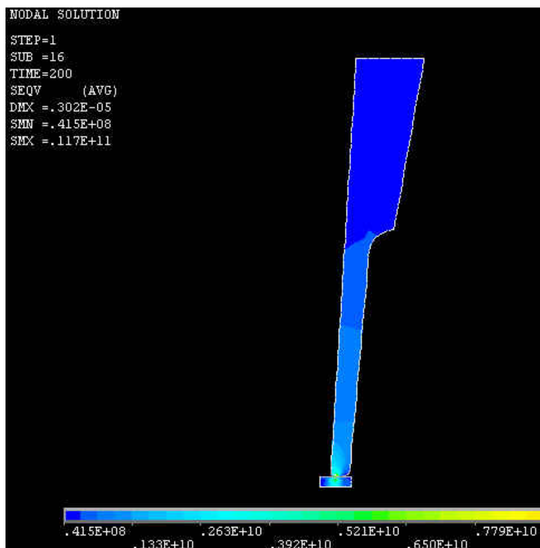


Fig. 6. Critical capillary dimensions consideration for multi-tier wire bonding.

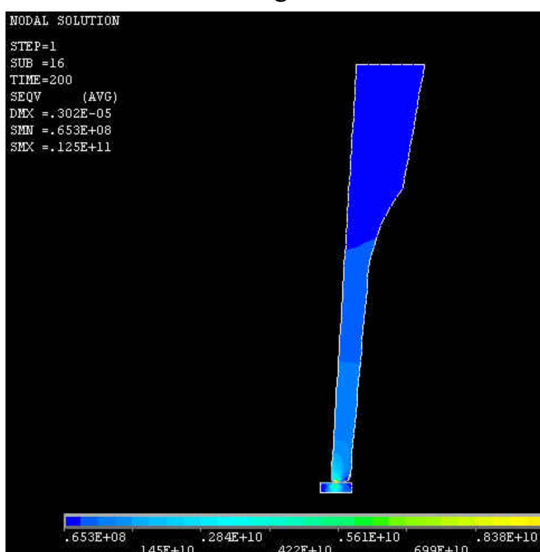
The stress levels obtained from the analysis can be represented in Figure 7. The analysis reveals that the maximum stresses for the various capillary designs occur at the tip of the capillaries. Design B has the lowest stress level. However, the differences are considered marginal. Destructive test was also performed to determine whether there is a significant difference in the shear reading at the MTA/BNA transition and the data together with the stress values obtained from the FEA are shown in Table 1. All the capillaries failed at the BNA/MTA transition. Breaking loads for design A and design C are about 3-7% lower than that for design B. This observation correlated with the results obtained from the FEA.



Design A



Design B



Design C

Fig. 7: Examples of FEA results showing the stress distributions.

Table 1. Results obtained from simulations and the destructive test

	Design A	Design B	Design C
Stress at tip (E+11 Pa)	0.1269	0.1167	0.1253
Stress at transition (E+09 Pa)	0.6632	0.5417	0.5687
Breakage load (gf)	228	245	238

5 Bonding Responses

Further verification on the simulation results was carried out on an ESEC 3100 wire bonder, with BGA substrate using a 25-µm wire size. Based on the inspection results, no wire disturbance was observed for all the bonded wires for the three capillary designs tested. However, it was noted that higher bonding parameters were needed for both design A and design C to achieve acceptable bond integrity. This observation was also confirmed from a laser interferometry test, as shown in Table 2. The test conducted has shown that the amplitude of vibration for design A and design C is about 10-16% lower than that for design B. No bondability issues were encountered for the ball and stitch bonds when wire bonding was performed on a BGA device with a 70-µm bond pad pitch.

Table 2. Wire bonding responses and laser interferometry test results

	Design A	Design B	Design C
Average ball size (µm)	52.6	53.8	53.3
Average ball shear (gf)	24.5	25.7	25.0
Average wire pull (gf)	7.32	7.54	7.41
Amplitude of vibration (nm)	454	544	488
Note: data collected based on the same parameter settings.			

6 Concluding Remarks

In multi-tier wire bonding, the main challenging factor is the loop profile and the consistency of the looping control. The external profile of the capillary has to be optimized so as to provide sufficient clearance to

prevent any interference to the adjacent wire during bonding. Based on the simulation results and bonding responses, all the three designs were capable of meeting the maximum loop height requirement of 475 µm without any wire interference. Ideally, design B is considered optimum for multi-tier wire bonding.

Wire bonding will still remain as the preferred choice for the integrated circuit packaging in years to come mainly because wire bonding has been a well-established technology, cost effective and flexible. Multi-tier wire bonding will allow chips that require higher I/O numbers to continue using wire bonding for the interconnection instead of migrating to flip chip bonding.

Future development on the multi-tier wire bonding will be the feasibility study for five-tier bonding applications and the impact on the looping control and wire sweep issues. Theoretical computation has shown that five-tier wire bonding using a 70-µm bond pad pitch platform has equivalent I/Os compared to flip chips with a 200-µm bond pad pitch.

7 Acknowledgment

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