

## N-Channel Power MOSFET

600V, 1A, 10Ω

### FEATURES

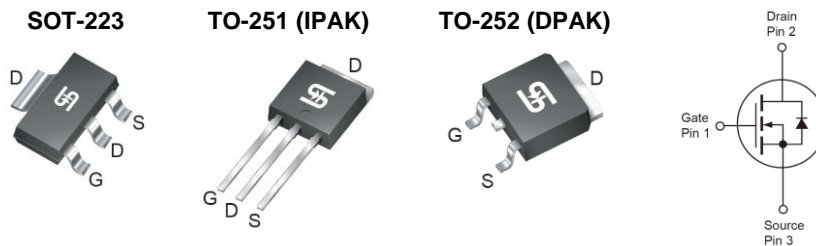
- Advanced planar process
- 100% avalanche tested
- Low  $R_{DS(ON)}$  8Ω (Typ.)
- Low gate charge typical @ 6.1 nC (Typ.)
- Low  $C_{rss}$  typical @ 4.2pF (Typ.)

### KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
$V_{DS}$	600	V
$R_{DS(on)}$ (max)	10	Ω
$Q_g$	6.1	nC

### APPLICATION

- Power Supply
- Lighting
- Charger



**Notes:** Moisture sensitivity level: level 3. Per J-STD-020

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	IPAK/DPAK	SOT-223	UNIT
Drain-Source Voltage	$V_{DS}$	600		V
Gate-Source Voltage	$V_{GS}$	±30		V
Continuous Drain Current <sup>(Note 1)</sup>	$I_D$	$T_C = 25^\circ\text{C}$		A
		$T_C = 100^\circ\text{C}$		
Pulsed Drain Current <sup>(Note 2)</sup>	$I_{DM}$	4		A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_{DTOT}$	39	2.1	W
Single Pulsed Avalanche Energy <sup>(Note 3)</sup>	$E_{AS}$	5		mJ
Single Pulsed Avalanche Current <sup>(Note 3)</sup>	$I_{AS}$	1		A
Peak Diode Recovery $dv/dt$ <sup>(Note 4)</sup>	$dv/dt$	4.5		V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150		°C

### THERMAL PERFORMANCE

PARAMETER	SYMBOL	IPAK/DPAK	SOT-223	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.87	--	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	110	60	°C/W

**Notes:**  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\theta JA}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.  $R_{\theta JA}$  shown below for single device operation on FR-4 PCB in still air.

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b> (Note 5)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	$BV_{DSS}$	600	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 0.5A$	$R_{DS(ON)}$	--	8	10	$\Omega$
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2.5	3.5	4.5	V
Zero Gate Voltage Drain Current	$V_{DS} = 600V, V_{GS} = 0V$	$I_{DSS}$	--	--	10	$\mu A$
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Forward Transfer Conductance	$V_{DS} = 10V, I_D = 0.5A$	$g_{fs}$	--	0.8	--	S
<b>Dynamic</b> (Note 6)						
Total Gate Charge	$V_{DS} = 480V, I_D = 1A, V_{GS} = 10V$	$Q_g$	--	6.1	--	nC
Gate-Source Charge		$Q_{gs}$	--	1.4	--	
Gate-Drain Charge		$Q_{gd}$	--	3.3	--	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{MHz}$	$C_{iss}$	--	138	--	pF
Output Capacitance		$C_{oss}$	--	17.1	--	
Reverse Transfer Capacitance		$C_{rss}$	--	4.2	--	
Gate Resistance	$F = 1\text{MHz}, \text{open drain}$	$R_g$	--	12.5	--	$\Omega$
<b>Switching</b> (Note 7)						
Turn-On Delay Time	$V_{DD} = 300V, R_G = 25\Omega, I_D = 1A, V_{GS} = 10V$	$t_{d(on)}$	--	7.7	--	ns
Turn-On Rise Time		$t_r$	--	6.8	--	
Turn-Off Delay Time		$t_{d(off)}$	--	15.3	--	
Turn-Off Fall Time		$t_f$	--	14.9	--	
<b>Source-Drain Diode</b> (Note 5)						
Diode Forward Voltage	$I_S = 1A, V_{GS} = 0V$	$V_{SD}$	--	0.9	1.4	V
Source Current	Integral reverse diode In the MOSFET	$I_S$	--	--	1	A
Source Current (Pulse)		$I_{SM}$	--	--	4	

**Notes:**

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3.  $L = 10\text{mH}, I_{AS} = 1A, V_{DD} = 50V, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$ .
4.  $I_{SD} \leq 1A, V_{DD} \leq BV_{DSS}, di/dt \leq 200A/\mu s$ , Starting  $T_J = 25^\circ\text{C}$ .
5. Pulse test:  $PW \leq 300\mu s$ , duty cycle  $\leq 2\%$ .
6. For DESIGN AID ONLY, not subject to production testing.
7. Switching time is essentially independent of operating temperature.

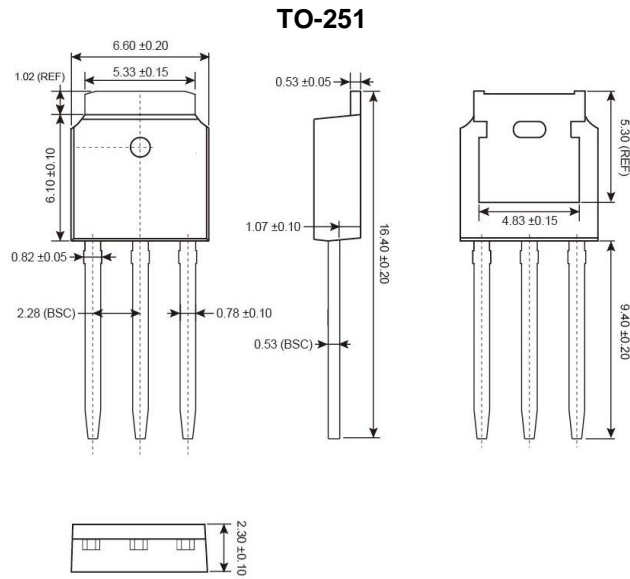
**ORDERING INFORMATION**

<b>PART NO.</b>	<b>PACKAGE</b>	<b>PACKING</b>
TSM1NB60CH C5G	TO-251	75 pcs / Tube
TSM1NB60CP ROG	TO-252	2,500 pcs / 13" Reel
TSM1NB60CW RPG	SOT-223	2,500 pcs / 13" Reel

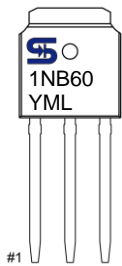
**Note:**

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)



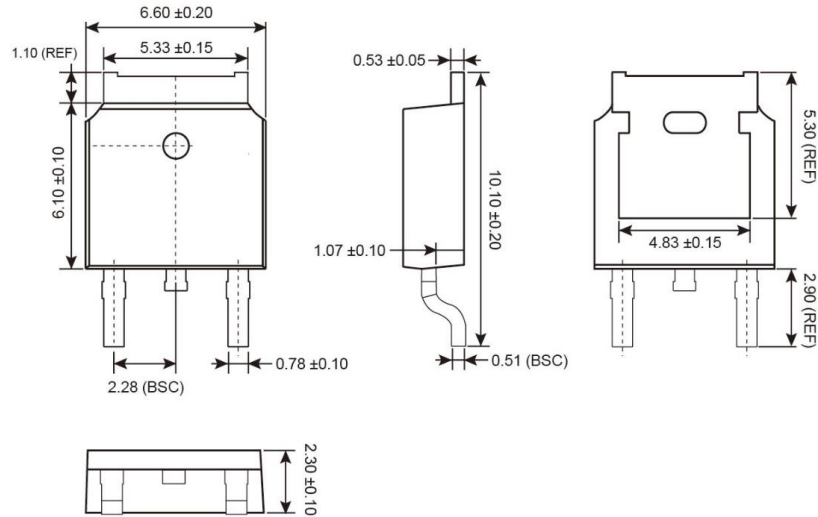
**MARKING DIAGRAM**



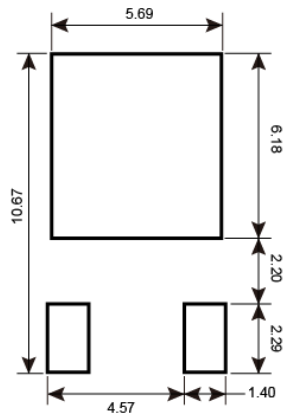
- Y** = Year Code
- M** = Month Code for Halogen Free Product
  - O** =Jan    **P** =Feb    **Q** =Mar    **R** =Apr
  - S** =May    **T** =Jun    **U** =Jul    **V** =Aug
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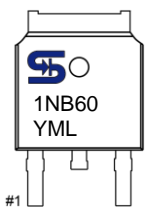
**TO-252**



**SUGGESTED PAD LAYOUT**



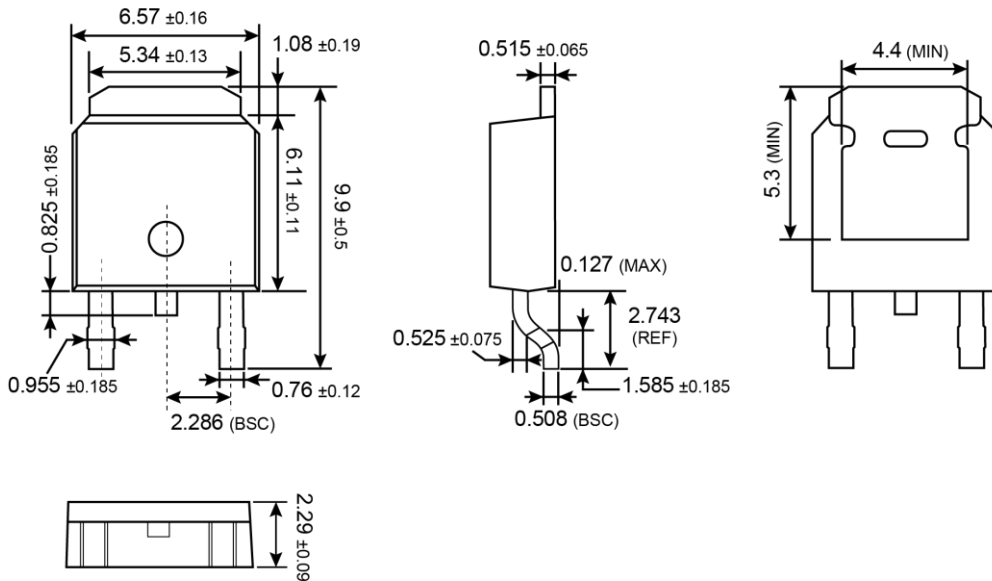
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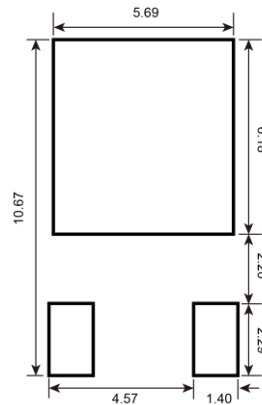
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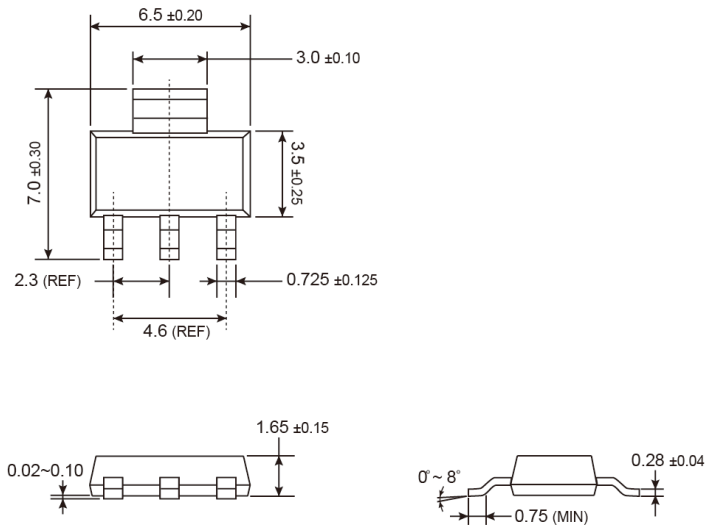
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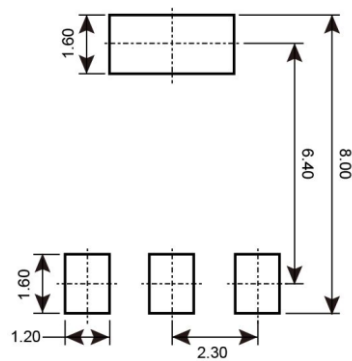
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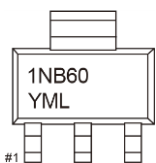
**SOT-223**



**SUGGESTED PAD LAYOUT**



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