Application Report
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Crystal Oscillator and Crystal Selection for the CC26xx and CC13xx Family of Wireless MCUs

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ABSTRACT

The CC26xx (CC2620, CC2630, CC2640, CC2650) and CC13xx (CC1310, CC1350) family is a low-power wireless MCU platform supporting multiple standards (that is, Bluetooth® low energy, IEEE® 802.15.4, and proprietary RF protocols). The devices have integrated 24-MHz and 32.768-kHz crystal oscillators TI designed for use with low-cost quartz crystals. The 24-MHz oscillator generates the reference clock for the RF blocks and the MCU system. RF systems are dependent on accurate clocks for correct operation. A deviation in clock frequency is reflected as a deviation in radio frequency. This deviation can degrade RF performance, violate regulatory requirements, or lead to a nonfunctioning system. In power-down mode, the high-frequency oscillator is typically turned off and a low-frequency oscillator is the system clock. For time-synchronized protocols such as Bluetooth Smart, a tight tolerance on the sleep clock enables longer time in low-power mode and reduced power consumption important in battery-powered applications. For this low-frequency oscillator, typically a 32-kHz crystal oscillator is used.

The scope of this application report is to discuss the requirements and trade-offs of the crystal oscillators for the CC26xx and CC13xx devices and provide information on how to select an appropriate crystal. This document also presents steps to configure the device to operate with a given crystal. You must configure the CC26xx and CC13xx based on the crystal used (that is, adjust the internal capacitor array to match the loading capacitor of the crystal for the 24-MHz oscillator). The application report also discusses some measurement approaches that may be used to characterize certain performance metrics, including crystal oscillator amplitude, and start-up time.

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1 Keywords

- Crystal oscillator
- Crystal selection
- IEEE 802.15.4
- RF4CE
- Bluetooth Smart
- Frequency tuning
- CC2620, CC2630, CC2640, CC2650
- CC1310, CC1350

2 Acronyms

Acronyms	Term
BLE	Bluetooth low energy
EM	Evaluation Module
IC	Integrated Circuit
ISM	Industrial, Scientific, Medical
LPRF	Low-Power RF
ppm	Parts per Million (1×10^{-6})
RF	Radio Frequency
RF4CE	Radio Frequency for Consumer Electronics
SoC	System on Chip
ESR	Equivalent Series Resistance

3 Oscillator and Crystal Basics

This section explains fundamentals of a quartz crystal and the oscillator operations required to understand the trade-offs when selecting a crystal for the CC26xx. The complete crystal oscillator circuit includes the loading capacitance, crystal, and the on-chip circuitry.

3.1 Oscillator Operation

The circuit used as high-accuracy clock source for TI’s low-power RF products is based on a Pierce oscillator as shown in Figure 1. There is no on-chip damping resistor and none must be added by the customer. The oscillator circuit consists of an inverting amplifier (shown as an inverter), a feedback resistor, two capacitors, and a crystal. When operating, the crystal and the capacitors form a pi filter that provides an 180-degree phase shift to the internal amplifier, keeping the oscillator locked at the specified frequency.

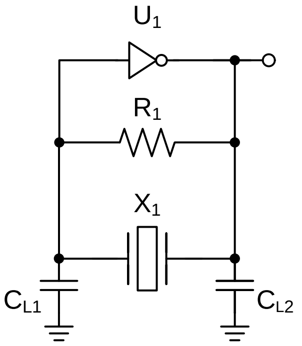

Figure 1. Pierce Oscillator

3.2 Quartz Crystal Electrical Model

A quartz crystal is a piezoelectric device that transforms electric energy to mechanical energy. This transformation occurs at the resonant frequency. Figure 2 shows the simplified electric model that describes the quartz crystal, where C_0 is the shunt capacitance, L_M is motional inductance, C_M is motional capacitance, and R_M is motional resistance. The model in Figure 2 is a simplified model and includes only the fundamental oscillation frequency. In reality, crystals can also oscillate at odd harmonics of the fundamental frequency.

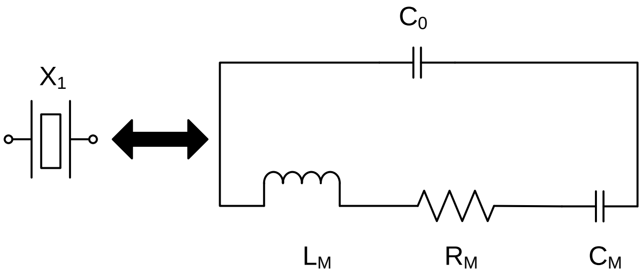

Figure 2. Crystal Symbol and the Electrical Model of a Quartz Crystal

3.2.1 Frequency of Oscillation

A crystal has two resonant frequencies characterized by a zero-phase shift. Equation 1 is the series resonance.

$$f_s = \frac{1}{2\pi\sqrt{L_M \times C_M}} \tag{1}$$

Equation 2 is the antiresonant frequency.

$$f_a = \frac{1}{2\pi\sqrt{L_M \times \frac{C_M \times C_0}{C_M + C_0}}} \tag{2}$$

As specified in the data sheet of the crystal, the frequency of oscillation is between the resonance frequencies. See Equation 3.

$$f_s < f_{XTAL} < f_a \tag{3}$$

3.2.2 Equivalent Series Resistance

The Equivalent Series Resistance (ESR) is the resistance the crystal exhibits at the series resonant frequency. Equation 4 gives the ESR.

$$\mathrm{ESR} = R_M \left(1 + \frac{C_0}{C_L}\right)^2 \tag{4}$$

Because C_0 is typically on the order of 1 pF and C_L is 5–9 pF, ESR is approximately R_M for many crystals, sometimes ESR is approximated as motional resistance.

3.2.3 Drive Level

The drive level of a crystal refers to the power dissipated in the crystal. The maximum drive level of a crystal is often specified in the data sheet of the crystal in µW. Exceeding this value can damage or reduce the life of the crystal. Equation 5 gives the drive level in W.

$$DL = ESR(\pi f(C_L + C_M)V_{pp})^2 \tag{5}$$

where:

V_{pp}— is the peak-to-peak voltage across the crystal

Calculating the DL with Equation 5 and comparing this value to the maximum specified DL in the crystal data sheet may reveal if the crystal is likely to have reliability issues during operation. Section 8 describes how to measure the value of Vpp.

3.2.4 Crystal Pulling

The crystal frequency can be pulled by changing the load capacitance. The parameter ΔF is the resonance frequency change of the crystal due to a change in its load capacitance. The pulling is given by Equation 6 around the specified (parallel) resonance frequency of the crystal.

$$\Delta F = \frac{F \times C_M}{2} \frac{C_{LMAX} - C_{LMIN}}{(C_0 + C_{LMAX})(C_0 + C_{LMIN})} \tag{6}$$

C_{LMAX} and C_{LMIN} are the maximum and minimum load capacitance that can be presented to the crystal. For more information, see Section 7. Table 3 shows how to change the internal load capacitance on the crystal using software

3.3 Negative Resistance

Negative resistance (R_N) is a parameter of the complete oscillator circuit, including capacitor values, crystal parameters, and the on-chip circuit. To ensure robust start-up of the crystal oscillator, the magnitude of the negative resistance must be at least 5 times greater than ESR during the initial start-up of the crystal but can be 2 to 3 times greater than ESR after start-up and during steady state operation. The following section shows an increasing negative resistance magnitude reduces the start-up time of the oscillator (see Equation 7).

$$ESR < \frac{|R_N|}{5} \tag{7}$$

Equation 8 approximates the negative resistance and shows that a low C_L gives a larger negative resistance.

$$R_N \approx \frac{-g_m}{(2\pi f)^2 (2C_L)^2} \tag{8}$$

where:

g_m— is the transconductance of the active element in the oscillator

C_L— is the load capacitance

You can also find the negative resistance of the circuit by introducing a resistor in series with the crystal. To avoid parasitic effects, TI recommends using a 0201 resistor for this task. The threshold of the sum of the extra 0201 external resistance and ESR or the crystal where the oscillator is unable to start up is approximately the same as the circuit negative resistance.

3.4 Time Constant of the Oscillator

The start-up time of a crystal oscillator is determined by transient conditions at turn-on, small-signal envelope expansion due to negative resistance, and large-signal amplitude limiting. The envelope expansion is a function of the total negative resistance and the motional inductance of the crystal. The time constant of the envelope expansion is proportional to the start-up time of the oscillator given by Equation 9.

$$\tau = \frac{-2L_M}{(R_M + R_N)} \approx \frac{-2L_M}{R_N}, \ |R_n| \gg |R_m| \tag{9}$$

A crystal with a low L_M gives a shorter start-up time and so does a high-magnitude R_N (low C_L). A trade-off exists between pullability due to low-motional capacitance (C_M) and fast start-up time due to low-motional inductance (L_M), because the frequency of the crystal is dependent on the both C_M and L_M. Crystals in smaller package sizes have larger L_M, and start more slowly than those in larger package sizes (see Section 3.2.1). Lowering C_L also reduces the drive level, allowing for an increase in oscillation amplitude (see Equation 5).

Table 1 summarizes crystal parameters and their values for the reference crystals recommended by TI for use with CC26xx and CC13xx.

Table 1. Crystal Parameters

Parameters	Description	24-MHz Crystal Used in TI Characterization	TI-Assumed Default 32.768-kHz Crystal
Motional Inductance (L_M)	Partly determines crystal speed (how quickly the crystal responds to a change from the oscillator). Lower L_m → crystal responds more quickly to changes from the oscillator. Along with C_M, a major determiner of the crystal quality factor	12.6 mH	5.0 kH
Motional Capacitance (C_M)	Partly determines crystal speed. Lower C_M → crystal responds more slowly to changes from the oscillator.	3.4 fF	4.718 fF
Motional Resistance (R_M)	At resonance, L_m and C_M cancel and R_M is presented to the oscillator. R_M ~ ESR assuming C_L >> C_O.	20 Ω (60-Ω maximum)	37 kΩ (70-kΩ maximum)
Load Capacitance (C_L)	The amount of load capacitor to tune the crystal to the correct frequency. This load capacitance also helps determine drive level.	9 pF	7 pF
Shunt Capacitance (C_O)	This is a parasitic capacitance due to crystal packaging. It helps determine the acceptable drive level.	1.2 pF	1 pF
ESR	Equivalent Series Resistance. If C_L >> C_O, then ESR ~ R_M	20 Ω (60-Ω maximum)	37 kΩ
Drive Level	The maximum level of power in the crystal for reliable long-term operation. $2 \times \text{ESR} (\omega (C_L + C_O)) \times V_{osc}$ where V_{osc} is the amplitude of the crystal oscillations.	200 µW	<500 nW

4 Overview of CC26xx and CC13xx Crystal Oscillators

The CC26xx and CC13xx have integrated 24-MHz and 32.768-kHz crystal oscillators that TI designed for use with low-cost quartz crystals. High-frequency (48 MHz) and low-frequency (32 kHz) RC oscillators are available on the CC26xx and CC13xx devices (beyond the scope of this application report).

4.1 24-MHz Crystal Oscillator

Figure 3 shows a simplified block diagram of the 24-MHz crystal oscillator. The oscillator circuit consists of an inverting amplifier, a feedback net, capacitors, and a crystal. The CC26xx and CC13xx have an internal capacitor array that can be adjusted and eliminates the requirement for external loading capacitors. The default setting of the internal capacitance is 9 pF, but this setting can be adjusted by register configuration within a range of 2 pF to 11 pF. For reliable operation, TI recommends operating the crystal with C_L from 5 to 9 pF. Section 7 shows how to set this value. If no external capacitors are used then the value of C_L is determined by the internal loading capacitors plus board parasitic capacitance.

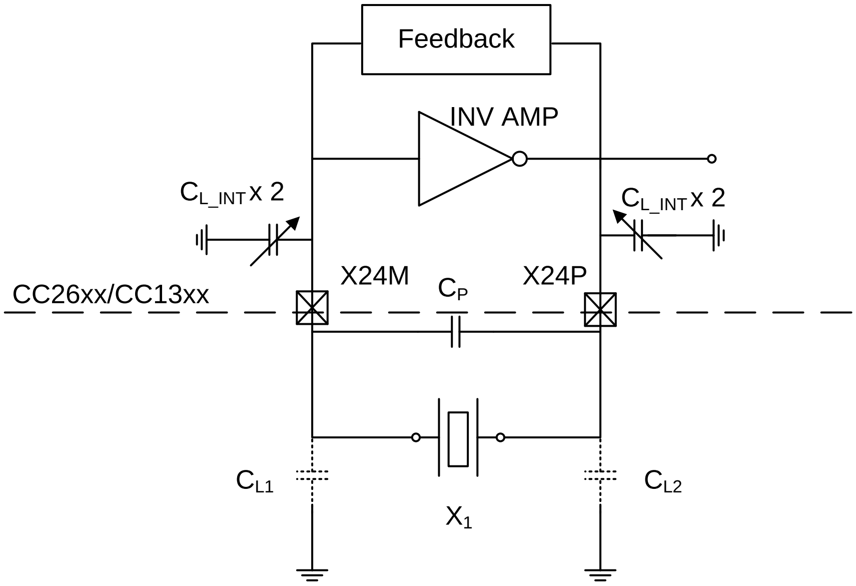

Figure 3. Simplified Block Diagram of the CC26xx and CC13xx High-Frequency Oscillator With Quartz Crystal

The 24-MHz crystal is controlled with a complex control loop described in Section 4.2 and Section 4.3.

4.2 24-MHz Crystal Control Loop

TI intends the amplitude control loop to regulate the amplitude of the oscillations of the crystal for optimal performance. The following are the two primary portions of the control loop:

- Start-up: The control loop injects as much current as possible into the oscillator that drives the crystal resonator.
- Steady state regulation: The amplitude of the crystal oscillator can be regulated in a steady state manner if required.

To turn on the crystal so that the radio can operate, start-up is required. Steady state amplitude regulation is not required for the crystal or radio to function.

4.3 32.768-kHz Crystal Oscillator

Figure 4 shows a simplified block diagram of the 32.768-kHz crystal oscillator. The oscillator circuit consists of an inverting amplifier, a feedback net, capacitors, and a crystal. The 32-kHz crystal lacks internal capacitors and requires external loading capacitors.

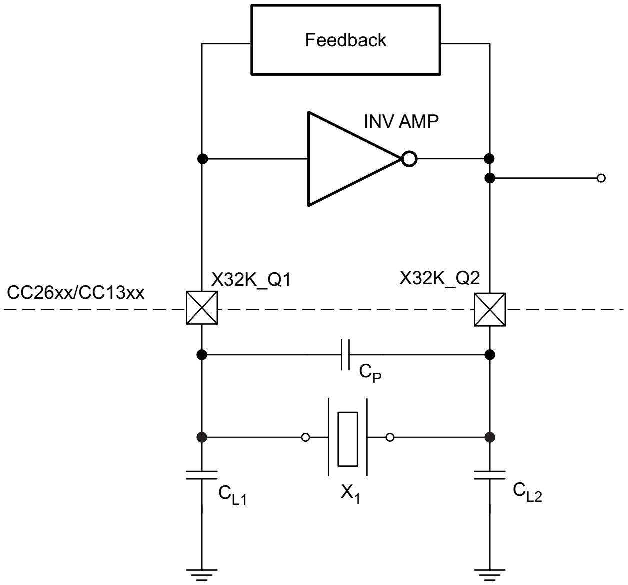

Figure 4. Simplified Block Diagram of the 32.768-kHz Oscillator With Quartz Crystal

5 Selecting Crystals for the CC26xx and CC13xx

This section presents some important considerations when selecting crystals for the CC26xx and CC13xx. CC26xx Crystals TI Wiki lists the crystals tested with the CC26xx and CC13xx. Selecting a crystal for a specific application depends on the following three factors:

- Size (footprint area and height)
- Performance (accuracy over temperature, lifetime, power consumption, and start-up time)
- Cost

Consider the following when selecting a crystal:

- Crystals must be selected to meet CC26xx and CC13xx data sheet or specification requirements
  - ESR must not be greater than can be driven by
  - CC26xx and CC13xx (60 Ω for the 24-MHz crystal). Capacitive loading and frequency tolerance must meet the specifications of the standard used (for example, Bluetooth)
  - Motional inductance must also meet specifications. Many crystal manufactures provide only motional inductance data upon customer request. TI has tested crystals with motional inductances up to the value specified in the data sheet (*CC2650 SimpleLink ™ Multistandard Wireless MCU*).
- Configuring the device
  - The required tuning capacitance of the 24-MHz crystal cannot lie outside of 2–11 pF unless external tuning capacitors are used.

NOTE: To achieve reliable results, keep the required tuning capacitance from 5 to 9 pF though a wider tuning range can be set.

  - The frequency accuracy of the 32.768-kHz crystal determines the accuracy of the sleep clock. The Bluetooth low energy (or other standard) stack must be updated to match the accuracy of the selected crystal

- Some other considerations when selecting a crystal include the following:
  - To improve start-up time and reduce power consumption, the crystal must have the following:
    - Low-capacitive loading, at the expense of greater susceptibility to frequency variation caused by the environment
    - Low-motional inductance
    - Low-motional resistance

5.1 Mode of Operation

Quartz crystals are used at the fundamental resonance frequency for frequencies relevant to the CC26xx and CC13xx, but there are crystals that operate at an odd overtone of the fundamental frequency. TI recommends using a crystal that operates at the fundamental mode for the CC26xx and CC13xx devices.

5.2 Frequency Accuracy

The total tolerance of the frequency accuracy of a crystal is dependent on several factors:

- Production tolerance
- Temperature tolerance
- Aging effects
- Frequency pulling of the crystal due to mismatched loading capacitance

When selecting the crystal, consider these parameters. Equation 10 gives the total crystal tolerance.

$$Tol_{tot} = Tol_{prod} + Tol_{temp} + Tol_{age} + Tol_{pull}\ (ppm) \tag{10}$$

These values are given in [ppm] (parts per million) and can be found in the data sheet of the crystal manufacturer, except pullability which can calculated by the formula in Section 3.

5.2.1 24-MHz Crystal

Because the 24-MHz crystal oscillator is used as a reference to generate the RF signal, any crystal frequency deviation is directly transferred to deviation of the RF signal. For example, 10 ppm leads a deviation in RF carrier frequency of 10 ppm. Select a crystal with performance within the limits of the RF specifications.

- For 802.15.4 (RF4CE/ZigBee®), the maximum deviation in carrier frequency is limited to ±40 ppm (see [1]).
- For Bluetooth core specifications 4.2, the limit is ±50 ppm (see [2]).

TI recommends using a 24-MHz crystal with a maximum 40-ppm total tolerance (including aging, temperature, and so forth).

5.2.2 32.768-kHz Crystal

The 32.768-kHz crystal oscillator is typically used as the system clock when the CC26xx and CC13xx devices are in a standby mode. Because Bluetooth low energy is a time-synchronized protocol, an accurate clock also enables longer periods of time in a low-power mode. If a lower-accuracy crystal is used, the device must wake up early to accommodate for the lower accuracy of the clock. If the 32.768-kHz crystal oscillator is used as the low-frequency clock in Bluetooth low energy, the clock must have a maximum of ±500 ppm of inaccuracy. For more information, see [2]. TI recommends using a tighter tolerance 32.768-kHz crystal to reduce the average power consumption in a typical Bluetooth low energy connection. In the *SimpleLink™ CC2650 EVM Kit 4XD (CC2650EM-4XD) v1.0.3 Design Files*, TI uses the Epson FC-135 crystal. If a crystal with different specifications is used, this setting must be adjusted for in the Bluetooth low energy stack. For more details, see Section 7.

The CC26xx device must be used with a 32.768-kHz crystal that has at least 500-ppm accuracy. TI recommends a crystal of 40-ppm accuracy.

See the FC-135 crystal at http://www.epsondevice.com/docs/qd/en/DownloadServlet?id=ID000805. The crystal has ±20-ppm frequency accuracy at room temperature but varies by 100 s of ppm overtemperature like other 32.768-kHz crystals. When specifying accuracy of the 32.768-kHz crystal, the accuracy over the entire temperature range, not just at room temperature, must be specified in the software stack.

Use the CC26xx and CC13xx devices only with a 32.768-kHz crystal that has at least 500-ppm accuracy over the desired operating temperature range. The Bluetooth low energy stack is by default set to 40-ppm accuracy. If a customer product is designed to operate over large temperature ranges, the customer must adjust this accuracy. Low-frequency tuning fork crystals have a resonance frequency that changes with temperature with a parabolic coefficient of (–0.04 × 10e – 6) / °C^2 typically. Figure 5 shows an example of this . In Figure 5, 40-ppm accuracy is maintained from –10°C to 50°C. Operating over wider temperature ranges requires the customer to adjust the Bluetooth low energy stack.

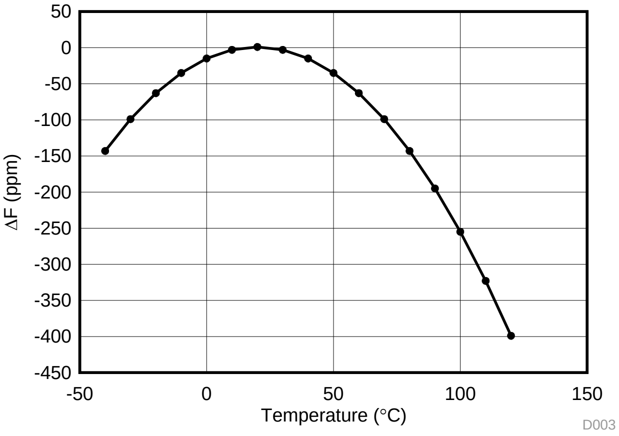

Figure 5. Typical Frequency vs Temperature Curve for a 32.768-kHz Tuning Fork Crystal

5.3 Load Capacitance

The crystal oscillator frequency is dependent on the values of the capacitive loading of the crystal. These capacitors with any parasitic capacitance in the PCB and the crystal terminals compose the total load capacitance that helps set the crystal resonance frequency. The crystal data sheet provides the optimum load capacitance for the crystal, C_L. This total C_L typically consists of both the loading capacitors and the parasitic capacitance of the layout and packaging.

Using external capacitors to get the correct frequency means that the internal caps must be set to minimum. For example, an application could use near minimum on-chip capacitance of approximately 2 pF and 7 pF of off-chip capacitor to get 9 pF. Table 2 shows using external caps this way gives slightly worse frequency stability with temperature than using internal capacitors.

Table 2. Using External Capacitor Results in Worse Frequency Stability Over Temperature

	9-pF internal C_L	**Minimum internal C_L**
Frequency variation –40°C to +90°C	Set by crystal	Set by crystal + 5 ppm
Voltage accuracy, ppm/V	6.9	9

The following presents the relative advantages of crystals with different C_L values.

The disadvantages of lower C_L are as follows:

- Crystals with < 7-pF C_L are more difficult to source with short lead times.
- Frequency becomes more sensitive to changes in board capacitance as C_L decreases. It is possible to meet frequency stability specifications with a C_L as low as 3 pF.
- Lowering C_L results in degraded RF phase noise.

Advantages of lower C_L are as follows:

- Lower C_L causes a much faster start-up time. (Start-up time goes as $\infty\left(\frac{1}{C_L^2}\right)$)
- Lower C_L causes a faster amplitude control loop response time.
- Lower C_L makes it easier to use small size crystals (2.0 × 1.6 and so on) and maintain a start-up time at or less than 400 µs. Start-up time worsens with smaller crystals due to an increase in L_M.

5.4 ESR and Start-Up Time

ESR (equivalent series resistance) is a parameter of the crystal in the data sheet of the crystal. Negative resistance is a parameter of the complete oscillator circuit, including capacitor values, crystal parameters, and an on-chip circuit. To ensure best start-up of the crystal oscillator, the negative resistance magnitude must be at least 5 times greater than R_N (see Equation 11 and Equation 12) during initial start up but can be 2 to 3 times greater when the crystal has reached steady state.

$$\text{ESR} < \frac{|R_N|}{5} \tag{11}$$

$$R_N = \frac{-g_m}{(2\pi f)^2 (2C_L)^2} \tag{12}$$

If the negative resistance magnitude is not 5× greater than R_N during initial start-up, the oscillator might not operate optimally or might fail to start. An increasing negative resistance magnitude leads to a faster the start-up time of the oscillator.

NOTE: Crystals with higher ESR typically result in longer start-up times than crystals with lower ESR. An higher-load capacitance decreases the negative resistance of the oscillator and increases the start-up time.

5.5 Drive Level and Power Consumption

The maximum drive level of a crystal is often specified in the data sheet of the crystal in µW. Exceeding this value can damage or reduce the lifetime the crystal. The CC26xx and CC13xx devices drive the crystal with a maximum 1.6 V_{pp} for the 24-MHz crystal and 600 mV_{pp} for the 32.768-kHz crystal. As Section 3.2.3 explains, Equation 13 gives the drive level in W.

$$DL = ESR(\pi f (C_L + C_M) V_{pp})^2 \tag{13}$$

As in Equation 13 of the drive level, a higher total capacitance load and ESR require more power to drive the crystal, increasing the power consumption of the oscillator. Because the 32.768-kHz crystal is on for an extended period of time, this increase is important. Selecting a low ESR and low-C_L 32.768-kHz crystal is important to achieve low-power consumption in a low-power mode.

NOTE: Do not use the internal DC-DC when applying a probe to the 24-MHz crystal oscillator pins. Applying the probe can lead to the oscillator stopping and may lead to the internal DC-DC producing a high-output voltage that may damage the device.

5.6 Crystal Package Size

There are several different packages for crystals. The available board space and cost determines the package size used. Crystals with smaller packages have a higher ESR and motional inductance. These smaller packages cause a longer start-up time of the crystal oscillator. By choosing a crystal with a low C_L if a smaller package is required, this start-up time increase can be compensated.

6 PCB Layout of the Crystal

The layout of the crystal can reduce the parasitic capacitance and, more importantly, reduce noise from coupling on the input of the oscillators. Noise on the input of the oscillator can lead to severe side effects such as clock glitches, flash corruption, or system crashes because the CC26xx and CC13xx devices rely on the crystal oscillators as the high- and low-frequency system clock.

The following are a few recommendations for the layout of the crystals:

- Place the crystal as close as possible to the device to minimize the length of the PCB traces. (This placement reduces crosstalk and minimizes EMI.)
- TI recommends a solid ground plane under the crystal.
- Ensure no high-speed digital signals are close to the crystal to minimize cross-coupling of noise into the oscillator.

Figure 6 shows the top layer of the layout of the CC26xx reference design. The bottom layer is a solid ground plane. For more details, see *SimpleLink™ CC2650 EVM Kit 4XD (CC2650EM-4XD) v1.0.3 Design Files*. The same crystal layout can be used with CC13xx device.

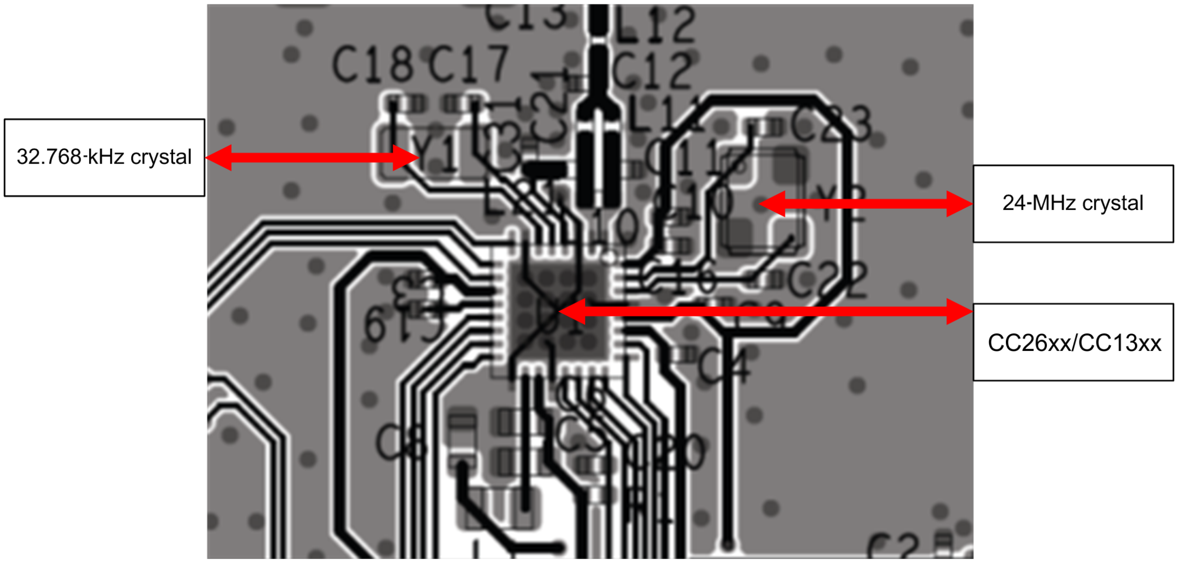

Figure 6. Layout of the CC26xx EVM

7 Configuring the CC26xx or CC13xx for Different Crystals

You must set the internal load capacitor to tune the frequency of the 24-MHz oscillator. The capacitor array can also be disabled and in this case the external loading capacitors are required. If using the TI BLE stack, you must also specify the tolerance of the 32.768-kHz clock to the BLE stack.

7.1 Internal Capacitor Array

The internal capacitor of the 24-MHz crystal oscillator can be adjusted. Equation 14 gives the total internal loading capacitance.

$$C_{L\_int} = 9 + C_{delta} \left(pF\right) \tag{14}$$

The value of C_{delta} is set in customer configuration area in the flash memory of the CC26xx/CC13xx. For more details, see the *CC13xx, CC26xx Technical Reference Manual*. The capacitance of the array can vary up to 8% from device to device and over operating conditions. Modify the oscillator CCFG.c file by performing the following steps:

1. Enable the cap-array delta (C_{delta}) (see the following code).

```
//*****************************************************
// Enable XOSC cap-array delta
//*****************************************************
#define SET_CCFG_MODE_CONF_XOSC_CAP_MOD              0x0        // Apply cap-array delta
// #define SET_CCFG_MODE_CONF_XOSC_CAP_MOD           0x1        // Don't apply cap-array delta
```

2. Set the value of the C_{delta}.

```
//*****************************************************
// Value of XOSC cap-array delta
//*****************************************************
#define SET_CCFG_MODE_CONF_XOSC_CAPARRAY_DELTA          0xFF       // Signed 8-bit value,
directly modifying trimmed XOSC cap-array value
```

Table 3 is a table with C_{L_int} for different settings of the SET_CCFG_MODE_CONF_XOSC_CAPARRAY_DELTA measure in the *SimpleLink™ CC2650 EVM Kit 4XD (CC2650EM-4XD) v1.0.3 Design Files*.

Table 3. Impact of SET_CCFG_MODE_CONF_XOSC_CAPARRAY_DELTA on Crystal Load Capacitance

SET_CCFG_MODE_CONF_XOSC_CAPARRAY_DELTA Value	C_{L_int}	SET_CCFG_MODE_CONF_XOSC_CAPARRAY_DELTA Value	C_{L_int}	SET_CCFG_MODE_CONF_XOSC_CAPARRAY_DELTA Value	C_{L_int}	SET_CCFG_MODE_CONF_XOSC_CAPARRAY_DELTA Value	C_{L_int}
–27	5	–17	6.2	–7	7.7	3	9.6
–26	5.1	–16	6.4	–6	7.7	4	9.8
–25	5.2	–15	6.5	–5	7.9	5	10.1
–24	5.3	–14	6.7	–4	8.2	6	10.3
–23	5.3	–13	6.8	–3	8.4	7	10.5
–22	5.5	–12	7	–2	8.6	8	10.7
–21	5.6	–11	7.1	–1	8.8	9	10.9
–20	5.8	–10	7.3	0	9	10	11.1
–19	5.9	–9	7.4	1	9.2		
–18	6.1	–8	7.6	2	9.4		

After configuring C_{delta}, the value of the DDI_0_OSC ANABYPASSVALUE1 register should match the required capacitance. To use a 6-pF crystal, set the value of SET_CCFG_MODE_CONF_XOSC_CAPARRAY_DELTA to –18.

7.2 Set the Sleep Clock Accuracy in the BLE Stack

The 32.768-kHz clock is typically used as the low-frequency system clock in low-power mode, especially when it is used in an application that relies on a time-synchronized network (for example, Bluetooth low energy). In a time-synchronized network, a more accurate clock enables a later wake up of the device to start listening or sending radio packets and not to miss radio events.

In the BLE stack from TI, you can set the accuracy of the 32.768-kHz clock to optimize the power consumption. By default, the accuracy is set to 40 ppm; you must adjust the accuracy to avoid missing radio events or waking up the device from a low-power mode earlier than necessary. The sleep clock accuracy is set in the BLE stack with the following HCI command:

HCI_EXT_SetSCACmd(40); //Default 40ppm

```
/*******************************************************************************
 * @fn          HCI_EXT_SetSCACmd
 *
 * @brief       This API is used to set this device's Sleep Clock Accuracy.
 *
 *              Note: For a slave device, this value is directly used, but only
 *                    if power management is enabled. For a master device, this
 *                    value is converted into one of eight ordinal values
 *                    representing a SCA range, as specified in Table 2.2,
 *                    Vol. 6, Part B, Section 2.3.3.1 of the Core specification.
 *
 *              Note: This command is only allowed when the device is not in a
 *                    connection.
 *
 *              Note: The device's SCA value remains unaffected by a HCI_Reset.
 *
 * input parameters
 *
 * @param       scaInPPM - A SCA value in PPM from 0..500.
 *
 * output parameters
 *
 * @param       None.
 *
 * @return      hciStatus_t
 */
extern hciStatus_t HCI_EXT_SetSCACmd( uint16 scaInPPM );
```

8 Measuring the Amplitude of the Oscillations of Your Crystal

Two functions exist in CC26XX/13XXWARE for measuring the amplitude of the oscillations of the crystal, and comparing this amplitude to the expected amplitude. These functions are as follows:

- uint32_t OSCHF_DebugGetCrystalAmplitude(void);
- uint32_t OSCHF_DebugGetExpectedAvarageCrystalAmplitude(void);

The first function inserted into a piece of code returns the amplitude of the crystal in mV. The second function returns the expected oscillation amplitude, also in mV. These are debug functions only. The first function uses an on-chip ADC to measure the amplitude of the crystal. If these functions return greatly different values, the crystal may have a problem. The uncertainty of the first function is ± 50 mV; a 50 mV deviation from the expected value is not cause for concern.

8.1 Measuring Start-Up Time to Determine HPMRAMP1_TH and XOSC_HF_FAST_START

The following code can be used to estimate the start-up time of the 24-MHz crystal. The code counts the edges of the 32.768-kHz crystal before the 24-MHz crystal is operational. For more accurate results, external measurement equipment is required.

```
//MeasureStartup()
//Returns the startup time as 65536 * number of 1/2 LF clock cycles elapsed during startup
//To get result in seconds divide this number by 2^32
//Must have these includes:
//#include <driverlib/osc.h>
//#include <driverlib/aon_ioc.h>
//Must initialize I/Os before running this routine: e.g. PIN_init(BoardGpioInitTable);
//This function may not work correctly if compiler optimizations are turned on
uint32_t MeasureStartup(){
    uint32_t Count = 0;
    uint32_t PollCount = 0;
    uint32_t PrevPollCount=0;
    uint32_t State = 0;
    uint32_t PrevState = 0;

    //Route SCLK_LF to DIO24, with DIO24 configured as input.
    AONIOC32kHzOutputEnable();
    HWREG(IOC_BASE+IOC_O_IOCFG24) = 0x20006307;
    //Enable IOC input, connect DIO 24 to SCLK_LF

    if (OSCClockSourceGet(OSC_SRC_CLK_HF) != OSC_RCOSC_HF) {
            OSCClockSourceSet(OSC_SRC_CLK_HF, OSC_RCOSC_HF);
            while (!OSCHfSourceReady());
            OSCHfSourceSwitch();
 }

    // Set XOSC_LF as SCLK_LF source
    OSCClockSourceSet(OSC_SRC_CLK_LF, OSC_XOSC_LF);
    //wait forever for SCLK_LF to be sourced from XOSC_LF

while((HWREG(AUX_DDI0_OSC_BASE+DDI_0_OSC_O_STAT0)&DDI_0_OSC_STAT0_SCLK_LF_SRC_XOSCLF)!=DDI_0_OSC_S
TAT0_SCLK_LF_SRC_XOSCLF) {};

    State = HWREG(GPIO_BASE+GPIO_O_DIN31_0)&GPIO_DIO_24_MASK;
    PrevState=State;
    while(State != 0 && PrevState !=GPIO_DIO_24_MASK )//Wait for negedge of XOSC_LF
    {
        PrevState=State;
        State = HWREG(GPIO_BASE+GPIO_O_DIN31_0)GPIO_DIO_24_MASK;
    }

    PrevState=0;
    OSCHF_TurnOnXosc();
```

```
while
((HWREG(AUX_DDI0_OSC_BASE+DDI_0_OSC_O_STAT0)&DDI_0_OSC_STAT0_PENDINGSCLKHFSWITCHING)!=DDI_0_OSC_ST
AT0_PENDINGSCLKHFSWITCHING)
    {//wait for pending bit
        State = HWREG(GPIO_BASE+GPIO_O_DIN31_0)&GPIO_DIO_24_MASK;

        PollCount=PollCount+1;//This counts number of polling cycles
        if(State!=PrevState)//This increments on every edge of XOSC_LF
        {
            Count=Count+1;//increase the count of detected XOSC_LF edges. This occurs at a rate
of 2 x freq of XOSC_LF
            PrevPollCount=PollCount;
            PollCount=0;
        }
        PrevState=State;

    }
    return 65536*Count+(65536*PollCount)/PrevPollCount;
    //(65536*PollCount)/PrevPollCount is to get the fractional part of XOSC_LF cycles remaining
uncounted by Count


}
```

Figure 7 is an example plot generated with this code across temperature.

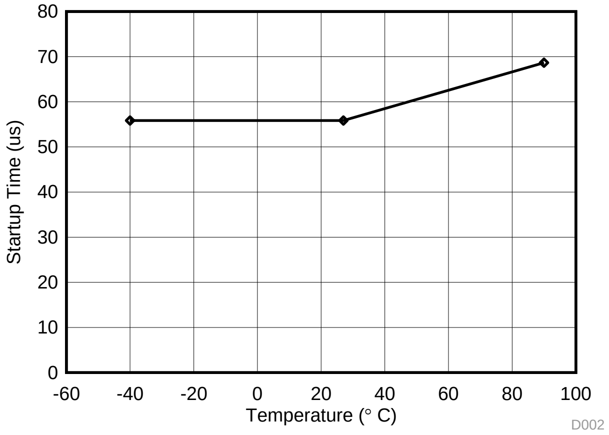

Figure 7. Example Start-Up Time Plot

9 Crystals for CC26xx and CC13xx

Tables giving appropriate crystals for use with the CC26xx and CC13xx devices can be found at this website: http://processors.wiki.ti.com/index.php/CC26xx_Crystals.

10 References

1. *Part 15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs), 802.15.4-2006*, http://standards.ieee.org/getieee802/download/802.15.4-2006.pdf
2. *Bluetooth Core Specifications, Version 4.2*, https://www.bluetooth.org/en-us/specification/adopted-specifications
3. *CC2650 SimpleLink™ Multistandard Wireless MCU*
4. *CC26xx Crystals TI wiki*
5. *SimpleLink™ CC2650 EVM Kit 4XD (CC2650EM-4XD) v1.0.3 Design Files*
6. *CC13xx, CC26xx SimpleLink Wireless MCU Technical Reference Manual*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from D Revision (April 2016) to E Revision	Page
• Changed Section 8.1	16

Changes from C Revision (March 2016) to D Revision	Page
• Removed 24-MHz Crystals Usable With CC26xx/CC13xx table.	17
• Removed 32.768-kHz Crystals Usable With CC26xx/CC13xx table.	17

Changes from B Revision (February 2016) to C Revision	Page
• Updated Crystal Parameters Table.	6
• Updated 32.768-kHz Crystals Usable With CC26xx/CC12xx table.	17

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