InGenius High-CMRR Balanced Input Line Receiver ICs

TT1200 Series

FEATURES

- High CMRR: typ. 90 dB at 60 Hz
- Extremely high common-mode input impedance
  - Maintains balance under real-world conditions
- Transformer-like performance in an IC
- Excellent performance
  - Wide bandwidth: typ. > 22 MHz
  - High slew rate: typ. 12 V/us
  - Low distortion: typ. 0.0005 % THD
  - Low noise: typ. -107 dBu
- Several gains: 0 dB, -3 dB, & -6 dB

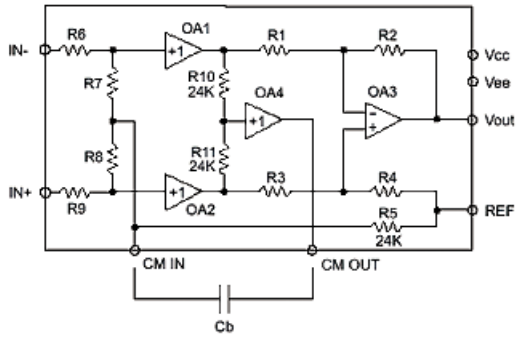
APPLICATIONS

- Balanced Audio Line Receivers
- Instrumentation Amplifiers
- Differential Amplifiers Expanders
- Transformer Front-End Replacements
- ADC Front-Ends

Description

The TT Semiconductor TT1200-series InGenius balanced line receivers overcome a serious limitation of conventional balanced input stages: poor common mode rejection in real-world applications. While conventional input stages measure well in the lab and perform well on paper, they fail to live up to their CMRR specs when fed from even slightly unbalanced source impedances. This is because conventional stages have low common-mode input impedance, which interacts with imbalances in source impedance to unbalance common-mode signals, making them indistinguishable from desired, balanced signals.

The patented InGenius input stage uses clever bootstrapping to raise its common-mode input impedance into the meg-ohm range without the noise penalty from the obvious solution of using high-valued resistors. Like transformers, InGenius line receivers maintain their high CMRR over a wide range of source impedance imbalances — even when fed from single-ended sources. These wide bandwidth solid state devices offer dc-coupling, low distortion, and lower signal noise that is not achievable with transformers.



Part no.	R6, R9	R7, R8	R1, R3	R2, R4
TT1200	0	24 kΩ	6 kΩ	6 kΩ
TT1203	7 kΩ	17 kΩ	6 kΩ	6 kΩ
TT1206	7 kΩ	17 kΩ	7 kΩ	5 kΩ

Figure 1. TT1200 series equivalent circuit diagram

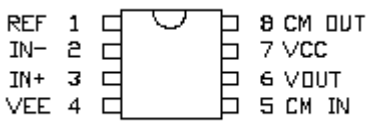


Figure 2. DIP Pinout Assignments

TT Semiconductor; 325 North Shepard Street; Anaheim, California 92806; USA
Tel: 1 714 257 2257; Fax: 1 714 257 2252; Web: www.ttsemiconductor.com

SPECIFICATIONS[1]

Absolute Maximum Ratings (T_A = 25°C)

Positive Supply Voltage (V_{CC})	+20 V	Operating Temperature Range (T_{OP})	-55 to +175°C
Negative Supply Voltage (V_{EE})	-20 V	Output Short-Circuit Duration (t_{SH})	Continuous
Storage Temperature Range (T_{ST})	-55 to +200°C		

	TT1200	**TT1203**	**TT1206**
Input Voltage (V_{IN})	25 V	31 V	31 V

Electrical Characteristics[2,3,4]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current	I_{CC}	No signal	—	4.7	8.0	mA
Supply Voltage	V_{CC},V_{EE}		3	—	18	V
Input Bias Current	I_B	no signal; Either input connected to GND	—	700	1,400	nA
Input Offset Current	I_{B-OFF}	No signal	—	—	300	nA
Input Voltage Range	V_{IN-CM}	Common mode	12.5	13.0	—	V
	$V_{IN-DIFF}$	Differential (equal and opposite swing)				
		TT1200	21.0	21.5	—	dBu
		TT1203	24.0	24.5	—	dBu
		TT1206	24.0	24.5	—	dBu
Input Impedance	$Z_{IN-DIFF}$	Differential		48.0		k ohm
	Z_{IN-CM}	Common mode		with bootstrap		
		60 Hz		10.0		M ohm
		20 kHz		3.2		M ohm
Common Mode Rejection Ratio	$CMRR_1$	Matched source impedances; V_{CM} = ±10V				
		DC	70	90	—	dB
		60 Hz	70	90	—	dB
		20 kHz	—	85	—	dB
Common Mode Rejection Ratio[5]	$CMRR_{IEC}$	10 unmatched source imped-ances; V_{CM} = ±10V				
		DC	—	90	—	dB
		60 Hz	—	90	—	dB
		20 kHz	—	85	—	dB
Common Mode Rejection Ratio	$CMRR_2$	600 unmatched source impedances; V_{CM} = ±10V				
		60 Hz	—	70	—	dB
		20 kHz	—	65	—	dB
Power Supply Rejection Ratio[6]	PSRR	At 60 Hz, with V_{CC} =-V_{EE}				
		TT1200	—	82	—	dB
		TT1203	—	80	—	dB
		TT1206	—	80	—	dB

1. All specifications subject to change without notice.
2. Unless otherwise noted, T_A=-55°C to +125 C, V_{CC} = +15V, V_{EE}= -15V
3. See test circuit in Figure 2.
4. 0 dBu = 0.775Vrms.
5. Per IEC Standard 60268-3 for testing CMRR of balanced inputs.
6. Defined with respect to the differential gain.

TT Semiconductor; 325 North Shepard Street; Anaheim, California 92806; USA
Tel: 1 714 257 2257; Fax: 1 714 257 2252; Web: www.ttsemiconductor.com

Electrical Characteristics (Cont'd)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Total Harmonic Distortion	THD	$V_{IN-DIFF}$ = 10 dBu; BW = 20 kHz;f =1 kHz				
		R_L =2 k	—	0.0005	—	%
Output Noise	$e_{n(OUT)}$	BW =20 kHz				
		TT1200	—	-106	—	dBu
		TT1203	—	-105	—	dBu
		TT1206	—	-107	—	dBu
Output Offset Voltage	V_{OFF}	No signal	—	—	10	mV
Slew Rate	SR	R_L = 2 k , C_L = 300 pF	6	12	—	V/ s
Small Signal Bandwidth	BW_{-3dB}	R_L = 10 k , C_L = 10 pF				
		TT1200	—	22	—	MHz
		TT1203	—	27	—	MHz
		TT1206	—	34	—	MHz
Output Gain Error	$G_{ER(OUT)}$	f = 1 kHz; R_L = 2 k	—	0	0.05	dB
Maximum Output Voltage	V_O	At max differential input				
		TT1200	20.5	21.5	—	dBu
		TT1203	20.5	21.5	—	dBu
		TT1206	17.5	18.5	—	dBu
Output Short Circuit Current	I_{SC}	R_L = R_{Lcm} = 0	—	25	—	mA
	I_{CMSC}	At CM output	—	10	—	mA
Minimum Resistive Load	R_{Lmin}		2	—	—	k
	R_{LCMmin}	At CM output	10	—	—	k
Maximum Capacitive Load	C_{Lmax}		—	—	300	pF
	C_{LCMmax}	At CM output	—	—	50	pF

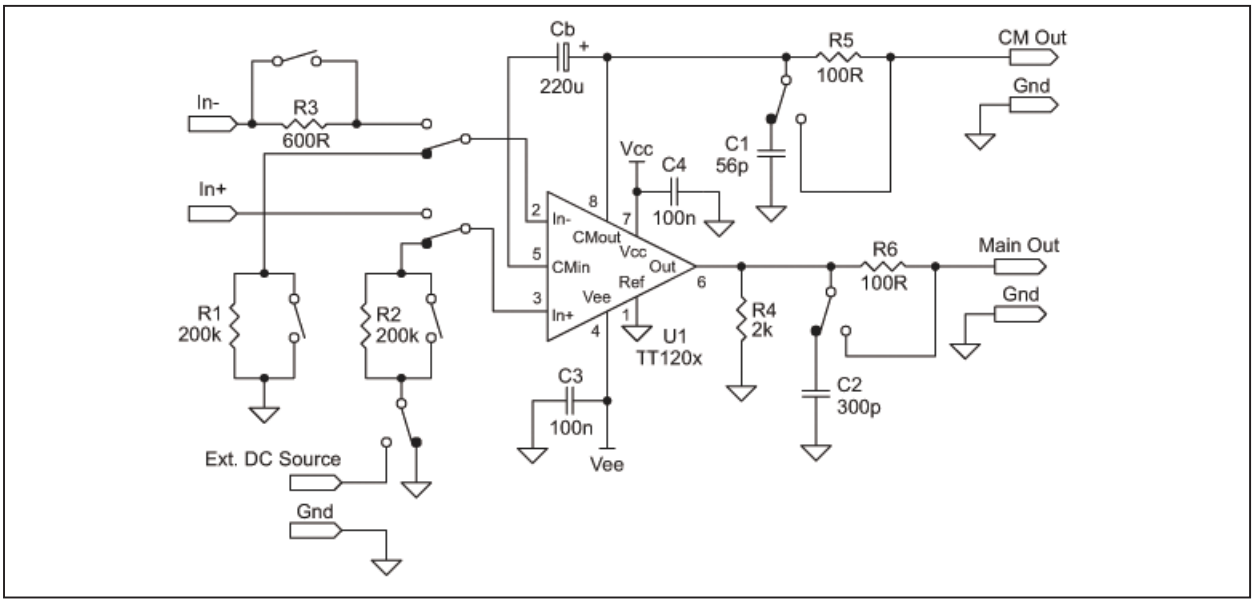


Figure 3. TT1200 series test circuit

TT Semiconductor; 325 North Shepard Street; Anaheim, California 92806; USA
Tel: 1 714 257 2257; Fax: 1 714 257 2252; Web: www.ttsemiconductor.com

Theory of Operation

The InGenius concept was invented to overcome limitations of traditional approaches to active input stage design. Because of the many misconceptions about the performance of conventional input stages, and to set the stage for discussion of InGenius, we will begin by discussing conventional approaches.

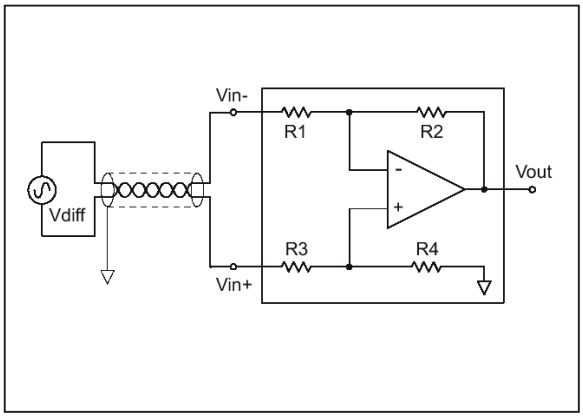


Figure 4. Basic differential amplifier

Traditional Balanced Input Stages

The typical balanced input stage used in most professional audio products is shown in figure 4. It amplifies differential signals but rejects common-mode interference based on the precision of the match in the ratios R_2/R_1 and R_4/R_3 . In this circuit,

$$V_{out} = (V_{in+})(1+\frac{R_2}{R_1})\frac{R_4}{(R_3+R_4)} + (V_{in-})\frac{R_2}{R_1}$$

In modern integrated circuits (such as the TT1240 series), these resistor ratios are trimmed (usually with a laser) to extreme precision, resulting in typical match of 0.005%. So, one can assume that $R_2/R_1 = R_4/R_3$. In this case, we can simplify this formula as follows:

$$V_{out} = (V_{in+})(1+\frac{R_2}{R_1})(\frac{R_2}{R_1})\frac{1}{(1+\frac{R_2}{R_1})} + (V_{in-})\frac{R_2}{R_1}$$

yielding:

$$V_{out} = \left[(V_{in+}) + (V_{in-})\right]\frac{R_2}{R_1}$$

CMRR Depends on Resistor Match

When driven from a theoretical, true voltage source, the precisely matched resistor ratios deliver extremely high CMRR. With perfectly matched resistor ratios, for $V_{in+} = -V_{in-}$ (this corresponds to a pure differential input signal), then V out $= 2*(V_{in+})*R_2/R_1$. On the other hand, for $V_{in+} = V_{in-}$ (this corresponds to a pure common mode signal), then $V_{out} = 0$. This produces an infinite common mode rejection ratio. Any difference between the ratios R_2/R_1 and R_4/R_3 will lead to less than perfect CMRR.

The Impact of Driving Source Impedance

However, in the real world, where sources have non-zero output impedance, the situation is more complicated. Figure 5 shows the equivalent circuit of a real-world differential application. In this case, the source connected to the differential receiver has source impedance of R_{s+} in the positive side, and R_{s-} in the negative side. Because these two resistive elements are in series with each other, they only serve to attenuate the signal Vdiff relative to the input impedance of the differential stage. Even if they (R_{s+} and R_{s-}) are mismatched, this attenuation is the only consequence of non-zero source impedance.

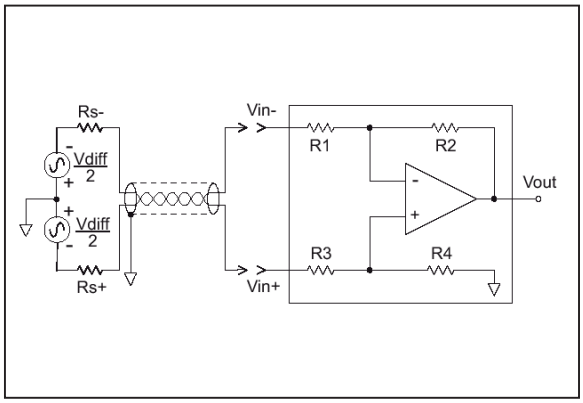


Figure 5. Basic differential amplifier showing mismatched source impedances

However, the same cannot be said for common-mode interference. Common-mode signals appear in phase between the two input terminals. For in-phase signals, the source impedances can have significant impact. As shown in Figure 6, this is because each leg of the source impedance forms a voltage divider when it interacts with the input impedance of its respective input of the differential amplifier.

Because the + and - inputs of the operational amplifier are forced by feedback to maintain the same voltage, the individual common-mode impedances of each side of the differential stage are:

$$Z_{CM+} = R_3 + R_4 \text{ ; and}$$

$$Z_{CM-} = \frac{R_3+R_4}{\frac{R_3}{R_1}} .$$

TT Semiconductor; 325 North Shepard Street; Anaheim, California 92806; USA
Tel: 1 714 257 2257; Fax: 1 714 257 2252; Web: www.ttsemiconductor.com

So long as $R_1=R_3$, these impedances, which form a load for common-mode input signals, are identical. (This is why, in discrete applications, it is wise to choose $R_1 =R_3$ and why, in all integrated applications, these resistors are chosen to be the same value.)

The total common-mode input impedance is

$$Z_{CM} = \frac{R_3+R_4}{1+\frac{R_3}{R_1}} .$$

Source Impedance Mismatches Ruin Good CMRR

Even if R_1 perfectly matches R_3 , any mismatch in the source impedances R_{S+} and R_{S-} will cause then voltage dividers to be unequal between the two input legs. This means that V_{in-} and V_{in+} in Figure 6 are no longer equal to each other. Essentially, imbalances in the two source impedances convert the common mode signal to a differential signal, which will not be rejected by the input stage no matter how high its theoretical CMRR is.

To see how this plays out in practice, consider the case of a typical unity-gain conventional balanced line receiver with common-mode input impedance of 10 k In such cases, a source impedance imbalance of only 10 can degrade CMRR to no better than 66 dB. A 10 mismatch could be caused by tolerances in coupling capacitors or output build-out resistors. The situation becomes much worse when a conventional balanced line receiver is driven from an unbalanced source, where it is common to use at least 100 in series with the output for protection. (With a 100 unbalanced output impedance, and a 10 k common-mode input impedance, even a perfect simple input stage can provide no more than 46 dB CMRR!)

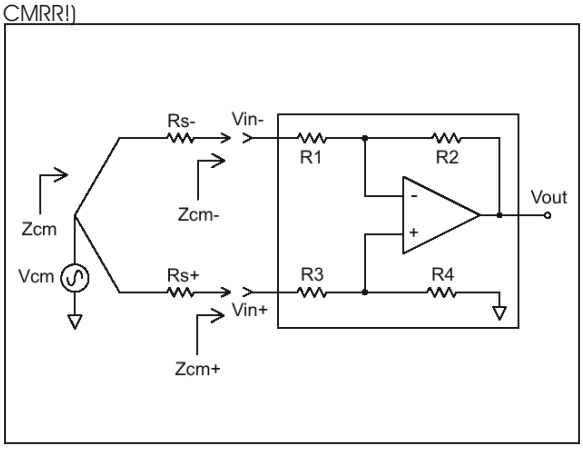


Figure 6. Basic differential amplifier driven by common-mode input signal

The best solution to this problem is to increase the line receiver's common-mode input impedance enough to minimize the unbalancing effect of the voltage divider. Preferably, this means achieving input impedances on the order of several megohms. However, in a conventional differential amplifier, this requires high-value resistances in the circuit. High resistance carries with it a high noise penalty, making this straightforward approach impractical for quality audio devices.

Instrumentation Amplifiers

Some designers prefer the more elaborate approach of an instrumentation amplifier, as shown in Figure 7. In this circuit, it is possible to raise the input impedance (both common-mode and differential) of the stage because the load seen by the source is decoupled by OA_1 and OA_2 from the balanced stage (OA_3 along with R_1, R_2, R_3 , and R_4). In this circuit, $Z_{CM-} = R_{i1}$, and $Z_{CM+} = R_{i2}$.

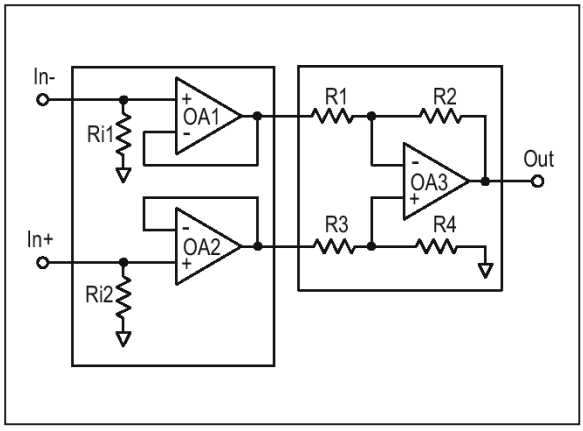


Figure 7. Instrumentation amplifier

To retain 90 dB CMRR in the face of a 10 mismatch in source impedance would require R_{i1} and R_{i2} to be > 317 k .Of course, any difference in the values of R_{i1} and R_{i2} themselves would further unbalance common mode signals as well, so these resistors would ideally be trimmed just like the resistors in the single opamp stage of Figure 4. Unfortunately for this approach, it is difficult and expensive to make precision trimmed resistors with such high values.

Furthermore, since the input bias current for amplifiers OA_1 and OA_2 flows through these resistors, their input currents must be extremely low if they are not to cause significant offsets. Practically, this necessitates using FET input stages for OA_1 and OA_2. While FETs may be a viable alternative, it is difficult to achieve with them

TT Semiconductor; 325 North Shepard Street; Anaheim, California 92806; USA
Tel: 1 714 257 2257; Fax: 1 714 257 2252; Web: www.ttsemiconductor.com

the low noise performance of modern bipolar input stages.

Transformer Input Stages

From the point of view of common mode input impedance, as well as that of electrical isolation, a transformer in front of the first active input stage is really the best possible solution. Transformers are the only approach of which we are aware that provides true electrical isolation with reasonable fidelity. Furthermore, their common-mode input impedance is easily extremely high (tens of Megohms), and almost completely decoupled from their differential input impedance.

But, transformers have many other limitations. They do not offer dc coupling, and suffer from saturation at low frequencies unless they are physically large and carefully made. Again, unless they are carefully made (which usually equates to high cost), they introduce phase shift at high audio-band frequencies. Furthermore, they tend to be big and heavy and pick up external magnetic fields, sometimes making it difficult to locate transformer-coupled equipment to avoid interference.

Fortunately, audio equipment usually does not require true electrical isolation. In most cases, transformers out-perform conventional input stages only because they excel at rejecting common-mode signals in real-world situations. It is no coincidence that the InGenius concept was developed by an individual responsible for manufacturing the world's premier line of audio transformers (Bill Whitlock, of Jensen Transformers). Bill's InGenius technology offers all the advantages of solid state input stages, including dc coupling, negligible phase shift from dc to beyond the edge of the audio band, and vanishingly low distortion, along with the primary advantage of a transformer: extremely high common-mode input impedance.

The InGenius Approach

The InGenius approach to balanced line receivers uses bootstrapping to increase common mode input impedance. With bootstrapping, we first create a replica of the common mode signal, and then feed it back appropriately to the inputs to increase the input impedance. Because doing this in a differential amplifier involves additional complications, it is useful to review the bootstrap concept with a single-ended design first. We will then show how Bill Whitlock applied that concept to the differential case.

Bootstrapping: a Simple Single-Ended Example

To illustrate the concept behind bootstrapping, consider the single-ended bootstrap shown in Figure 8. In this circuit, amplifier A is configured for unity gain, and can be considered to have infinite input impedance. Capacitor C_b blocks DC, so at DC, the input impedance, Z_{in} ,is $R_a + R_b$.

However, for high-frequency AC signals (where C_b is effectively a short), amplifier A drives the junction of R_a and R_b through C_b to nearly the same AC voltage as V_{in}. As a result, practically no AC current flows through R_a. This effectively increases the input impedance seen at Z_{in}.

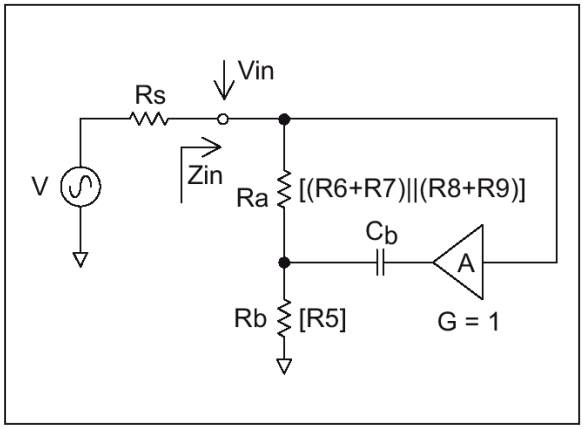


Figure 8. Single-ended bootstrap topology

The cutoff frequency of the filter formed by C_b and R_a /R_b is determined primarily by the values of C_b and R_b. (Because so little current flows in R_a,it is hardly involved in this filter.)

Input impedance Z_{in} ; at frequency f, is described the following equation:

$$Z_{in} = (R_a + R_b)\sqrt{\frac{1+(\frac{f}{f_n})^2}{1+(1-G)^2(\frac{f}{f_D})^2}}$$

where

$$f_n = \frac{1}{2\pi(\frac{R_a \cdot R_b}{R_a + R_b}) \cdot C_b}$$

$$f_D = \frac{1}{2\pi R_b C_b}$$

For example, if R_a and R_b are 10 k each, Z_{inDC} is 20 k .This resistance provides a DC path for amplifier bias current. At higher frequencies, the bootstrap greatly increases the input impedance, limited ultimately by how close gain G approaches unity.

Common Mode Bootstrapping in an Instrumentation Amplifier = InGenius

The genius behind Bill Whitlock's invention was to recognize that in an instrumentation amplifier, it is possible to bootstrap the common-mode signal to

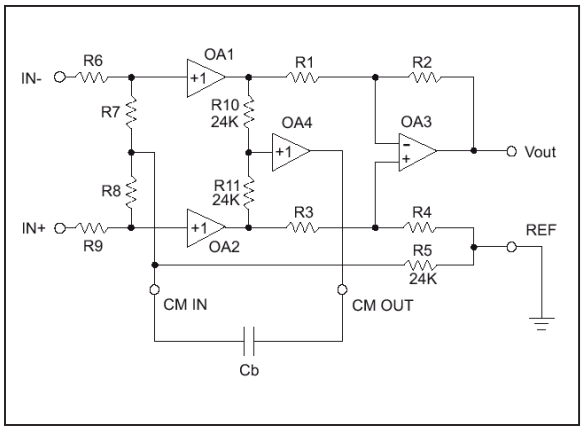


Figure 9. TT1200-series equivalent circuit diagram

increase common-mode input impedance. This is the concept behind the InGenius patents. To see how this works, refer to the circuit of Figure 9.

Like Figure 1, Figure 9 shows an equivalent circuit for the TT Semiconductor's TT1200-series ICs. OA_1 and OA_2 are high input-impedance, unity-gain buffers feeding differential amplifier OA_3 in an instrumentation amplifier configuration. OA_4 is a third high input-impedance, unity-gain buffer. With $R_{10} = R_{11}$, the voltage at the input to OA_4 will be equal to the common-mode component of the input signal. OA_4 buffers this signal, and feeds it back to both inputs via capacitor C_b and resistors R_6,R_7,R_8 ,R_9 , and R_5 . Note that in most applications C_b is large (>100 f).

Similarly to the single-ended application above, at high frequencies, the junction of R_7, R_8, and R_5 is driven through C_b to the same potential as the common-mode input voltage. Hence at high frequencies, no common-mode current flows in resistors R_6 and R_7 ,or R_8 and R_9. Since OA_1 and OA_2 have high input impedances, this effectively raises the input impedance seen at In+ and In- to high-frequency common- mode signals. Of course, for differential signals, the input impedance is (R_6 +R_7 +R_8 +R_9). And, at DC, the common-mode input impedance is:

$$Z_{CM_{DC}} = \frac{(R_6 + R_7)(R_8 + R_9)}{R_6 + R_7 + R_8 + R_9} + R5.$$

DC bias for OA_1 and OA_2 is supplied through R_5 and either R_7 or R_8.

For the resistor values chosen for the TT1200-series ICs, the input impedances Z_{CM} and Z_{diff} , are described by the following equations:

$$Z_{CM_{DC}} = 36\ k\Omega$$

$$Z_{CM}(f) = 36\ k\Omega \sqrt{\frac{1+(50240 \cdot C_b \cdot f)^2}{1+(73.8 \cdot C_b \cdot f)^2}}$$

where f is the input frequency,

$$Z_{diff} = R_6 + R_7 + R_8 + R_9 = 48\ k\Omega$$

In order to get the most out of this topology, OA_1 and OA_2 must have high input impedance, and the common-mode gain loop (OA_1 ,OA_2 ,R_{10} /R_{11} and OA_4) must have precisely unity gain over the entire audio band. TT Semiconductor integrated the InGenius parts using a dielectric isolation process because it offers very high bandwidth and low noise for relatively high-voltage applications like this one. This in turn makes it easier to meet these requirements, and typically, results in a maximum mid-audio-band Z_{inCM} of >20 M .

Because OA_1 and OA_2 isolate the differential amplifier (OA_3) from the effects of external source impedances, the CMRR of OA_3 and its associated four resistors is determined solely by OA_3's bandwidth and the precision of the resistor matching. The complimentary DI process contributes to high bandwidth in OA_3 , and on-chip laser trimming of the four thin film resistors to ensure extremely good matching, as well as precise gain.

Finally, perhaps the most common interfering signals that a good differential line receiver must reject is the power-line frequency: usually either 50 or 60 Hz and its harmonics. So, it is essential that the common-mode input impedance remain high down to 50 Hz, and up to at least to the edge of the audio band. While Twilight Technology's process and circuit design ensure the latter condition, the value of C_b will determine how low in frequency the common-mode input impedance will be increased. To maintain at least a 1 common-mode input impedance, C_b should be at least 10 f.

It is possible to solve the above equation for C_b in terms of the desired Z_{CM} for a specific frequency. However, reaching a general closed-form solution is difficult and results in a very complex formula. The relatively simple formula below takes advantage of some approximation, and yields good results for Z_{CM} between about 100 k and 10 M .

$$C_b \cong 0.553 \times 10^{-3} \frac{Z_{CM}}{f}$$

TT Semiconductor; 325 North Shepard Street; Anaheim, California 92806; USA
Tel: 1 714 257 2257; Fax: 1 714 257 2252; Web: www.ttsemiconductor.com

Applications

Basic Application

At its most basic, Twilight Technology's TT1200-series ICs need very little external support circuitry. As is shown in the basic application circuit of Figure 10, they need little else beyond positive and negative power supplies, a ground reference, the common-mode bootstrap capacitor, and input and output connections. Because all TT1200-series ICs are wide bandwidth parts, it is important to provide bypass capacitors for both positive and negative supply rails within an inch or so of the part. Sharing supply bypass capacitors across several TT1200-series ICs separated by several inches on a circuit board (as, for example, along the back panel of a multi-input product) is not recommended[1].

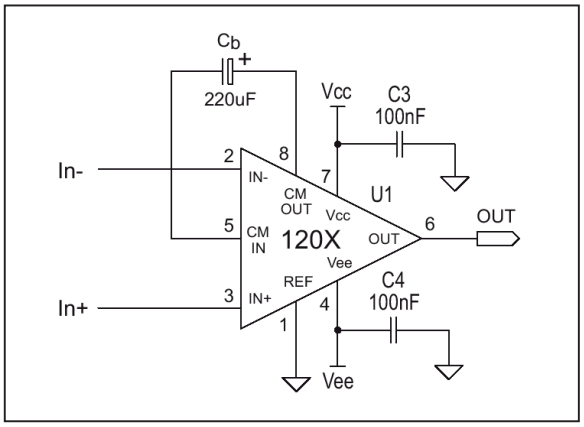


Figure 10. Basic TT1200-series application circuit

Bootstrap Capacitor Polarity

Because the bootstrap capacitor, C_b , will usually be large (see formula on page 7) an electrolytic or tantalum capacitor is a logical choice. Such capacitors are normally polarized, though non-polarized types are available at higher cost. For the TT1200-series, a polarized capacitor is appropriate, with the positive end towards CM_{out} (pin 8), because of the direction of the input bias currents for internal opamps OA_1 and OA_2. Furthermore, because C_b never has much voltage across it[2], it only needs to support a few tens of mV. Therefore, we recommend a 220 uF, 3V capacitor for C_b.

RFI Protection[3]

As an input stage, the TT1200-series ICs are susceptible to RF interference (RFI). Like most semiconductor devices, if high levels of RF are permitted at the input pins of TT1200-series parts, they may become nonlinear, which can create audible interference. Therefore, it is good design practice to filter unwanted high frequencies at the input of any product in which the TT1200-series is used. The objective should be to prevent RF from entering the chassis, and especially, the circuit board of any devices using a TT1200-series part. Generally, this is done by means of small capacitors connected between the signal inputs and chassis ground, with the capacitors located as physically close to the input connectors as possible.

Figure 11 shows a basic, simple application circuit to protect the TT1200 series against RFI. For many non-demanding applications, this simple circuit will suffice. C_1 and C_2 provide RF bypassing from pins 2 and 3 of the input XLR connector to chassis ground and the XLR connector's shell (which are tied together, ideally only at the XLR connector jack). RF picked up on the cable plugged into the connector is conducted by C_1 and C_2 to chassis ground. Chassis ground should connect to circuit ground through one (and only one) low inductance path, usually at the power supply connector.

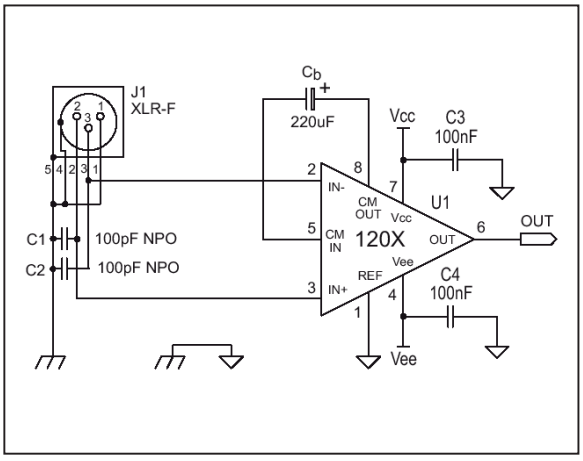


Figure 11. TT1200 application with simple RFI protection

1. Lack of proper bypassing may not cause obvious problems at normal temperatures. We have seen cases in which improperly bypassed parts begin to draw excessive current when operated near their upper temperature limits. Close bypassing prevents this phenomenon.
2. Even at DC, Cb will not see much voltage, because the signal at the junction of R_7 and R_8 should closely equal the signal at the junction of R_{10} and R_{11}. With OA_4 configured for unity gain, both ends of C_b see the same signal - AC and DC - except for offsets.
3. Good practice to protect inputs against RFI is a science in itself, and it is beyond the scope of this data sheet to provide more than a glimpse of this complex subject. We refer the interested reader to:

Considerations in Grounding and Shielding Audio Devices, by Stephan R. Macatee, JAES Volume 43, Number 6, pp.472-483; June 1995;
Noise Susceptibility in Analog and Digital Signal Processing Systems, by Neil A. Muncy, AES 97th Convention Preprint 3930, October 1996.

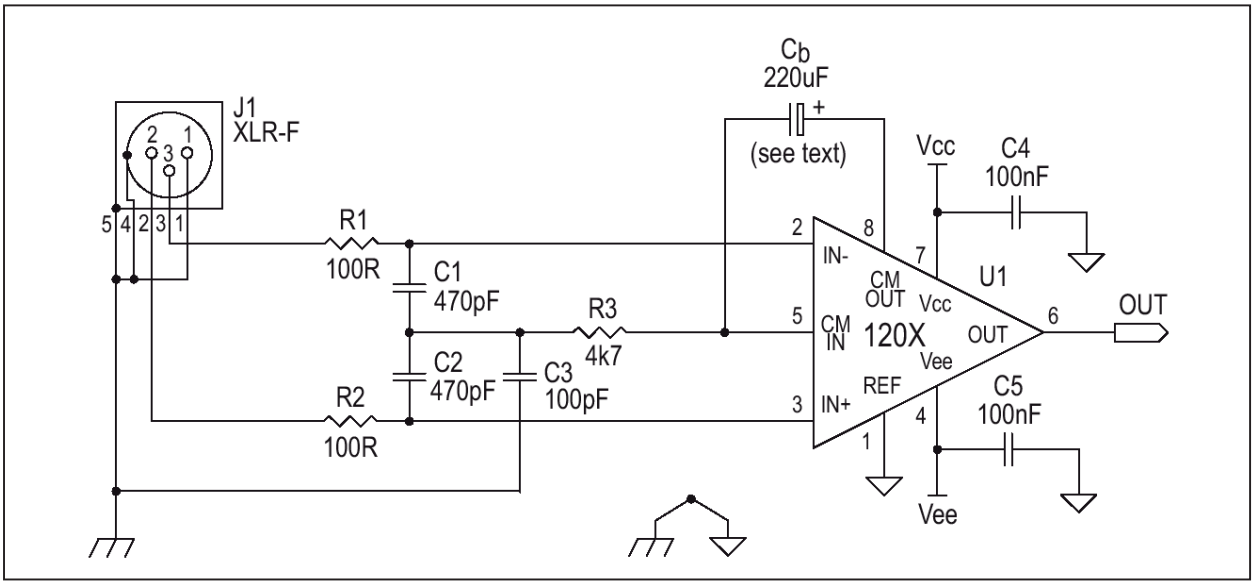


Figure 12. TT1200 application with recommended RFI protection.

The one drawback to this circuit is that C_1 and C_2 will reduce the common-mode input impedance of the TT1200 stage to ~ 80 k at 20 kHz. Of course, this figure drops by a factor of ten for each decade increase in frequency. Additionally, any mismatch between these capacitors can unbalance an interfering common mode signal, thus making it impossible for the TT1200 to reject it.

Figure 12 shows a more elaborate and robust circuit for RFI protection. While more complex, it offers many improvements over the circuit of Figure 11 that make it worth serious consideration. First, C_1 and C_2 are larger than their counterparts in Figure 11. Because they are in series with each other, they act as a 235 pf capacitor across pins 2 and 3 of the XLR. This allows them to be effective at lower frequencies. Second, because their center point ties to chassis ground through a smaller, common capacitor (C_3 , 100 pf), any mismatch in their values has less tendency to unbalance common-mode signals compared to the circuit of figure 10[4]. Third, because they are driven from the common-mode bootstrap circuit through R_3 , this common point gains the benefit of the InGenius common-mode bootstrapping. Finally, R_1 and R_2 provide some additional build out impedance against which the bypass capacitors can work, making the entire network more effective against strong RF signals.

ESD Protection

All the TT1200-series ICs contain internal over-voltage protection circuitry for the two input pins. Figure 13 is an equivalent circuit of this circuitry.

These internal diodes provide modest protection against common low-voltage ESD incidents. However, because these ICs are intended to be connected directly to the input connectors of electronic products, they may be exposed to unpredictable and possibly extreme ESD. For ESD to affect the InGenius operation, it would have to be conducted via one of the input connectors to the device itself. This is unlikely, but certainly not impossible. Not surprisingly, TT Semiconductor own testing indicates that repeated exposure to high levels (above 1 kV) of ESD through pins 2 and/or 3 of the input XLR connector can adversely affect the device's CMRR, and may cause failure if the ESD reaches sufficiently high levels.

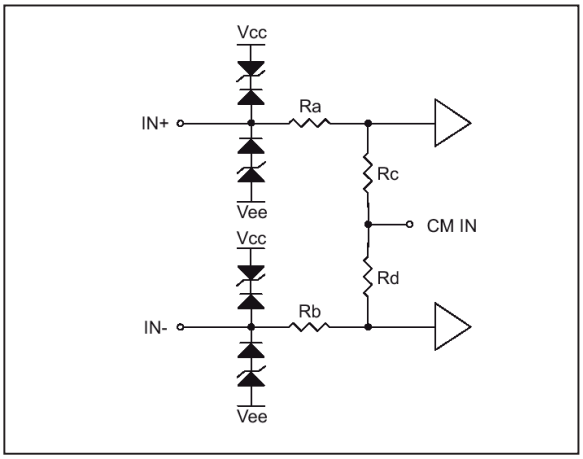


Figure 13. Internal input protection circuitry

TT Semiconductor; 325 North Shepard Street; Anaheim, California 92806; USA
Tel: 1 714 257 2257; Fax: 1 714 257 2252; Web: www.ttsemiconductor.com

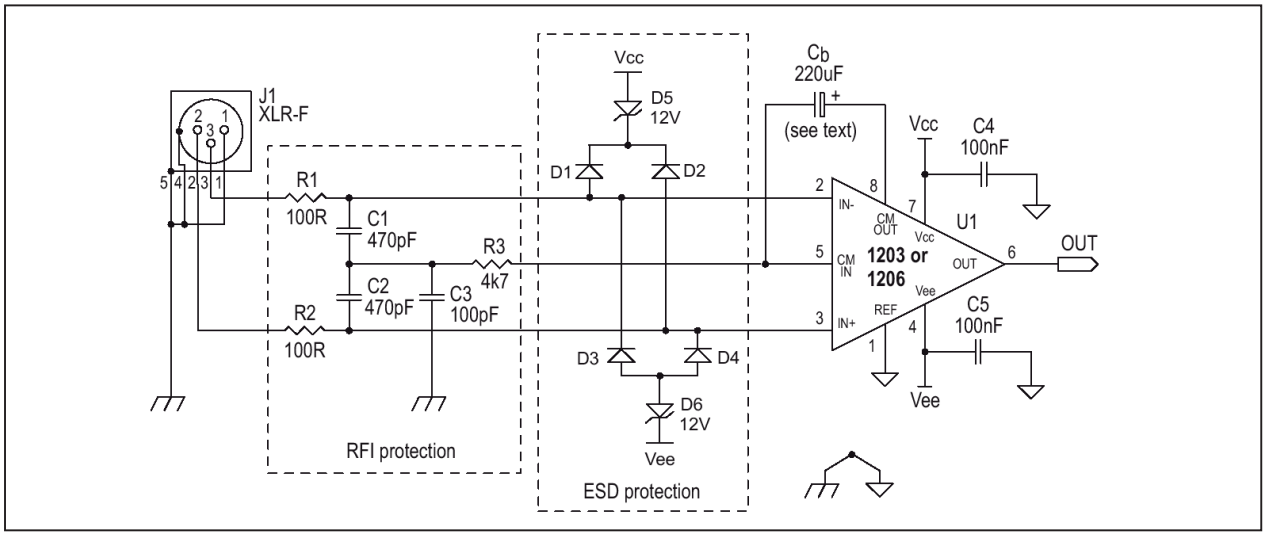


Figure 14. RFI and ESD protection for the TT1203 and TT1206

If the application requires surviving such ESD incidents, TT Semiconductor recommends the circuit of either Figure 14 or 15. Figure 14 is appropriate for the TT1203 and TT1206, both of which support input signals that swing higher than the supply rails. This arrangement of signal and Zener diodes permits the maximum allowable (audio) input signal to reach the IC's input pins, but directs high-energy ESD impulses to the rails. So long as the supply rails are adequately de-coupled and the diodes themselves are reasonably robust, all but the most drastic ESD events will not affect the TT1203/6 IC itself. Figure 15, which works similarly, is appropriate for the TT1200, which is limited to input signals up to about the supply rails.

D_1 through D_4 in figures 14 and 15 can be 1N4148 types, while the 12V Zener diodes should be ½ watt to allow them to support relatively high currents with 12V across them for the short duration of an ESD pulse.

We will continue to work to find real world solutions to the often difficult problem of ESD protection. Please look to our web site for future application notes regarding this subject.

Note that we know of no circuit that will protect against really strong ESD, such as lightning, so please do not take this advice as suggesting that the circuits of Figures 14 and 15 are completely immune to ESD!

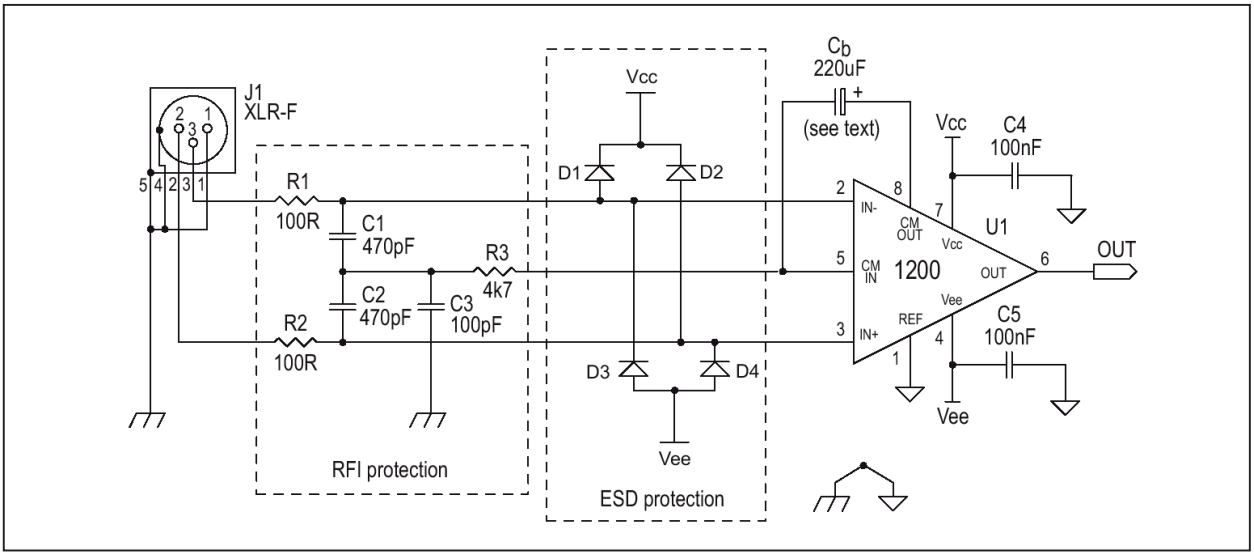


Figure 15. RFI and ESD protection for the TT1200

TT Semiconductor; 325 North Shepard Street; Anaheim, California 92806; USA
Tel: 1 714 257 2257; Fax: 1 714 257 2252; Web: www.ttsemiconductor.com

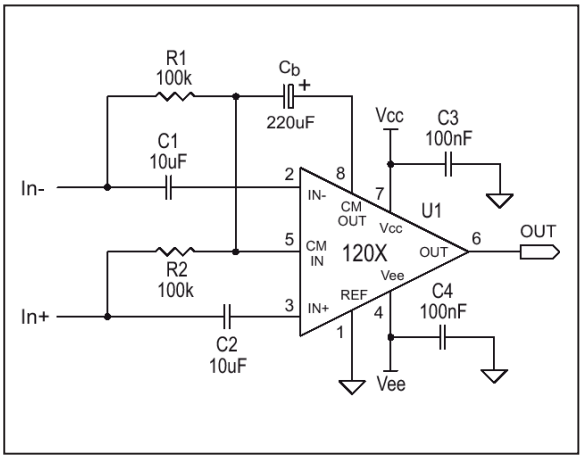


Figure 16. AC coupling TT1200-series inputs

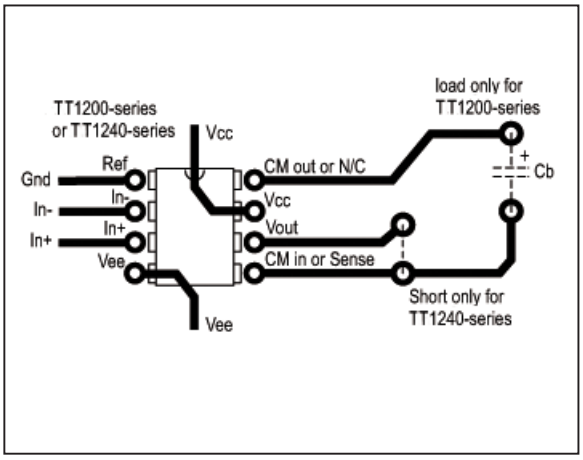


Figure 17. Dual PCB layout for TT120X and TT124X

AC Coupling Inputs

It is not necessary to AC couple the TT1200-series inputs. However, if desired, we recommend the circuit of Figure 16. In this circuit Resistors R1 and R2 benefit from the common-mode bootstrap via their connection to CM_{in}. This reduces their impact on common-mode input impedance, preserving the benefit of InGenius, while providing a discharge path for charge in the input coupling capacitor. Choose capacitors large enough to present minimal impedance to the lowest signals of interest, compared to the differential input impedance of the InGenius IC (48 k). If desired, this may be combined with the RF protection of Figures 11 or 12, and ESD protection of figures 14 or 15.

Dual Layout Option

InGenius ICs are available only from TT Semiconductor. Should a manufacturer wish to provide some alternatives to the TT1200 series, it is possible to lay out the circuit board for a TT1200 such that a TT Semiconductor's TT1240-series (conventional) balanced input stage could be substituted in a pinch. Since the TT1240 series is pin-compatible with similar parts available from other manufacturers, this offers the possibility of several reduced-performance second sources if TT1200-series ICs were for unavailable for any reason.

The PCB layout shown in Figure 17 provide manufacturers with the option to load a PCB with either of these input stages. Note that these figures are not to scale. The interconnects should be as short as practical, constrained only by component size and relevant manufacturing considerations.

When a TT1200-series IC is installed, capacitor C_b is connected between CM_{in} and CM_{out} . No connection is made between V_{out} and CM_{in}. When the Twilight Technology's TT1240-series is used, capacitor C_b is removed, and a jumper connects the V_{out} and Sense pins.

TT Semiconductor; 325 North Shepard Street; Anaheim, California 92806; USA
Tel: 1 714 257 2257; Fax: 1 714 257 2252; Web: www.ttsemiconductor.com

Ordering Information

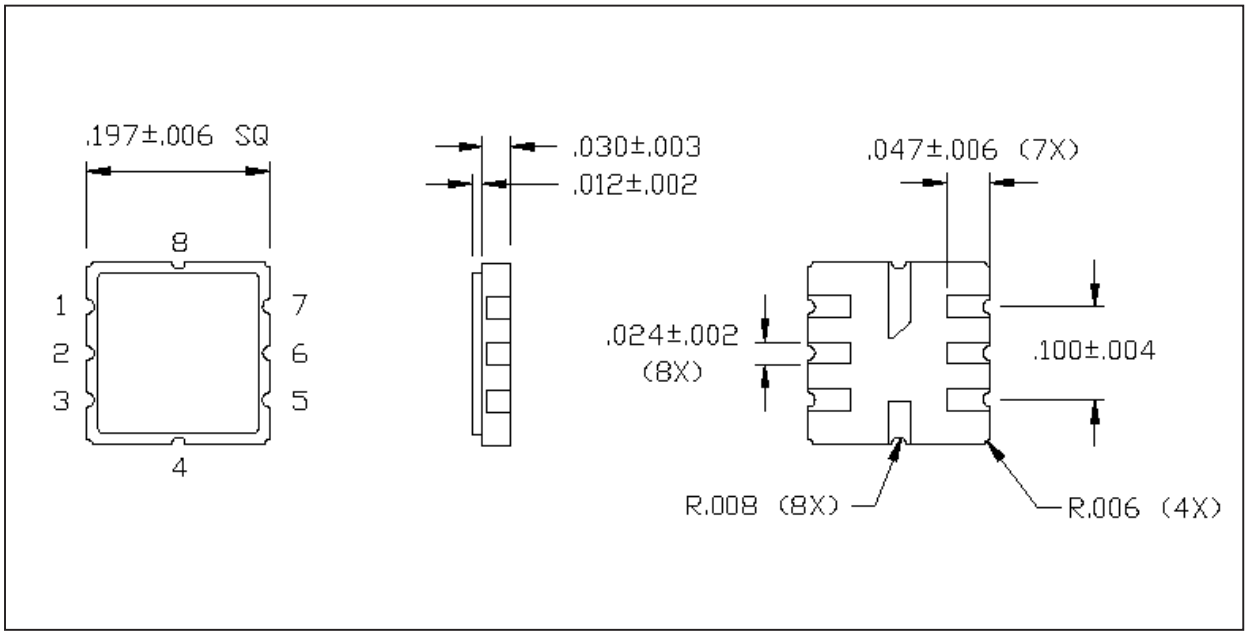


Figure 18. Ceramic LCC package outline

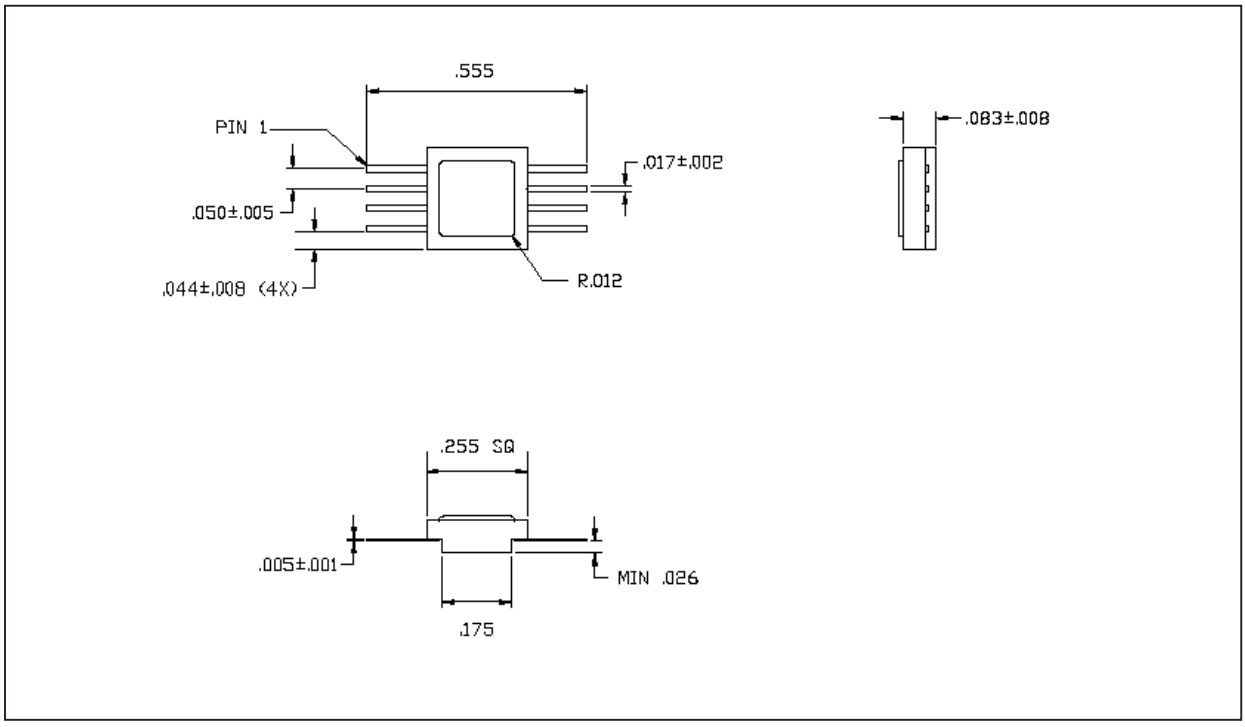


Figure 19. Ceramic Flatpack package outline

TT Semiconductor; 325 North Shepard Street; Anaheim, California 92806; USA
Tel: 1 714 257 2257; Fax: 1 714 257 2252; Web: www.ttsemiconductor.com

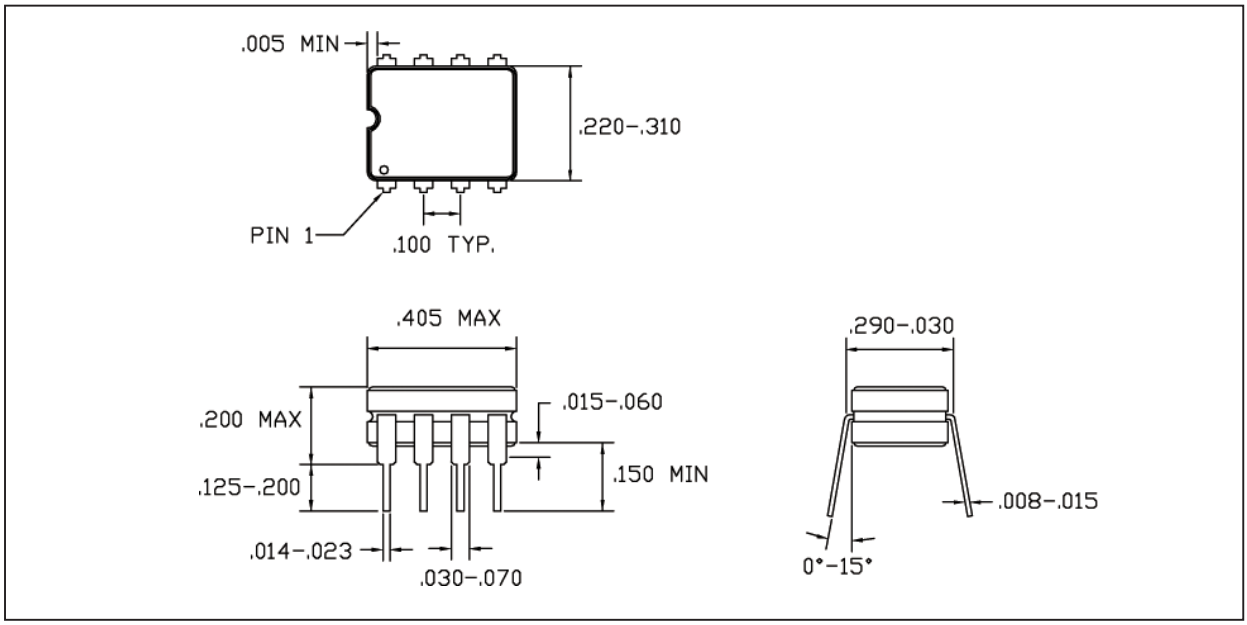


Figure 20. Ceramic dual in-line package outline

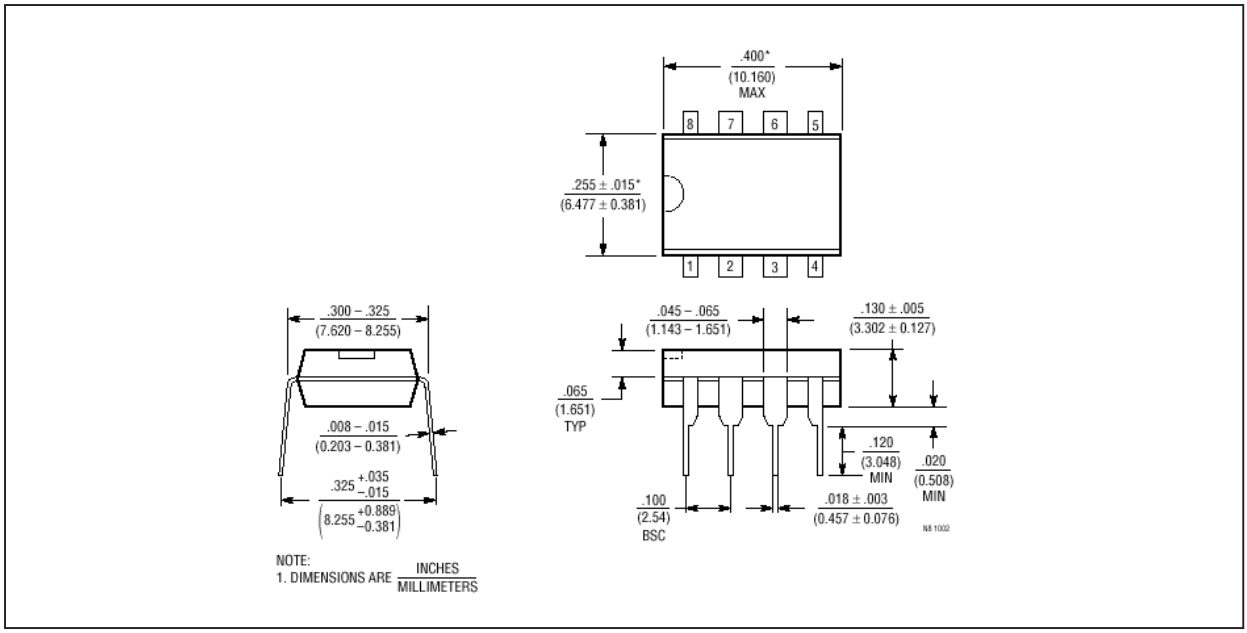


Figure 21. Plastic Extended Temperature dual in-line package outline

TT Semiconductor; 325 North Shepard Street; Anaheim, California 92806; USA
Tel: 1 (714) 257-2257; Fax: 1 (714) 257-2252; Web: www.ttsemiconductor.com

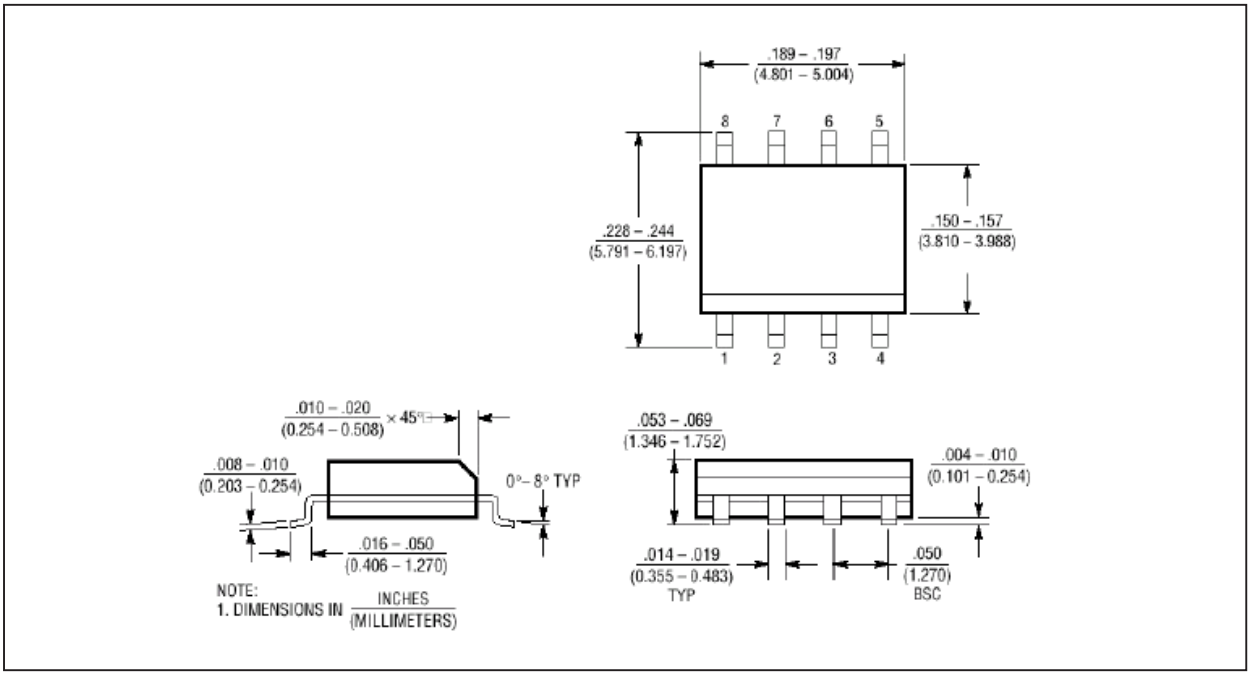


Figure 22. Plastic Extended Temperature SOIC

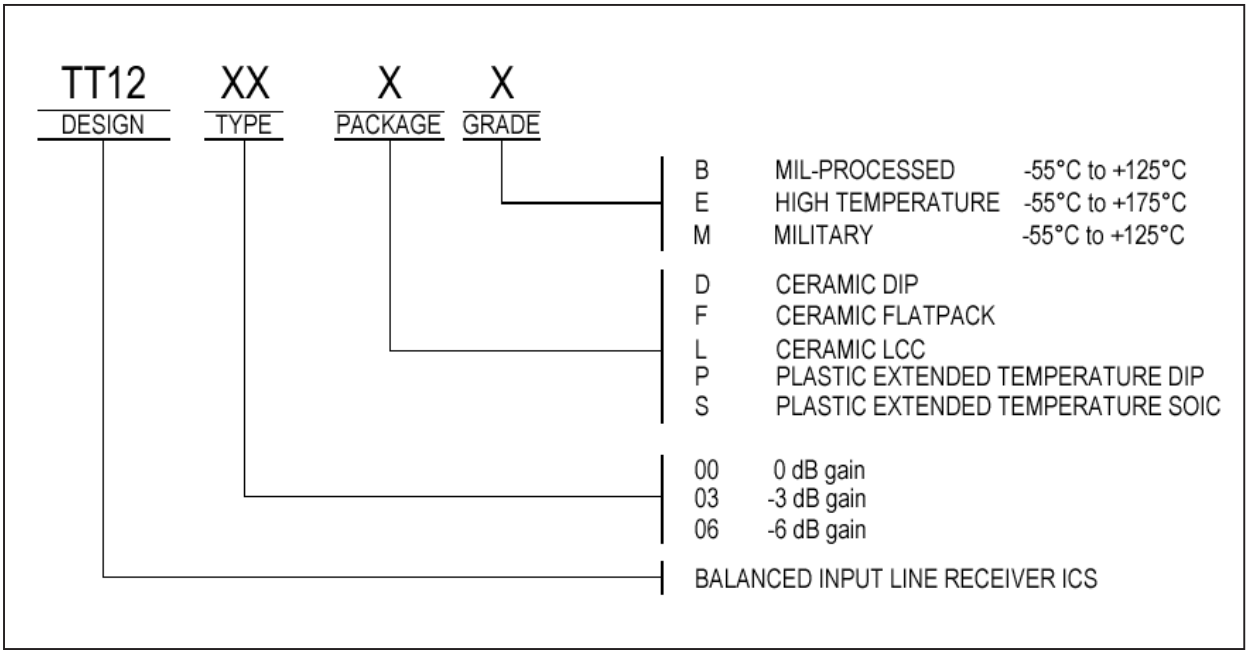


Figure 23. Ordering Information

TT Semiconductor; 325 North Shepard Street; Anaheim, California 92806; USA
Tel: 1 (714) 257-2257; Fax: 1 (714) 257-2252; Web: www.ttsemiconductor.com