Extended Temperature, 5 Volt, 1 Megabit EEPROM

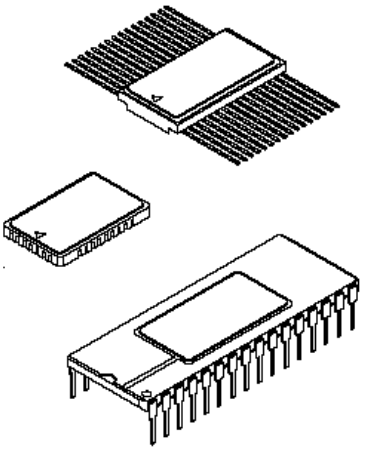
TTE128HT8F/G/K/N

DESCRIPTION:

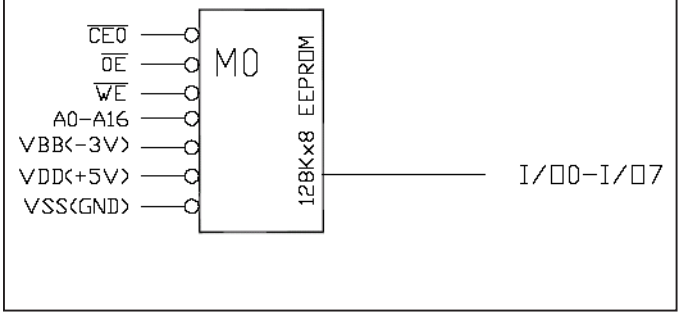
The TTE128HT8F/G/K/N memory contains a 128Kx8 EEPROMs, packaged in a hermetically sealed cermaic package, making the modules suitable for commercial, industrial military and extended temperature applications. The modules are organized in a 128Kx8 configuration supporting 256-Byte Page write operations. This keeps write cycle timing down to as low as 19us/Byte which enables completely writing one memory in less than 2.5 seconds.

FEATURES:

Organizations Available: 128Kx8
Access Times: 200, 250ns
200°C Extended Temperature Range Full Functionality
Single +5V Power Supply, 5% Tolerance
Single Byte or 2 to 256 Byte Page Writes
Self Timed Writes - No Erase before Writes
Easy Programming Algorithms, No Overerase Problem
Data Retention: 100 Years.
Endurance: 10,000 Write Cycles
Packages Available:
32 - Pin Ceramic Side Brazed DIP
32 - Pin Ceramic FLATPACK
32 - Pin Ceramic LCC
36 - Pin Ceramic PGA



FUNCTIONAL BLOCK DIAGRAM

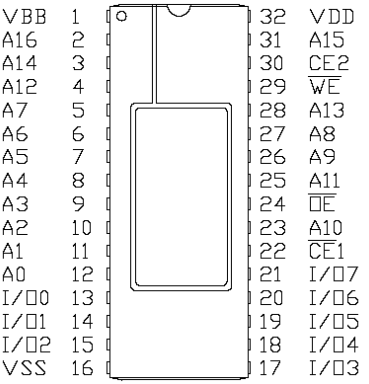


PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O8	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE0}$	Low Chip Enables
$\overline{OE}$	Output Enable
V_{BB}	Back Bias (-3V)
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

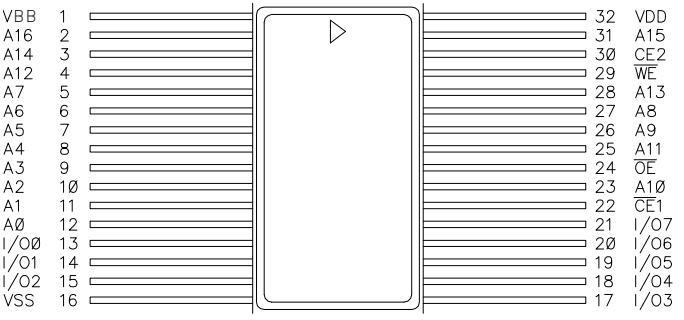
BACK BIAS VOLTAGE (V_{BB})
It is required to provide -3V on pin 40 (D3). This negative voltage improves higher temperature functionality.

PIN-OUT DIAGRAM

DIP PACKAGE

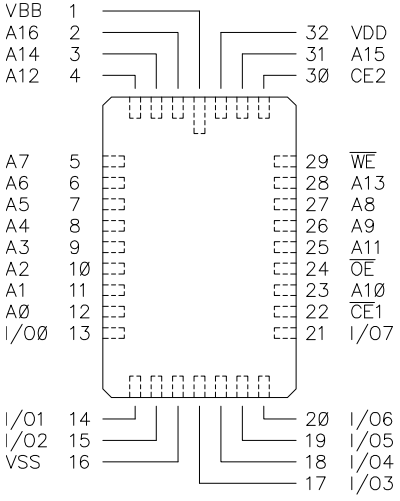


FLAT PACK PACKAGE

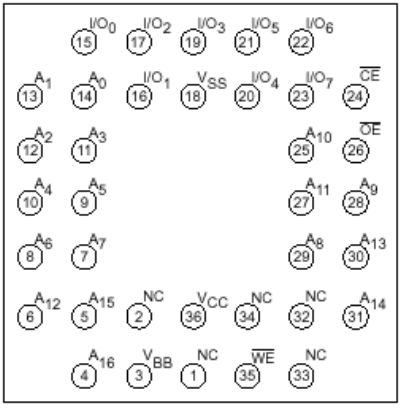


PIN-OUT DIAGRAM

LCC PACKAGE



PGA PACKAGE



DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The TTE128HT8 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, which-ever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

The page write feature of the TTE128HT8 allows one entire memory to be written in 5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the TTE128HT8 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A8 through A16) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address. The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty-six bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100ms of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100ms, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycletime of 100ms.

HARDWARE DATA PROTECTION

The TTE128HT8 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is 3.4V.
- Write inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SYSTEM CONSIDERATIONS

Because the TTE128HT8 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

It has been demonstrated that markedly higher temperature performance can be obtained from this device if $\overline{CE}$ is left enabled throughout the read and write operation.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the TTE128HT8 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 F high frequency ceramic capacitor be used between V_{DD} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 F electrolytic bulk capacitor be placed between V_{DD} and V_{SS} for each four modules employed in the array. This bulk capacitor is employed to overcome

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
TTE128HT8.....-55°C-200°C
Voltage on any Pin with
Respect to Vss.....-1V to +7V D.C.
Output Current.....5mA
Lead Temperature
(Soldering, 10 seconds).....220°C

*COMMENT

Stresses above thoselisted under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device

RECOMMENDED OPERATING RANGE					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
V_{BB}	Back Bias Voltage	-3.3	-3.0	-2.7	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD} + 1	V
V_{IL}	Input LOW Voltage	-1		0.6	V
T_A	Operating Temp	-40	+25	+175	°C

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH}= -1.0mA	2.4		V
V_{OL}	LOW Voltage	I_{OL}=2.1mA		0.4	V

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active
Write Inhibit	X	H	X	-	-
Write Inhibit	X	X	L	-	-

CAPACITANCE (2): T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	6	pF	V_{IN} = 0V
C_{CE}	Chip Enable	4		
C_{WE}	Write Enable	6		
C_{OE}	Output Enable	6		
$C_{I/O}$	Data Input/Output	4		

Note: (2) This Parameter is periodically sampled and not 100% tested

DC OPERATING CHARACTERISTICS: +25°C					
Symbol	Parameter	Test Conditions	Limits		Unit
			Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-10	+10	A
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ = V_{IH}	-10	+10	A
I_{CC}	Active Supply Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I_{OUT} = 0mA Address Inputs = .4/2.4V @ f=5MHz		35	mA
I_{SB}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, All I/O's = Open, Other Inputs = V_{IH}		2	mA
I_{BB}	Back Bais Current	V_{BB} = -3V 10%		125	A
V_{IL} (1)	Input Low Voltage		-1	0.6	V
V_{IH} (1)	Input High Voltage		2.2	V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OUT} = 1.0 mA		0.5	V
V_{OH}	Output High Voltage	I_{OUT} = -400 A	2.6		V

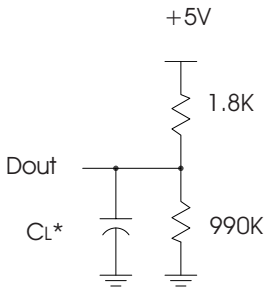
Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested. Unless otherwise stated, measurements are made at +25°C, V_{DD} = 5.0V.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	10ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100pF	except t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OLZ}, and t_{WHZ}
2	5pF	t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OLZ}, and t_{WHZ}

Figure 1. Output Load

*Including Probe and Jig Capacitance.



Power-Up Timing			
Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to Read Operation	100	s
t_{PUW}(2)	Power-Up to Write Operation	5	ms

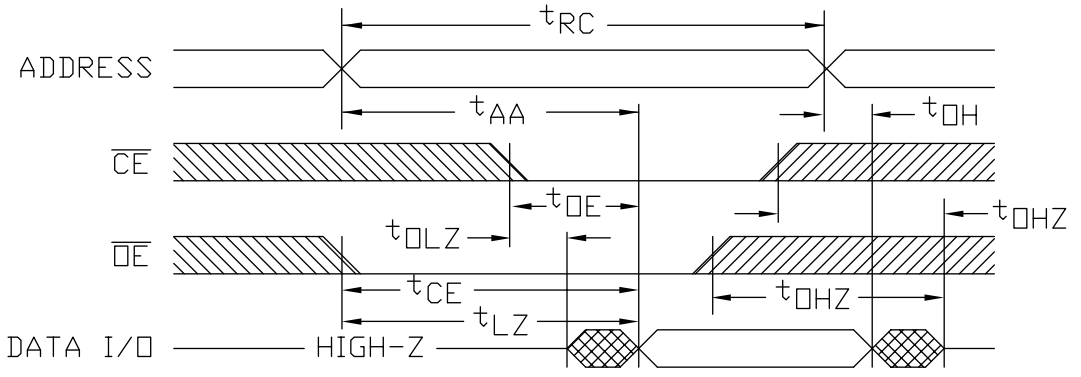
Note: (2) This Parameter is periodically sampled and not 100% tested

Endurance and Data Retention			
Parameter	Min.	Max.	Units
Endurance	10,000	-	Cycles per Byte
Data Retention	100	-	Years

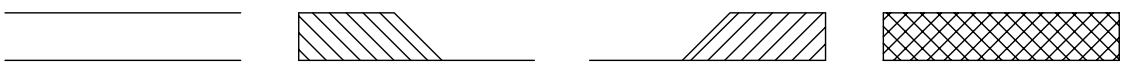
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges							
No.	Symbol	Parameter	200ns		250ns		Unit
			Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	200		250		ns
2	t_{AA}	Address Access Time		200		250	ns
3	t_{CE}	$\overline{CE}$ to Output Valid		200		200	ns
4	t_{OE}	Output Enable to Output Valid		50		50	ns
5	t_{LZ}	$\overline{CE}$ to Output in LOW-Z	0		0		ns
6	t_{OLZ}	Output Enable to Output in LOW-Z	0		0		ns
7	t_{HZ}	$\overline{CE}$ to Output in HIGH-Z [4, 5]		50		50	ns
8	t_{OHZ}	Output Enable to Output in HIGH-Z		50		50	ns
9	t_{OH}	Output Hold from Address Change		0		0	ns

Note: (3) t_{LZ} min., t_{HZ}, T_{OLZ} min. and t_{OHZ} are periodically sampled and not 100% tested

READ CYCLE



WAVEFORM KEY

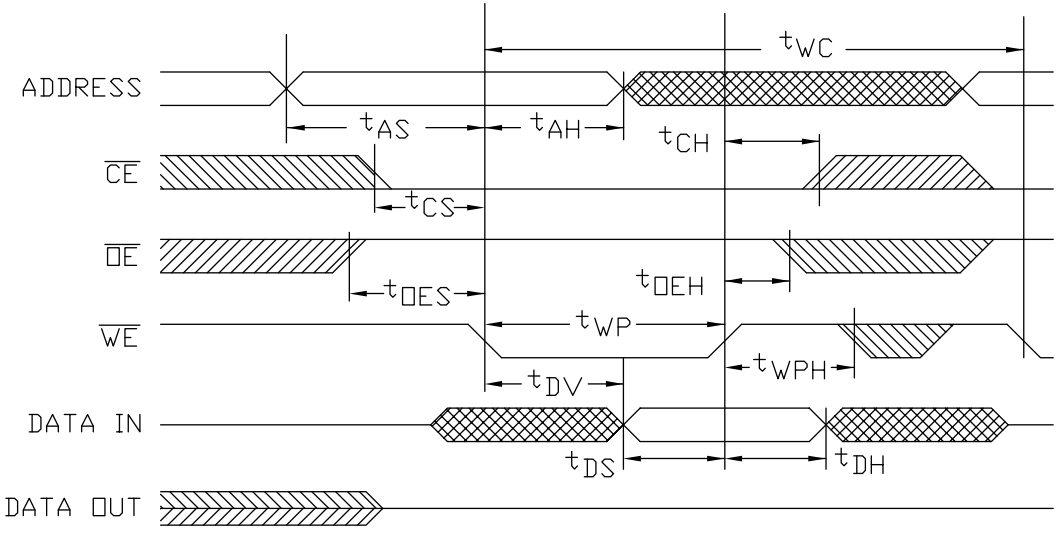


Data Valid | Travsition from HIGH to LOW | Travsition From HIGH to LOW | Data Undefined or Don't Care

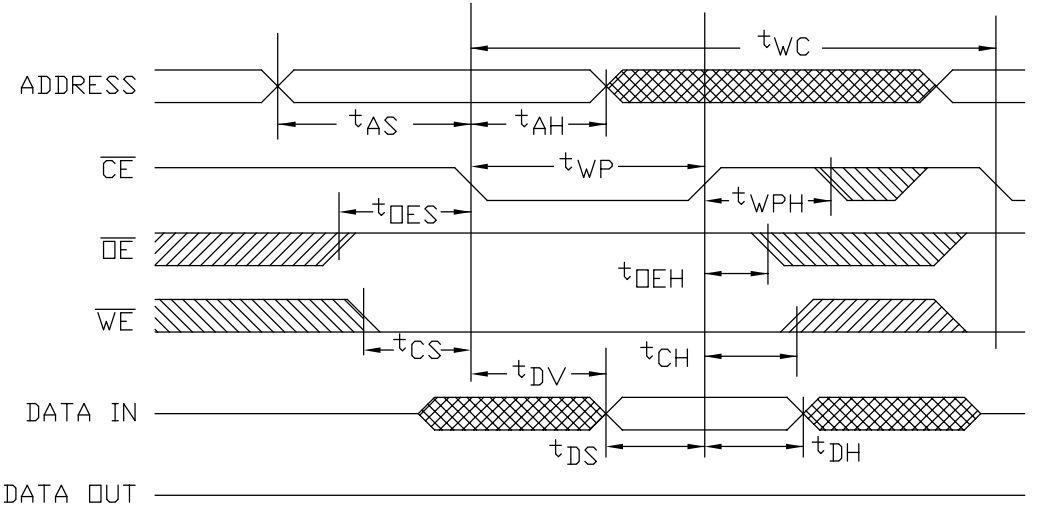
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6, 7]: Over operating ranges					
No.	Symbol	Parameter	Min.	Max.	Unit
13	t_{WC}	Write Cycle Time		10	ms
14	t_{AS}	Address Setup Time	20		ns
15	t_{AH}	Address Hold Time	100		ns
16	t_{CS}	Write Set-Up Time	0		ns
17	t_{CH}	Write Hold Time	0		ns
18	t_{CW}	Chip Enable Low Pulse Width	200		ns
18	t_{OES}	Output Enable HIGH Setup Time	10		ns
19	t_{OEH}	Output Enable HIGH Hold Time	10		ns
20	t_{WP}	Write Enable Low Pulse Width	200		ns
21	t_{WPH}	Write Enable High Recovery Time	200		ns
22	t_{DV}	Data Valid		1	s
22	t_{DS}	Data Setup	100		ns
22	t_{DH}	Data Hold	25		ns
22	t_{DW}	Delay to Next Write	10		s
22	t_{BLC}	Byte Load Cycle	0.4		s

Notes: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is

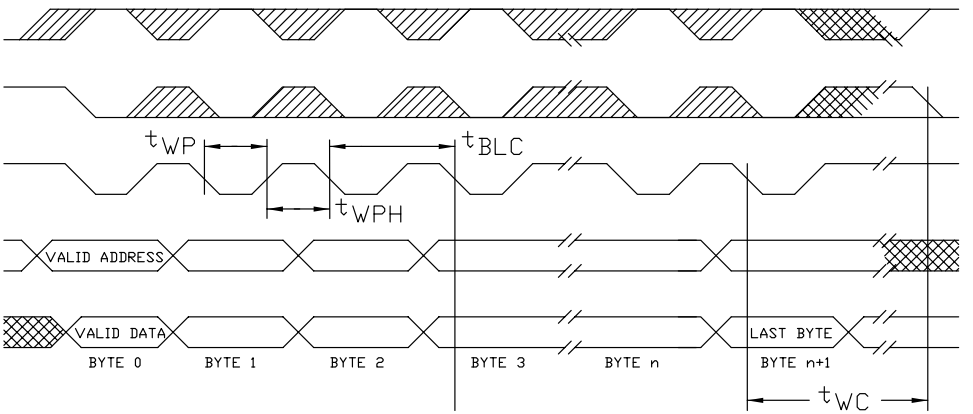
WRITE CYCLE 1: $\overline{WE}$ Controlled



WRITE CYCLE 2: $\overline{CE}$ Controlled



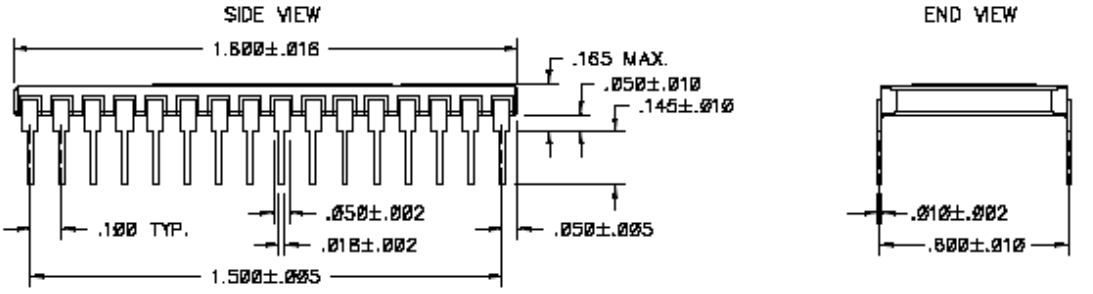
PAGE WRITE CYCLE



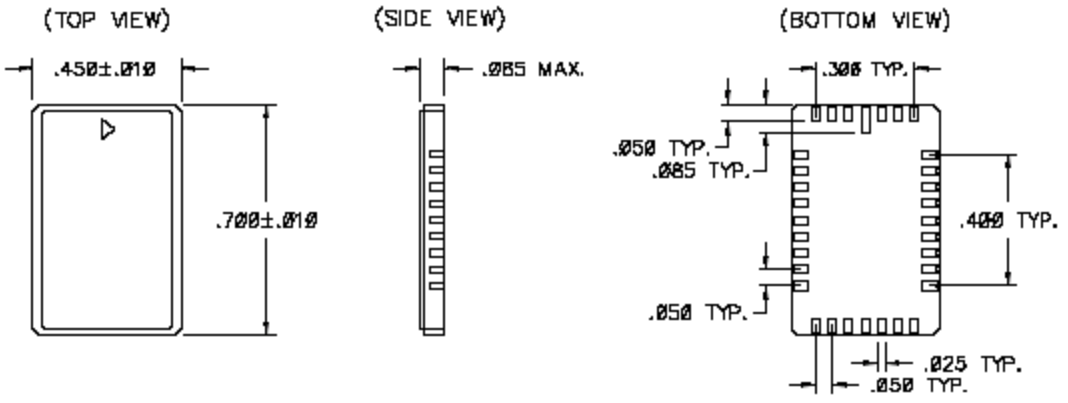
NOTES: (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

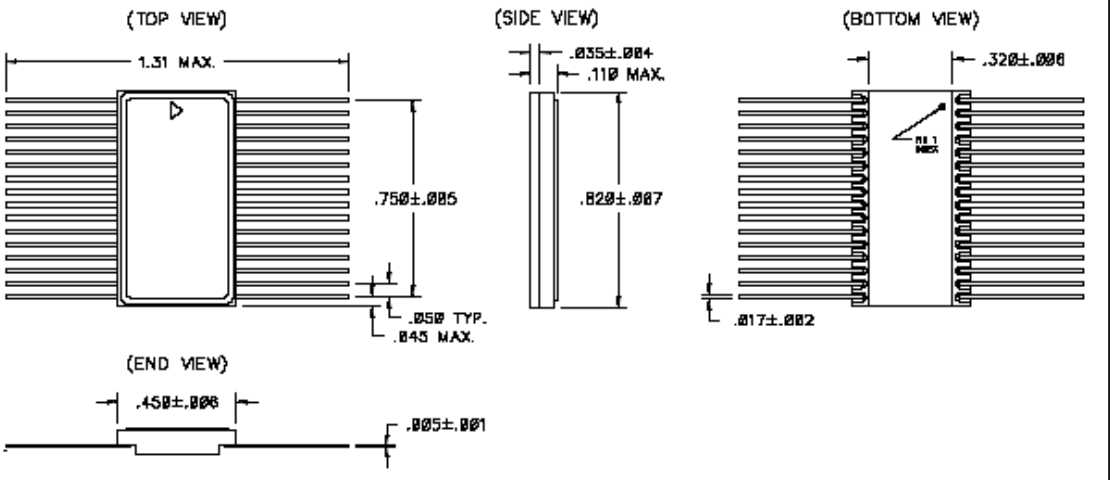
CERAMIC DIP MECHANICAL DRAWING



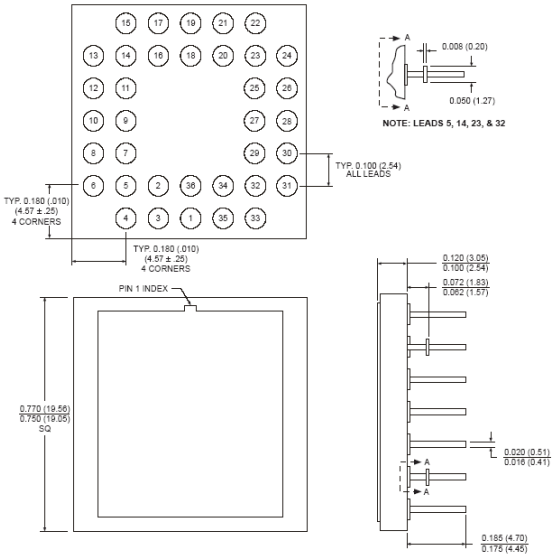
CERMAIC LCC MECHANICAL DRAWING



CERAMIC FLATPACK MECHANICAL DRAWING



CERAMIC PGA MECHANICAL DRAWING



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