Description

The TTE25C16 is an are electrically erasable PROM device that uses the Serial Peripheral Interface (SPI) for communications. The TTE25C16 is 16Kbit (2048 x 8). This EEPROM is offered in a wide operating voltage range of 3.0V to 5.5V to be compatible with most application voltages. The TTE25C32/64 is designed to be an efficient SPI EEPROM solution. The devices are packaged in 8-pin CDIP, 8-pin LCC, 8-pin SOIC and 8-pin Flatpack.

The functional features of the TTE25C16 allows it to be among the most advanced serial non-volatile memories available. Each device has a Chip-Select (CS) pin, and a 3-wire interface of Serial Data In (SI), Serial Data Out (SO), and Serial Clock (SCK). While the 3-wire interface of the TTE25C16 provides for high-speed access, a HOLD pin allows the memories to ignore the interface in a suspended state; later the HOLD pin re-activates communication without reinitializing the serial sequence. A Status Register facilitates a flexible write protection mechanism, and a device-ready bit (RDY).

FEATURES

Serial Peripheral Interface (SPI) Compatible
-Supports SPI Modes 0 (0,0) and 3 (1,1)

Wide-voltage Operation
-Vcc = 3.0V to 5.5V

Low Power CMOS
-Active Current less than 3 mA (3.0V)
-Stanby Current less than 2 μA (3.0V)

FEATURES

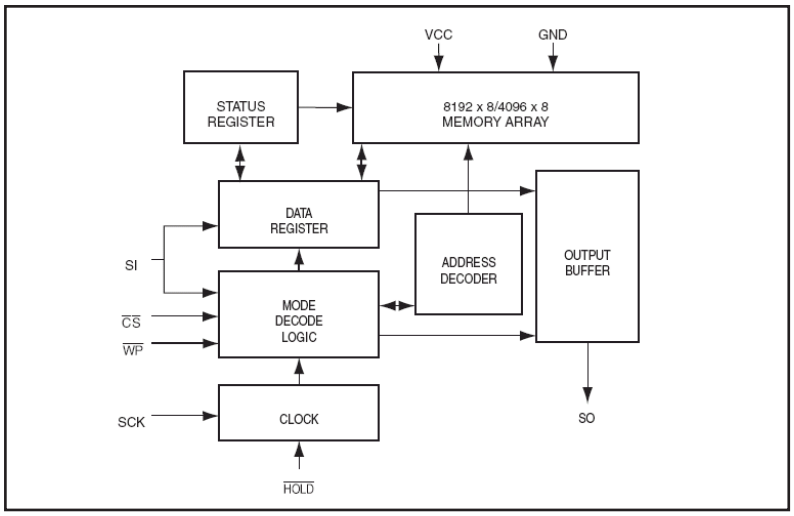
10 MHz Clock Rate (5V)

Self timed write cycles (5 ms MAX)

High-reliability

32 byte page write mode
-Partial page writes allowed

8-pin CDIP, 8-pin LCC, and 8-pin Flatpack and 8-pin Plastic SOIC Packages avaliable



Function Block Diagram

Pin Name	DIP, SOIC, Flat Pack, LCC Package
$\overline{CS}$	1
SO	2
$\overline{WP}$	3
GND	4
SI	5
SCK	6
$\overline{HOLD}$	7
VCC	8

Table 1. Pin Configurations

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PIN DESCRIPTIONS

CS- Chip Select

SCK- Serial Data Clock

SI- Serial Data Input

SO- Serial Data Output

GND- Ground

VCC- Power

WP- Write Protect

PIN DESCRIPTIONS

Serial Clock (SCK): This timing signal provides synchronization between the microcontroller and TTE25C16. Op-Codes, byte addresses, and data are latched on SI with a rising edge of the SCK. Data on SO is refreshed on the falling edge of SCK for SPI modes (0,0) and (1,1). Serial Data Input (SI): This is the input pin for all data that the TTE25C16 is required to receive. Serial Data Output (SO): This is the output pin for all data transmitted from the TTE25C16.

Chip Select (CS): The CS pin activates the device. Upon power-up, CS should follow Vcc. When the device is to be enabled for instruction input, the signal requires a High-to-Low transition. While CS is stable Low, the master and slave will communicate via SCK, SI, and SO signals. Upon completion of communication, CS must be driven High. At this moment, the slave device may start its internal write cycle. When CS is high, the device enters a power-saving standby mode, unless an internal write operation is underway. During this mode, the SO pin becomes high impedance.

Write Protect (WP): The purpose of this input signal is to initiate Hardware Write Protection mode. This mode prevents the Block Protection bits and the WPEN bit in the Status Register from being altered. To cause Hardware Write Protection, WP must be Low at the same time WPEN is 1. WP may be hardwired to Vcc or GND.

HOLD (HOLD): This input signal is used to suspend the device in the middle of a serial sequence and temporarily ignore further communication on the bus (SI, SO, SCK). Together with Chip Select, the HOLD signal allows multiple slaves to share the bus. The HOLD signal transitions must occur only when SCK is Low, and be held stable during SCK transitions. (See Figure 8 for Hold timing) To disable this feature, HOLD may be hardwired to Vcc.

SERIAL INTERFACE DESCRIPTION

MASTER: The device that provides a clock signal.

SLAVE: The TTE25C16 is a slave because the clock signal is an input.

TRANSMITTER/RECEIVER: The TTE25C16 has both data input (SI) and data output (SO).

MSB: The most significant bit. It is always the first bit transmitted or received.

OP-CODE: The first byte transmitted to the slave following CS transition to LOW. If the OP-CODE is a valid member of the TTE25C16 instruction set (Table 3), then it is decoded appropriately. If the OP-CODE is not valid, and the SO pin remains in high impedance.

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STATUS REGISTER

Table 1. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Notes:

1. X = Don't care bit.

2. During internal write cycles, bits 0 to 7 are temporarily 1's.

The status register contains 8-bits for write protection control and write status. (See Table 1). It is the only region of memory other than the main array that is accessible by the user.

The Status Register is Read-Only if either: a) Hardware Write Protection is enabled or b) WEN is set to 0. If neither is true, it can be modified by a valid instruction.

Ready ($\overline{RDY}$), Bit 0: When $\overline{RDY}$ = 1, it indicates that the device is busy with a write cycle. $\overline{RDY}$ = 0 indicates that the device is ready for an instruction. If $\overline{RDY}$= 1, the only command that will be handled by the device is Read Status Register. Don't Care, Bits 4-6: Each of these bits can receive either 0 or 1, but values will not be retained. When these bits are read from the register, they are always 0.

Write Protect Enable (WPEN), Bit 7: This bit can be used in conjunction with WP pin to enable Hardware Write Protection, which causes the Status Register to be read-only. The memory array is not protected by this mode. Hardware Write Protection requires that WP = 0 and WPEN = 1; it is disabled otherwise. Note: WPEN cannot be changed from 1 to 0 if the WP pin is already set to Low. (See Table 4 for data protection relationship)

Block Protect (BP1, BP0), Bits 2-3: Together, these bits represent one of four block protection configurations implemented for the memory array. (See Table 2 for details.) BP0 and BP1 are non-volatile cells similar to regular array cells, and factory programmed to 0. The block of memory defined by these bits is always protected,regardless of the setting of WPEN, WP, or WEN.

Table 2. Block Protection

	Status Register Bits		Array Addresses Protected
Level	BP1	BP0	TTE25C16
0	0	0	None
1(1/4)	0	1	0600h 07FFh
2(1/2)	1	0	0400h 07FFh
3(All)	1	1	0000h 07FFh

Don't Care, Bits 4-6: Each of these bits can receive either 0 or 1, but values will not be retained. When these bits are read from the register, they are always 0.

Write Protect Enable (WPEN), Bit 7: This bit can be used in conjunction with WP pin to enable Hardware Write Protection, which causes the Status Register to be read-only. The memory array is not protected by this mode. Hardware Write Protection requires that WP = 0 and WPEN = 1; it is disabled otherwise. Note: WPEN cannot be changed from 1 to 0 if the WP pin is already set to Low. (See Table 4 for data protection relationship)

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DEVICE OPERATION

The operations of the TTE25C16 are controlled by a set of instructions that are clocked-in serially SI pin. (See Table 3). To begin an instruction, the chip select (CS) should be dropped Low. Subsequently, each Low-to-High transition of the clock (SK) will latch a stable value on the SI pin. After the 8-bit op-code, it may be appropriate to continue to input an address or data to SI, or to output data from SO. During data output, values appear on the falling edge of SK. All bits are transferred with MSB first. Upon the last bit of communication, but prior to any following Lowto- High transition of SK, CS should be raised High to end the transaction. The device then would enter Standby Mode if no internal programming were underway.

Table 3. Instruction Set

Name	Op-code	Operation	Address	Data(SI)	Data (SO)
WREN	0000 X110	Set Write Enable Latch	-	-	-
WRDI	0000 X100	Reset Write Enable Latch	-	-	-
RDSR	0000 X101	Read Status Register	-	-	D7-D0,...
WRSR	0000 X001	Write Status Register	-	D7-D0	-
READ	0000 X011	Read Data from Array	A15-A0	-	D7-D0,...
WRITE	0000 X010	Write Data to Array	A15-A0	D7-D0,...	-

1. X = Don't care bit. For consistency, it is best to use "0".

2. Some address bits are don't care. See Table 5.

3. If the bits clocked-in for an op-code are invalid, SO remains high impedance, and upon CS going High there is no affect. A valid op-code with an invalid number of bits clocked-in for address or data will cause an attempt to modify the array or Status Register to be ignored.

WRITE ENABLE (WREN)

When Vcc is initially applied, the device powers up with both status register and entire array in a write-disabled state. Upon completion of Write Disable (WRDI), Write Status Register (WRSR), or Write Data to Array (WRITE), the device resets the WEN bit in the Status Register to 0. Prior to any data modification, a WREN instruction is necessary to set WEN to 1. (See Figure 2 for timing).

WRITE DISABLE (WRDI)

The device can be completely protected from modification by resetting WEN to 0 through the WRDI instruction. (See Figure 3 for timing).

READ STATUS REGISTER (RDSR)

The Read Status instruction tells the user the status of Write Protect Enable, the Block Protection setting (see Table 2), the Write Enable state, and the RDY status. RDSR is the only instruction accepted when a write cycle is underway. It is recommended that the status of Write Enable and RDY be checked, especially prior to an attempted modification of data. The 8 bits of the Status Register can be repeatedly output on SO after the initial Op-code. (See Figure 4 for timing).

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WRITE STATUS REGISTER (WRSR)

This instruction lets the user choose a Block Protection setting, and set or reset the WPEN bit. The values of the other data bits incorporated into WRSR can be 0 or 1, and are not stored in the Status Register. WRSR will be ignored unless both the following are true: a) WEN = 1, due to a prior WREN instruction; and b) Hardware Write Protection is not enabled. (See Table 4 for details). Except for the RDY status, the values in the Status Register remain unchanged until the moment when the write cycle is complete and the register is updated. Note: WPEN can be changed from 1 to 0 only if WP is already set High. Once completed, WEN is reset for complete chip write protection. (See Figure 5 for timing).

READ DATA (READ)

This instruction begins with the op-code and the 16-bit address, and causes the selected data byte to be shifted out on SO. Following this first data byte, additional sequential bytes are output. If the data byte in the highest address is output, the address rolls-over to the lowest address in the array, and the output could loop indefinitely. At any time, a rising CS signal completes the operation. (See Figure 6 for timing).

WRITE DATA (WRITE)

The WRITE instruction begins with the op-code, the 16-bit address of the first byte to be modified, and the first data byte. Additional data bytes may be written sequentially to the array after the first byte. Each WRITE instruction can affect the contents of a 32 byte page, but no more. The page begins at address XXXXXXXX XXX00000, and ends with XXXXXXXX XXX11111. If the last byte of the page is input, the address rolls over to the beginning of the same page. More than 32 data bytes can be input during the same instruction, but upon a completed write cycle, a page would only contain the last 32 bytes.

The region of the array defined within Block Protection cannot be modified as long as that block configuration is selected. The region of the array outside the Block Protection can only be modified if Write Enable (WEN) is set to 1. Therefore, it may be necessary that a WREN instruction occur prior to WRITE. Hardware Write Protection has no affect on the memory array. Once Write is completed, WEN is reset for complete chip write protection. (See Figure 7 for timing).

Table 5. Address Key

Name	TTE25C16
A_N	A_{10}-A_0
Don't Care Bits	A_{15} - A_{11}

Table 4. Write Protection

WPEN	$\overline{WP}$	Hardware Write Protection	WEN	Inside Block	Outside Block	Status Register (WPEN, BP1, BP0)
0	X	Not Enabled	0	Read-only	Read-only	Read-only
0	X	Not Enabled	1	Read-only	Unprotected	Unprotected
1	0	Enabled	0	Read-only	Read-only	Read-only
1	0	Enabled	1	Read-only	Unprotected	Read-only
X	1	Not Enabled	0	Read-only	Read-only	Read-only
X	1	Not Enabled	1	Read-only	Unprotected	Unprotected

Note: X = Don't care bit.

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Absolute Maximum Ratings[1] (T_A = 25°C)

Supply Voltage (V_S)	+0.5 to +6.5 V	Storage Temperature (T_{STG})	-65 to +210°C
Voltage on Any Pin (V_P)	-0.5 to V_{CC} +0.5 V	Output Current (I_{OUT})	5 mA
Temperature Under Bias (T_{BIAS}) Ceramic Package	-55 to +200 °C	Temperature under Bias (T_{BIAS}) Plastic Packages	-55 to 150 C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Military	V_{CC}	-55 °C to +125 °C	3.0		5.5	V
Extended Military	V_{CC}	-55 °C to +150 °C	3.0		5.5	V
Extended Temperature	V_{CC}	-55 °C to +175 °C	4.5		5.5	V
Highest Temperature	V_{CC}	-55 °C to +200 °C	4.5		5.5	V

Capacitance[2,3]

Parameter	Symbol	Conditions	Max	Units
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	8	pF

1. Stress greater than the conditions listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device outside these conditions or those indicated in the operational sections of this specification is not implied. Exposure to these conditions for extended periods may affect reliability.

2. Tested initially and after any design or process changes that may affect these parameters and not 100% tested.

3. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

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DC Electrical Characteristics (T_A=-55 C to +200 C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Low Voltage	V_{OL}	V_{CC} = 5V,I_{OL}=2 mA	—	—	0.4	V
Input High Voltage[4]	V_{IH}		V_{CC} x 0.7		V_{CC} + 1	V
Input Low Voltage[4]	V_{IL}		-0.3	—	V_{CC} x 0.3	V
Input Leakage Current	I_{LI}	V_{IN} =0V to V_{CC}	-20	—	20	A
Output Leakage Current	I_{LO}	V_{OUT}=0V to V_{CC}, $\overline{CS}$=V_{CC}	-20	—	20	A

Power Supply Characteristics (T_A = -55 C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VCC Operating Current	$I_{CC}1$	Read at 10 MHz (V_{CC} = 5V)	—	—	5.0	mA
VCC Operating Current	$I_{CC}2$	Write at 5 MHz (V_{CC} = 2.5V)	—	—	3.0	mA
Standby Current	$I_{SB}1$	V_{CC} = 5.0V,V_{IN} =V_{CC} or GND $\overline{CS}$= V_{CC}	—	—	3	A
Standby Current	$I_{SB}2$	V_{CC} = 2.5V, V_{IN}=V_{CC} or GND $\overline{CS}$ = V_{CC}	—	—	2	A

Power Supply Characteristics (T_A = -55 C to +200°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VCC Operating Current	$I_{CC}1$	Read at 5 MHz (V_{CC} = 5V)	—	—	5.0	mA
VCC Operating Current	$I_{CC}2$	Write at 5 MHz (V_{CC} = 2.5V)	—	—	3.0	mA
Standby Current	$I_{SB}1$	V_{CC} = 5.0V,V_{IN} =V_{CC} or GND $\overline{CS}$= V_{CC}	—	—	180	A
Standby Current	$I_{SB}2$	V_{CC} = 2.5V, V_{IN}=V_{CC} or GND $\overline{CS}$ = V_{CC}	—	—	5.0	A

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AC Electrical Characteristics (T_A = -55°C to +150°C)

Parameter	Symbol	3.0V-5.5V Min	3.0V-5.5V Max	4.5V-5.5V[1] Min	4.5V-5.5V[1] Max	Units
SCL Clock Frequency	f_{SCL}	0	5	0	10	MHz
Input Rise Time	t_{RI}	—	2	—	2	s
Input Fall Time	t_{FI}	—	2	—	2	s
SCK High Time	t_{WH}	90	—	40	—	ns
SCK Low Time	t_{WL}	90	—	40	—	ns
CS High Time	t_{CS}	100	—	40	—	ns
CS Setup Time	t_{CSS}	90	—	40	—	ns
CS Hold Time	t_{CSH}	90	—	25	—	ns
Data in Setup Time	t_{SU}	20	—	15	—	ns
Data In Hold Time	t_H	30	—	15	—	ns
Hold Setup Time	t_{HD}	50	—	25	—	ns
Hold Hold Time	t_{CD}	50	—	25	—	ns
Output Valid	t_V	0	60	0	25	ns
Output Hold Time	t_{HO}	0	—	0	—	ns
Hold to Output Low Z	t_{LZ}	0	50	0	25	ns
Hold to Output High Z	t_{HZ}	—	100	—	25	ns
Output Disable Time	t_{DIS}	—	100	—	25	ns
Write Cycle Time	t_{WC}	—	5	—	5	ms

* Plastic Packaging only

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AC Electrical Characteristics (T_A = -55°C to + 200°C)

Parameter	Symbol	4.5V-5.5V[1] Min	Max	Units
SCL Clock Frequency	f_{SCL}	0	10	MHz
Input Rise Time	t_{RI}	—	2	s
Input Fall Time	t_{FI}	—	2	s
SCK High Time	t_{WH}	40	—	ns
SCK Low Time	t_{WL}	40	—	ns
CS High Time	t_{CS}	40	—	ns
CS Setup Time	t_{CSS}	40	—	ns
CS Hold Time	t_{CSH}	25	—	ns
Data in Setup Time	t_{SU}	15	—	ns
Data In Hold Time	t_H	15	—	ns
Hold Setup Time	t_{HD}	25	—	ns
Hold Hold Time	t_{CD}	25	—	ns
Output Valid	t_V	0	25	ns
Output Hold Time	t_{HO}	0	—	ns
Hold to Output Low Z	t_{LZ}	0	25	ns
Hold to Output High Z	t_{HZ}	—	25	ns
Output Disable Time	t_{DIS}	—	25	ns
Write Cycle Time	t_{WC}	—	5	ms

*Ceramic Packaging only

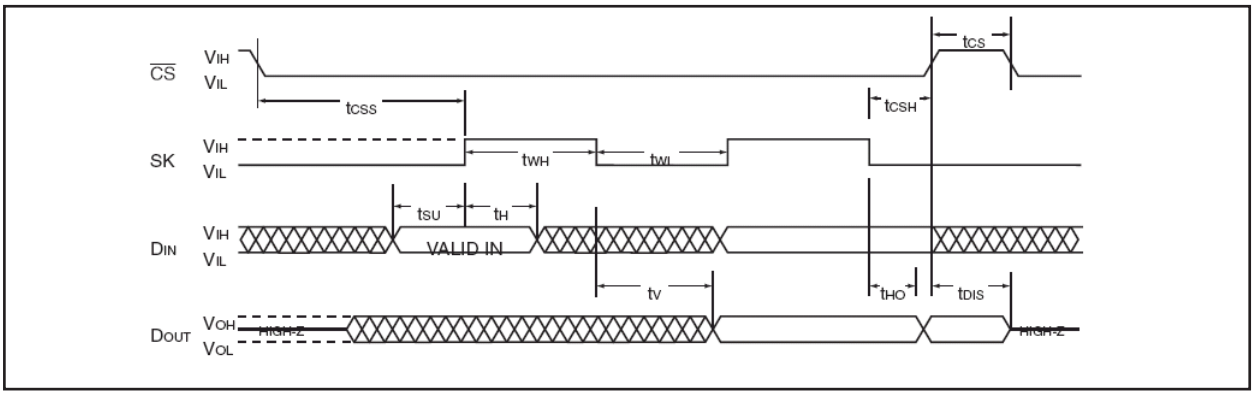

Figure 1. Synchronous Data Timing

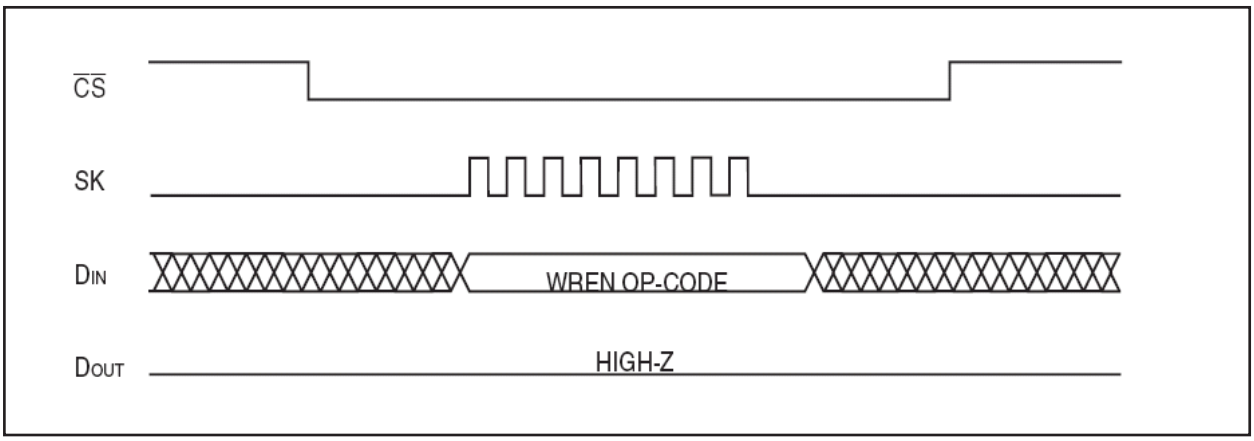

Figure 2. WREN Timing

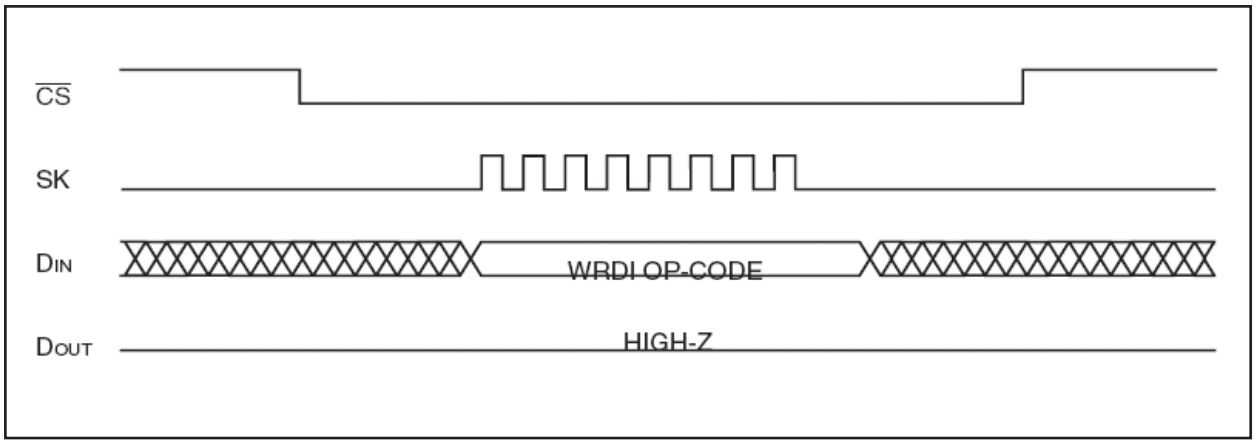

Figure 3. WRDI Timing

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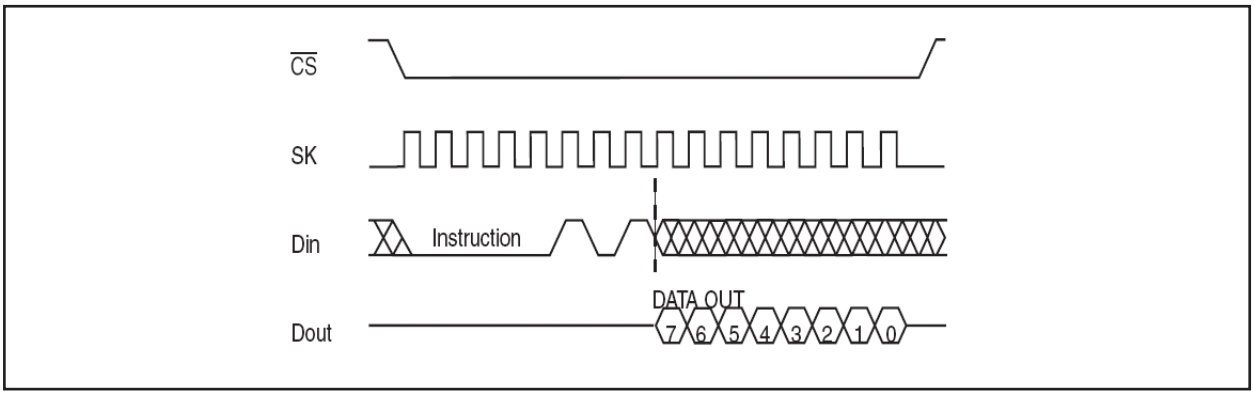

Figure 4. RDSR Timing

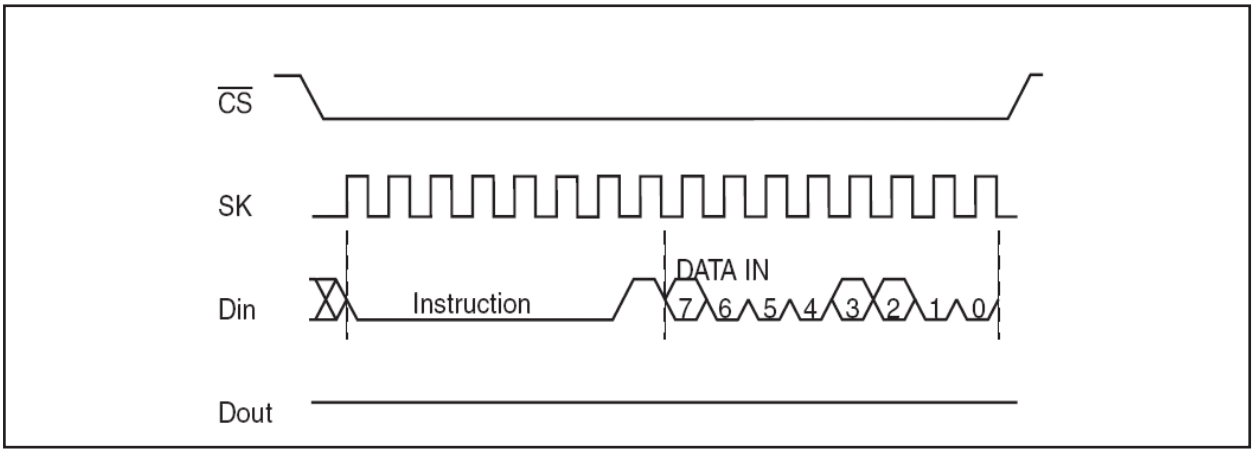

Figure 5. WRSR Timing

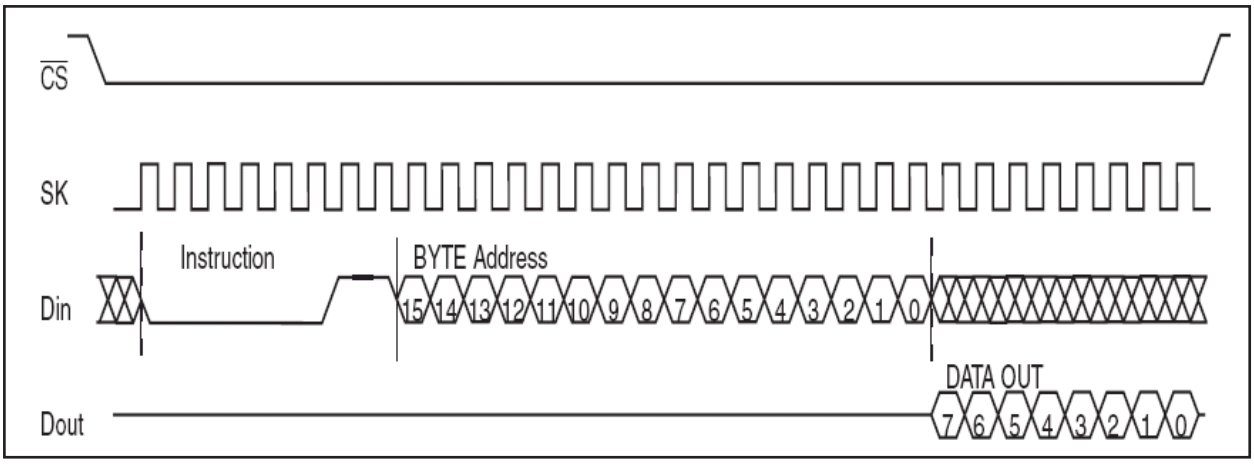

Figure 6. READ Timing

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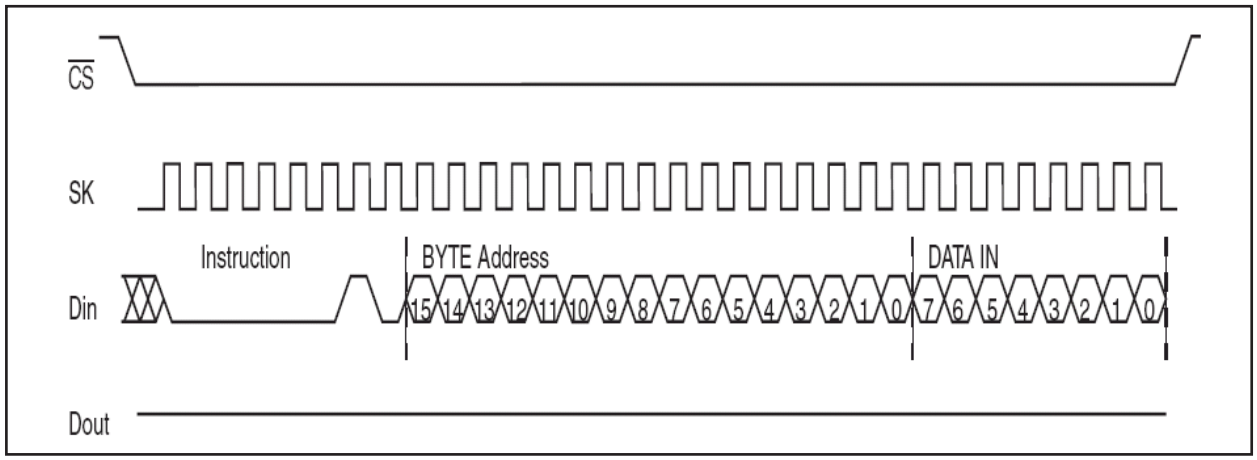

Figure 7. WRITE Timing

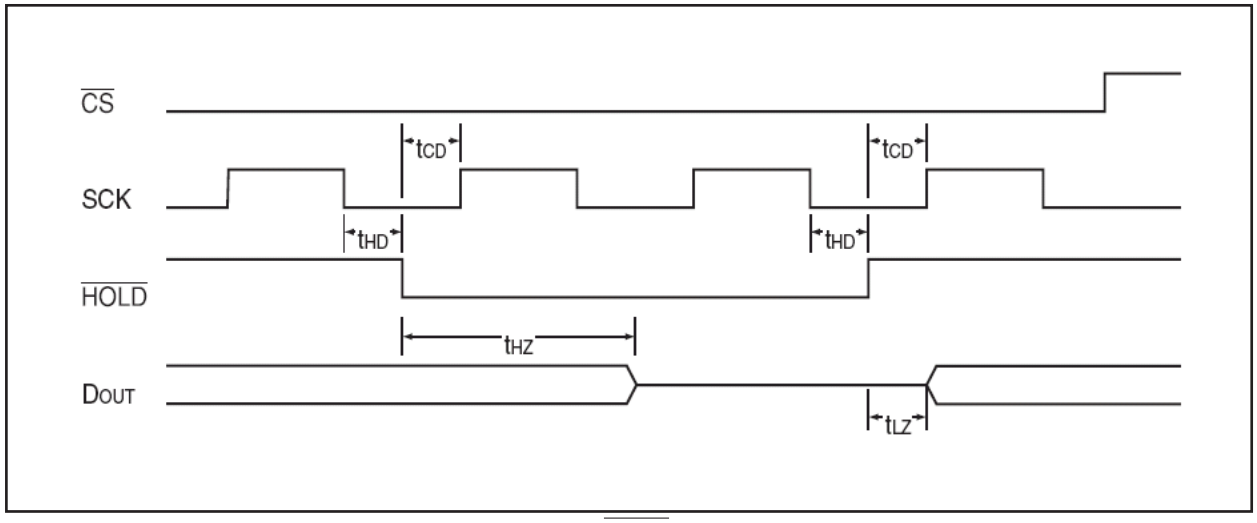

Figure 8. $\overline{\text{HOLD}}$ Timing

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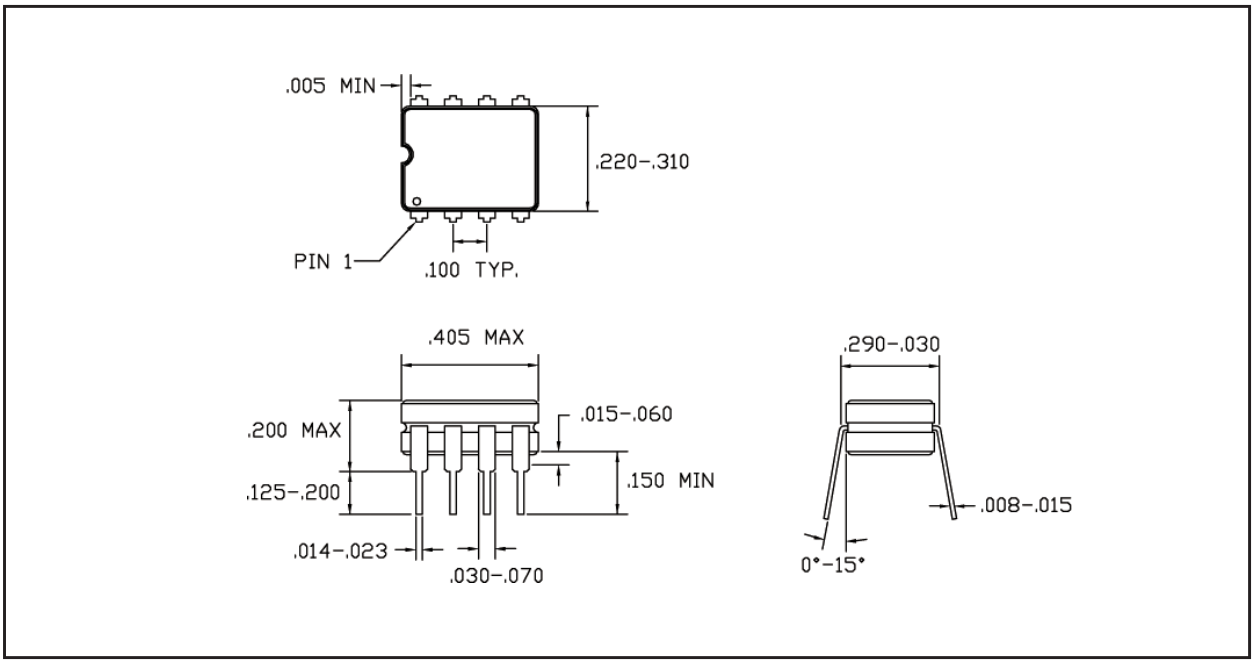

Figure 13. 8-pin CDIP package outline

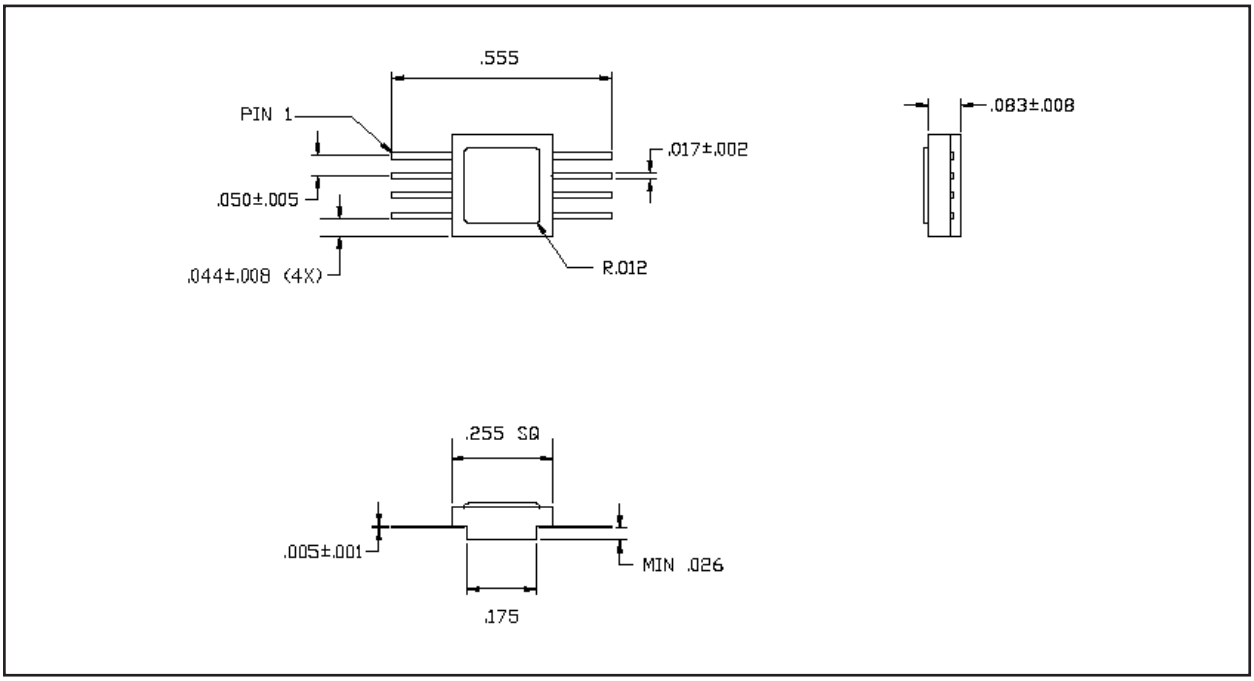

Figure 14. 8-pin Flatpack package outline

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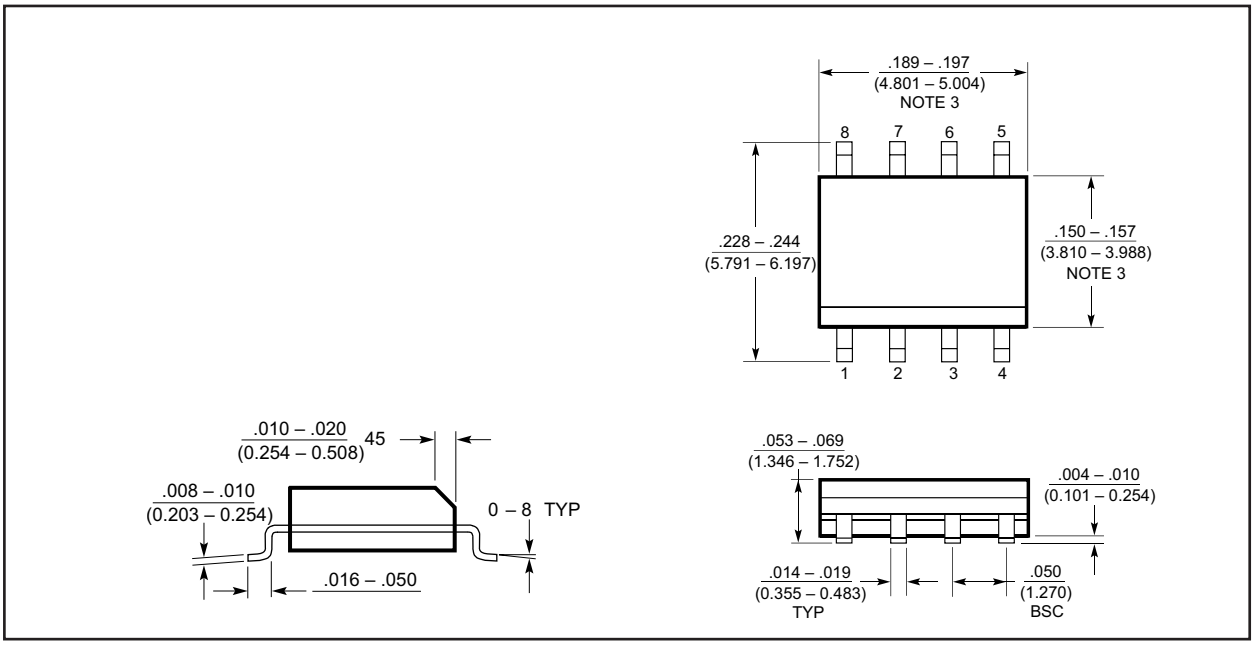

Figure 15. 8-pin SOIC package outline

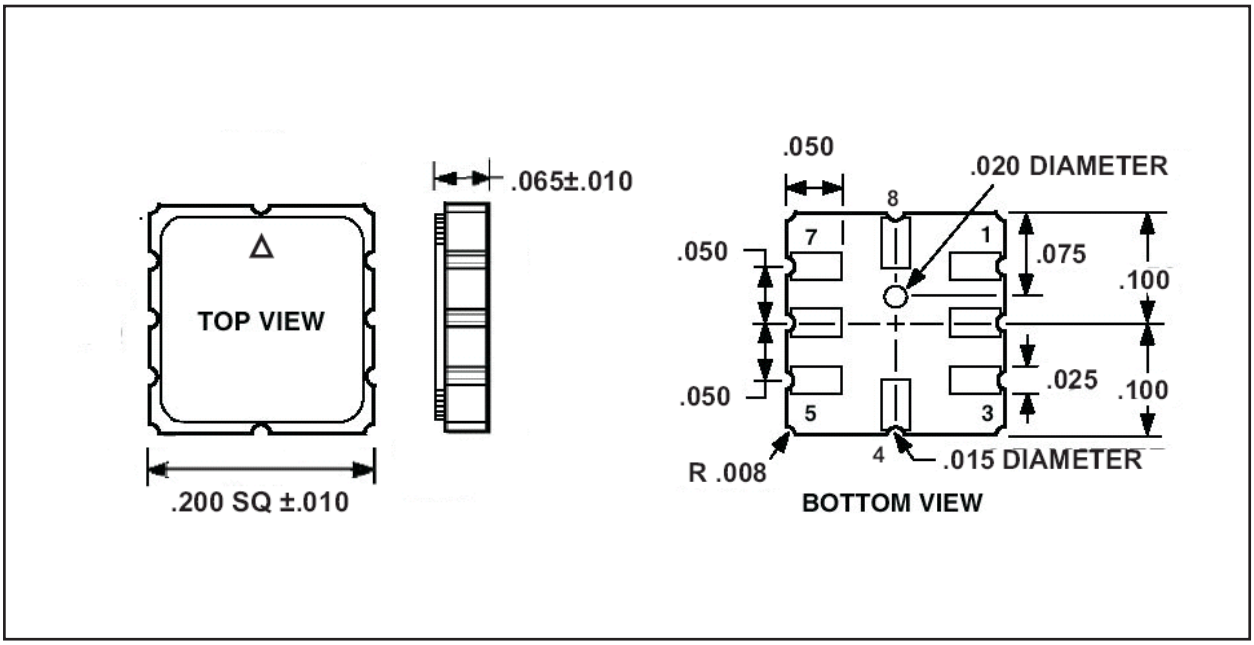

Figure 16. 8-pin LCC package outline

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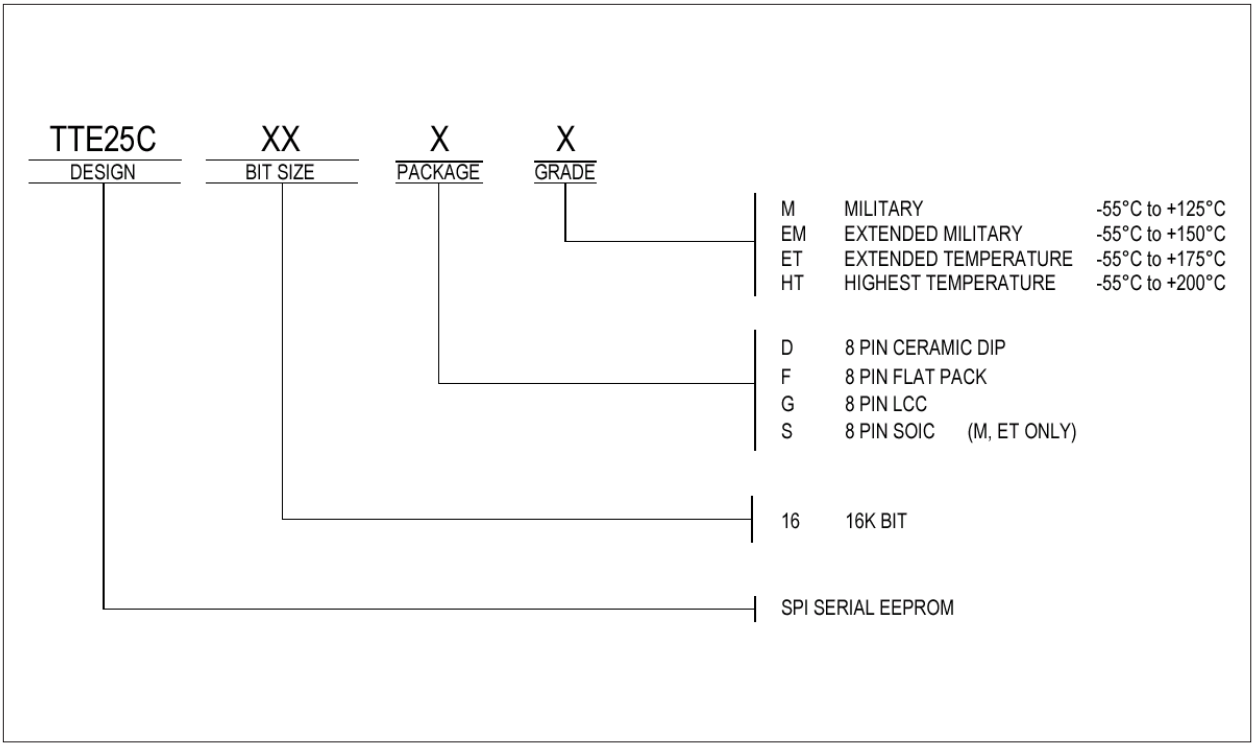

Figure 17. Order Information

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