FEATURES

-High-speed access time: 20,25, 35ns
-Low Active Power: 85mW (typical)
-Low stand-by power: 7mW (typical)
CMOS standby

-Single power supply
-V_{dd} 3.0V to 3.6V
-Fully static operation:no clock or refresh required
-Three state outputs
-Extended temperature support

Description

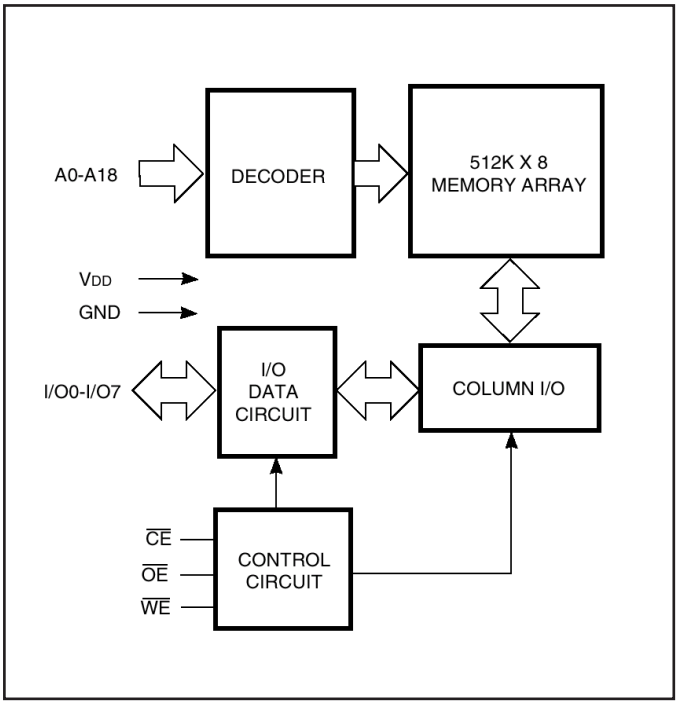
The TTS512WV8 is very high-speed, low power, 524,288-word by 8 bit CMOS static RAMs.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels. The TTS512WV operates from single power supply.

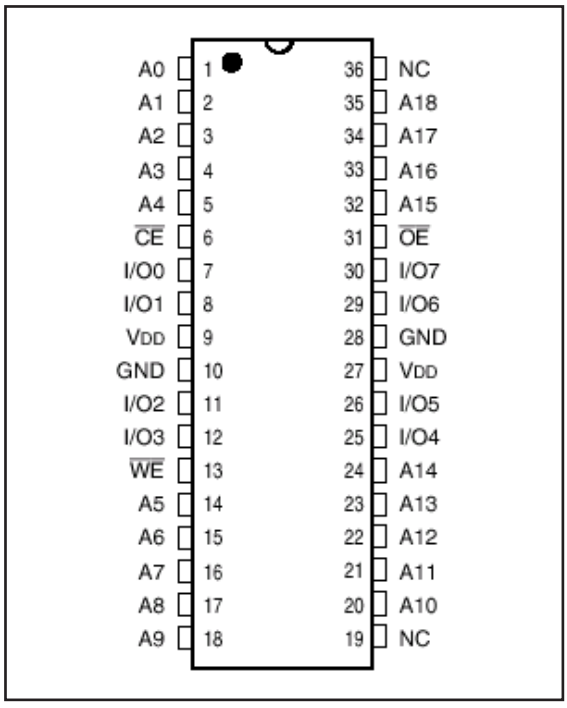
The TTS512WV is available in 36-pin SOJ, Ceramic LCC and DIP (ceramic or plastic) packages.

PIN DESCRIPTIONS

A0-A18	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Bidirectional Ports
V_{DD}	Power
GND	Ground
NC	No Connection



Function Block Diagram



Pin Configuration

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DC OPERATING CONDITIONS

V_{DD} = 3.3V 0.3V

Parameter	Symbol	Conditions	Min.	Max.	Units
Output HIGH Voltage	V_{OH}	V_{DD} = Min, I_{OH} = -4.0mA	2.4		V
Output LOW Voltage	V_{OL}	V_{DD} = Min, I_{OH} = 8.0mA	1.7	0.4	V
Input HIGH Voltage	V_{IH}		2	V_{DD} + 0.3	V
Input LOW Voltage[1]	V_{IL}		-0.3	0.8	V
Input Leakage	I_{IL}	GND VIN VDD	-1	1	A
Output Leakage	I_{LO}	GND VIN VDD, Outputs Disabled	-1	1	A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Units
Terminal Voltage with Respect to GND	V_{TERM}	-0.5 to V_{DD} + 0.5	V
VDD Relates to GND	V_{DD}	-0.3 to 4.0	V
Storage Temperature	T_{STG}	-65 to +150	C
Power Dissipation	P_T	1.0	W

INPUT/OUTPUT CAPACITANCE

(T_A = 25 C, f = 1 MHz, V_{DD} = 3.3V)

Parameter	Symbol	Conditions	Max.	Units
Input Capacitance	C_{IN}	V_{IN} =0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} =0V	8	pF

1. V_{IL}(min) = -0.3V DC; V_{IL} (min) = -2.0V AC (pulse width < 10 ns). Not 100% tested
2. V_{IH}(min) = V_{DD} +0.3V DC; V_{IH} (min) = V_{DD}+2.0V AC (pulse width < 10 ns). Not 100% tested

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TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	VDD Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

OPERATING RANGE (V_{DD})

(T_A = 25 C, f = 1 MHz, V_{DD} = 3.3V)

Range	Ambient Temperature	V_{DD}
Extended	-55C to +125C	3.0-3.6V

POWER SUPPLY CHARACTERISTICS[1]

				-20		-25		-35		
Parameter	Symbol	Conditions		Min	Max	Min	Max	Min	Max	Units
V_{DD} Dynamic Operating Supply Current	I_{CC}	V_{DD} = Max I_{OUT} = 0 mA, f = f_{MAX}	Mil Ext typ[2]	— — 45	65 90	— —	65 90	— —	50 80	mA
Operating Supply Current	I_{CC1}	V_{DD} = Max I_{OUT} = 0 mA, f = 0	Mil Ext	— —	60 90	— —	60 90	— —	40 55	mA
TTL Standby Current	I_{ISB1}	V_{DD} = Max V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ V_{IH}, f = 0	Mil Ext	— —	30 50	— —	30 50	— —	20 35	mA
CMOS Standby Current	I_{ISB2}	V_{DD} = Max $\overline{CE}$ V_{DD}- 0.2V V_{IN} V_{DD} - 0.2V or V_{IN} 0.2V, f = 0	Mil Ext Typ[2]	— — 10	20 35	— —	20 35	— —	20 30	mA

1. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency, f= 0 means no input lines change
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25 C and not 100% tested.

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AC TEST CONDITIONS

Parameter	Unit 3.0V-3.6V
Input Pulse Level	0V to 3V
Input Rise and Fall Times	1V/ns
Input and Output Timing and Reference Level (V_{REF})	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

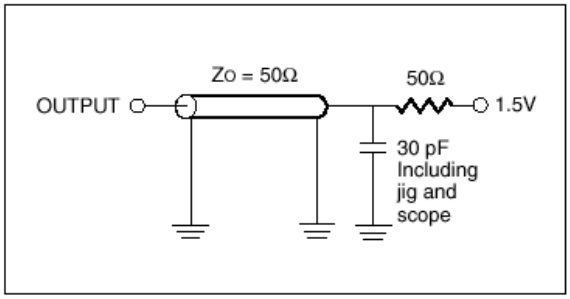

Figure 1.

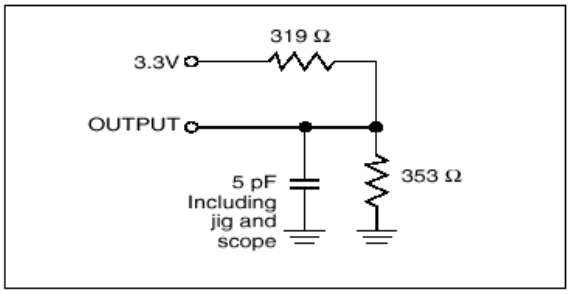

Figure 2.

READ CYCLE SWITCHING CHARACTERISTICS[1]

		-20		-25		-35		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Read Cycle Time	t_{RC}	20	—	25	—	35	—	ns
Address Access Time	t_{AA}	—	20	—	25	—	35	ns
Output Hold Time	t_{OHA}	2.5	—	4	—	4	—	ns
$\overline{CE}$ Access Time	t_{ACE}	—	20	—	25	—	35	ns
$\overline{OE}$ Access Time	t_{DOE}	—	8	—	12	—	15	ns
$\overline{OE}$ to High-Z Output	t_{HZOE}[2]	0	8	—	8	—	10	ns
$\overline{OE}$ to Low-Z Output	t_{LZOE}[2]	0	—	0	—	0	—	ns
$\overline{CE}$ to High-Z Output	t_{HZCE}[2]	0	8	0	8	0	10	ns
$\overline{CE}$ to Low-Z Output	t_{LZCE}[2]	3	—	10	—	10	—	ns
Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Power Down Time	t_{PD}	—	20	—	25	—	35	ns

1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.

2. Tested with load in Figure 1b. Transition is measured 500mV from steady-state voltage. Not 100% tested.

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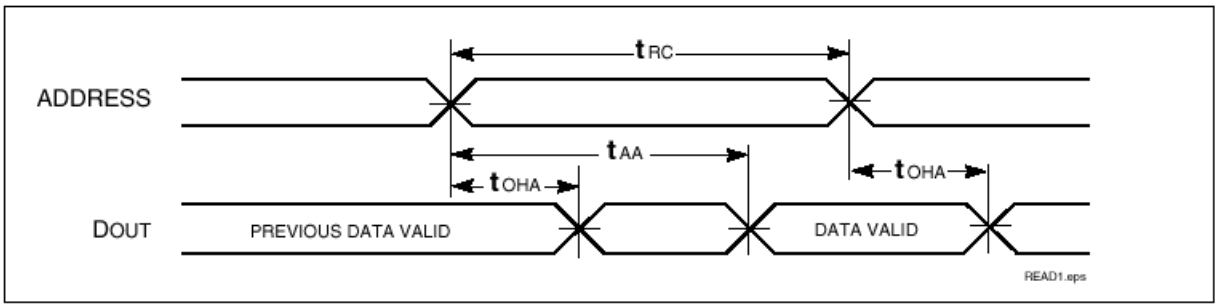
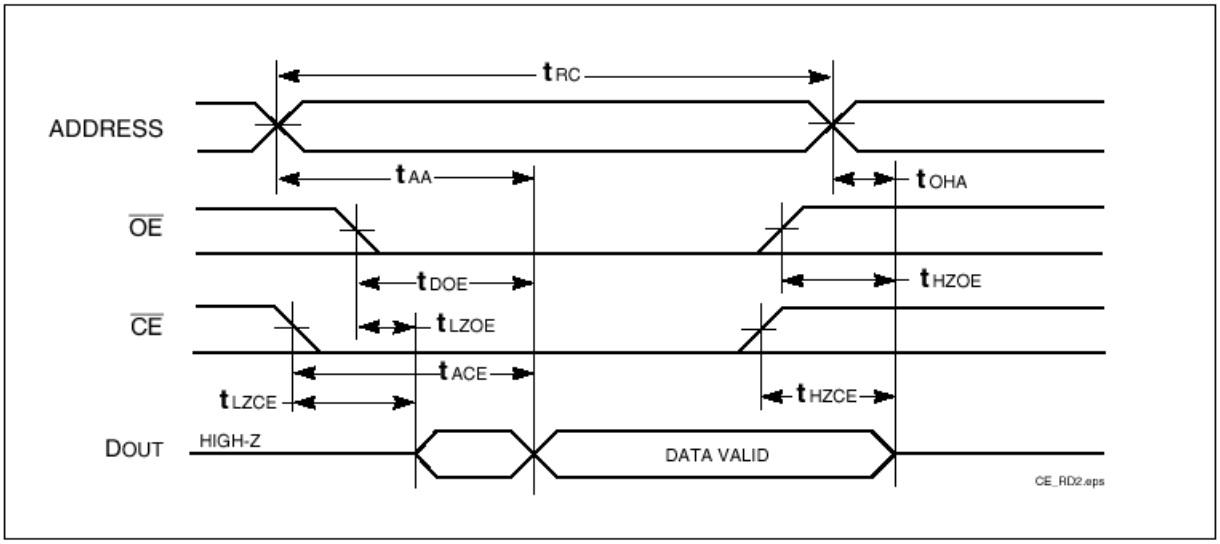
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = V_{IL})



READ CYCLE NO. 2[1,3] ($\overline{CE}$ and $\overline{OE}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

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WRITE CYCLE SWITCHING CHARACTERISTICS[1,2]

Parameter	Symbol	-20 Min	-20 Max	-25 Min	-25 Max	-35 Min	-35 Max	Units
Write Cycle Time	t_{WC}	20	—	25	—	35	—	ns
$\overline{CE}$ to Write End	t_{SCE}	12	—	18	—	25	—	ns
Address Setup Time to Write End	t_{AW}	12	—	15	—	25	—	ns
Address Hold from Write End	t_{HA}	0	—	0	—	0	—	ns
Address Setup Time	t_{SA}	0	—	0	—	0	—	ns
$\overline{WE}$ Pulse Width (OE = High)	t_{PWE}[1]	12	—	18	—	30	—	ns
$\overline{WE}$ Pulse Width (OE=Low)	t_{PWE}[2]	17	—	20	—	30	—	ns
Data Setup to Write End	t_{SD}	9	—	12	—	15	—	ns
Data Hold from Write End	t_{HD}	0	—	0	—	0	—	ns
$\overline{WE}$ LOW to High-Z Output	t_{HZWE}[3]	0	9	0	12	0	20	ns
$\overline{WE}$ HIGH to LOW-Z Output	t_{LZWE}[3]	3	20	5	—	5	—	ns

1. Test conditions TTS512WV8 assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3 and output loading specified in Figure 1a.

2. Tested with load in Figure 1b. Transition is measured 500mV from steady-state voltage. Not 100% tested.

3. The internal write time is defined by the overlap of CE LOW and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates and write.

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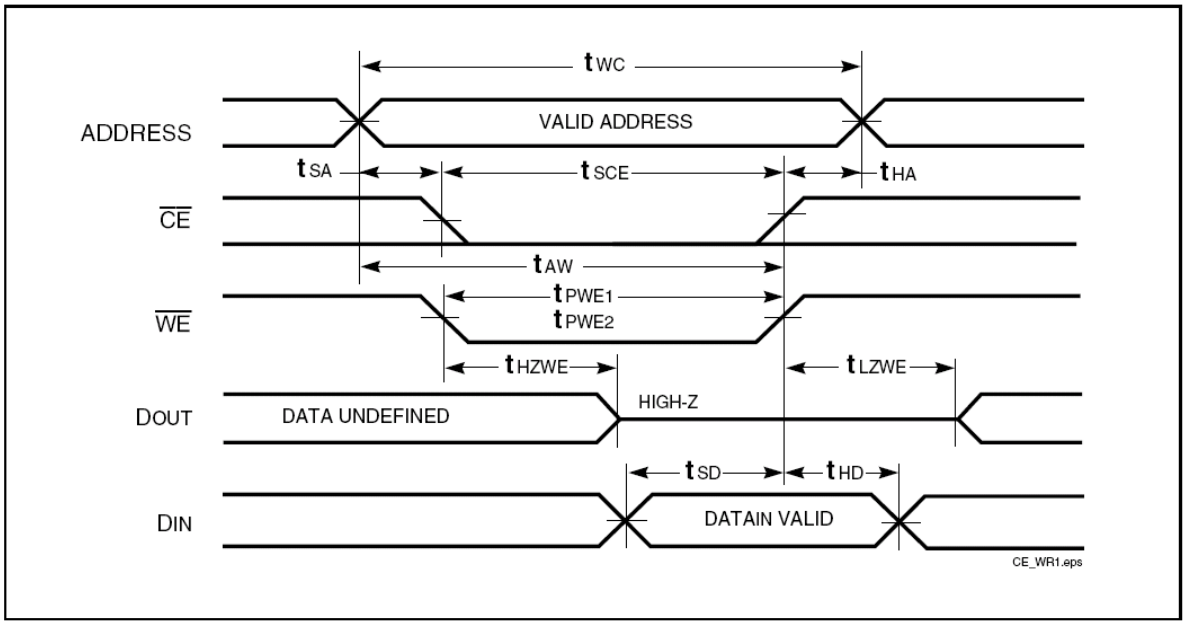
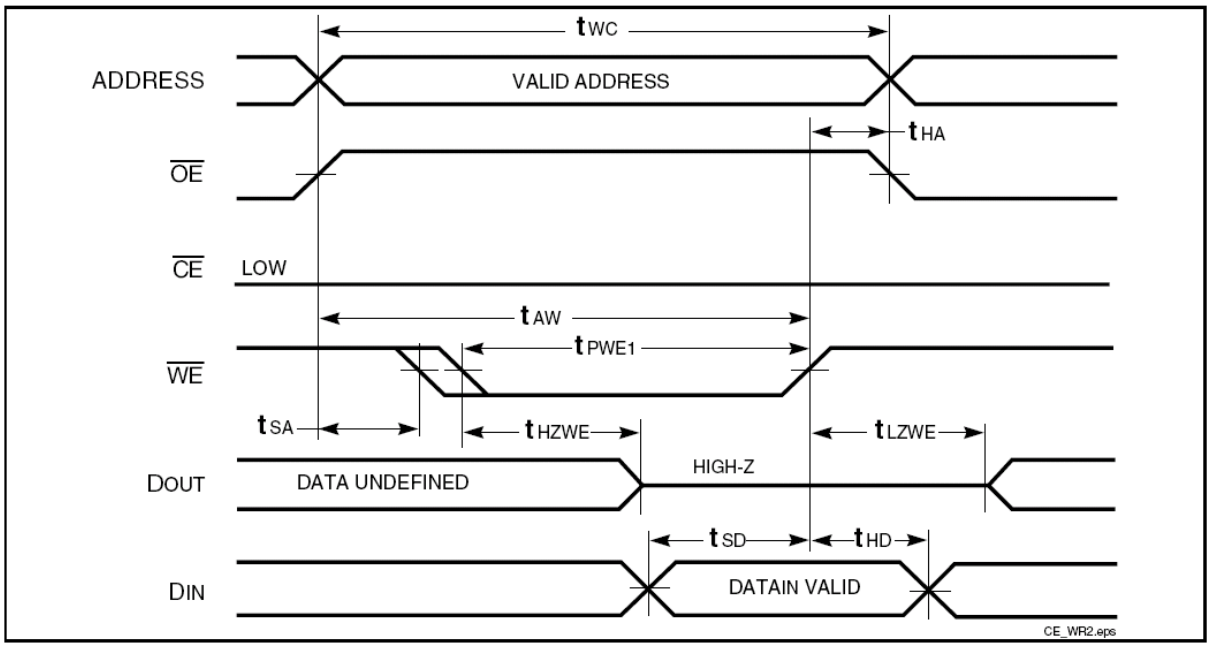
AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)



WRITE CYCLE NO. 2[1,2] ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ > V_{IH}.

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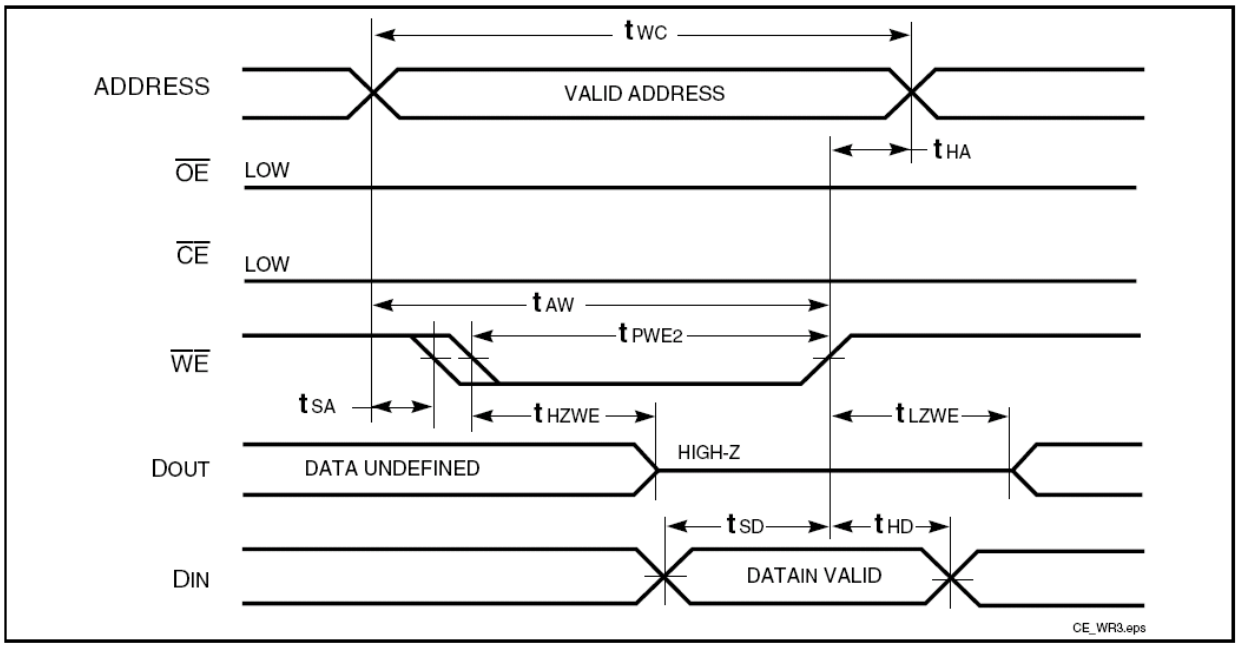
WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



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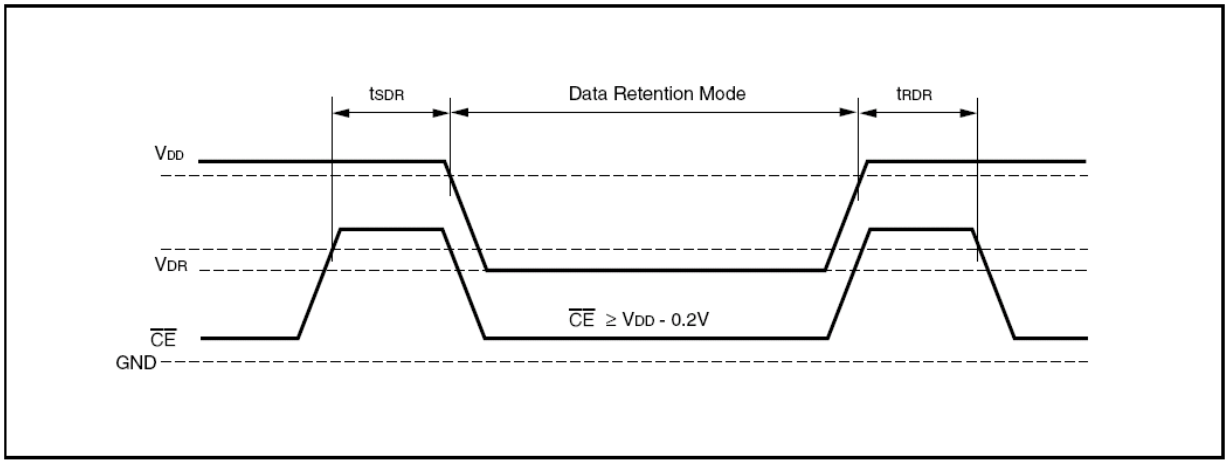
Data Retention Switching Characteristics

Parameter	Symbol	Test Condition	Options	Min	Typ[1]	Max	Units
V_{DD} for Data Retention	V_{DR}	See Data Retention Waveform		2.0	—	3.6	V
Data Retention Current	I_{DR}	V_{DD} = 2.0V, CE V_{DD} -0.2V	Mil. Ext.	— —	2 —	15 20	mA
Read Retention Setup Time	t_{SDR}	See Data Retention Waveform		0	—	—	ns
Recovery Time	t_{RDR}	See Data Retention Waveform		t_{RC}	—	—	ns

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



1.Typical values are measured at V_{DD} = 3.0V, T_A = 25 C and not 100% tested.

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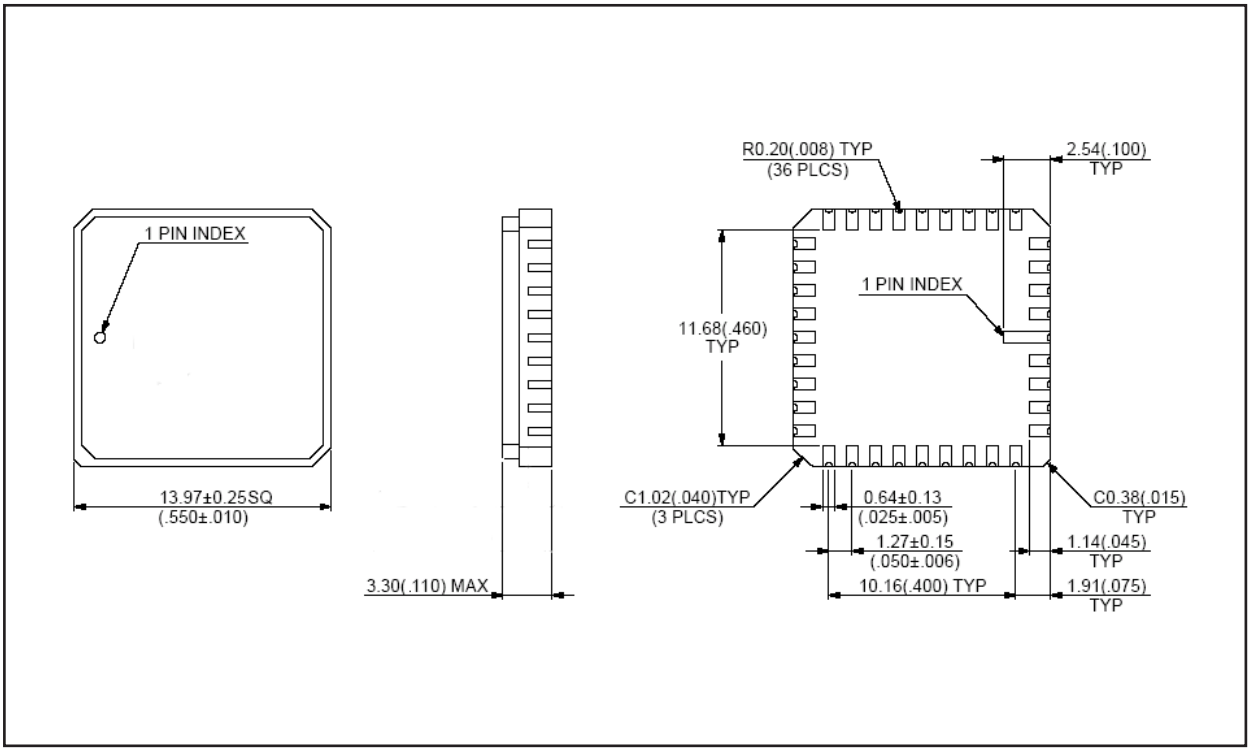

Figure 1: 36 Ld LCC Package

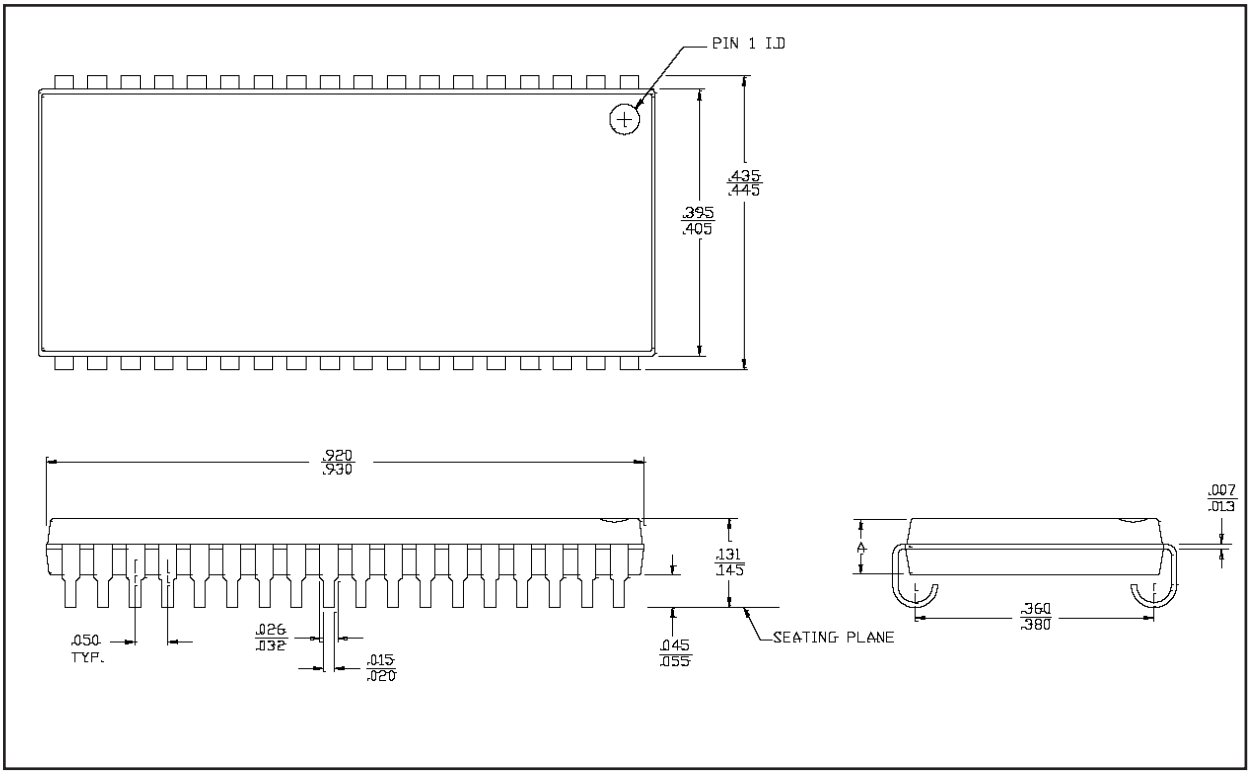

Figure 2: 36 Ld SOJ

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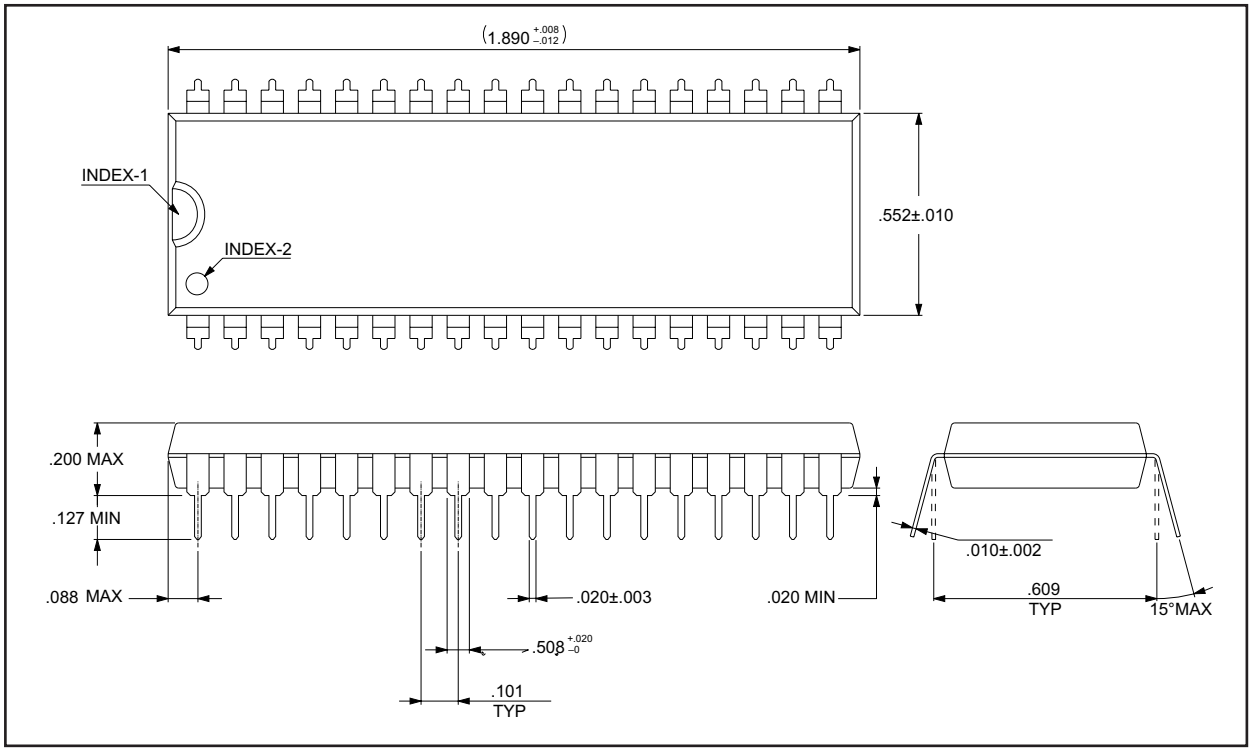

Figure 3: 36 Ld Plastic DIP

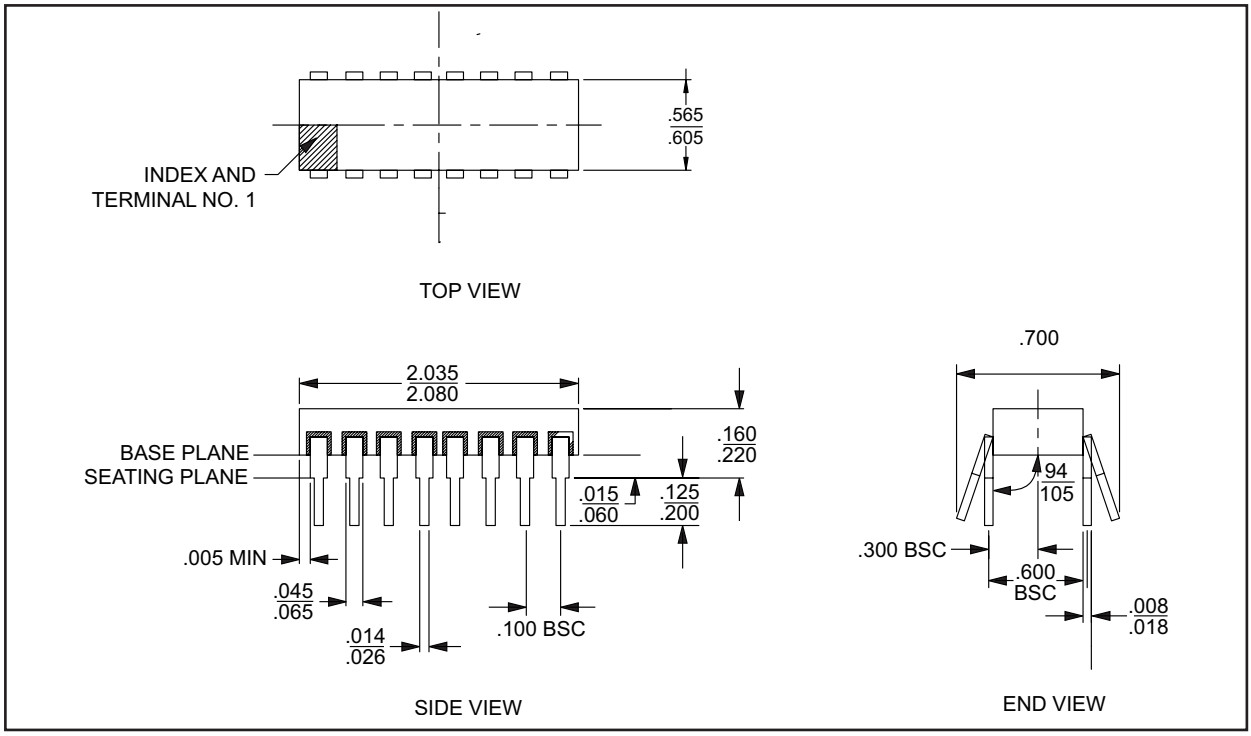

Figure 4: 36 Ld Ceramic DIP

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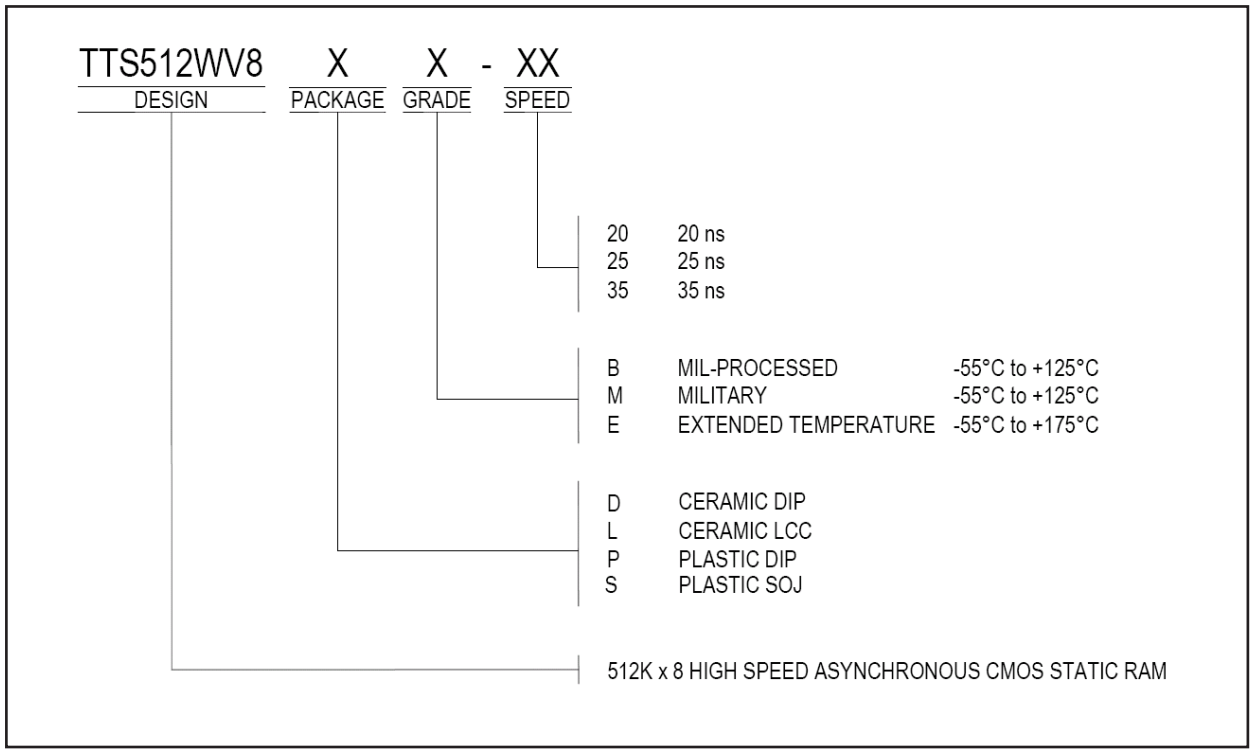

Figure 5: Ordering Information