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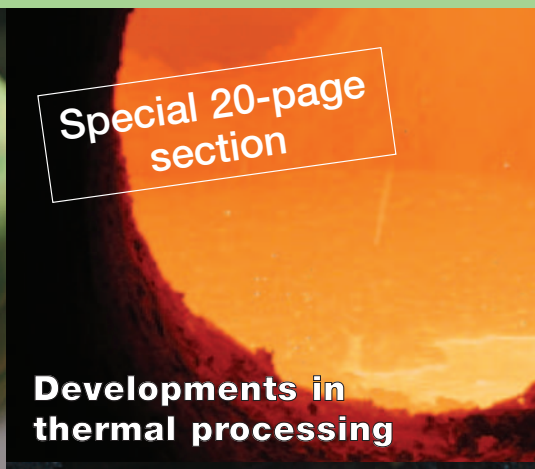
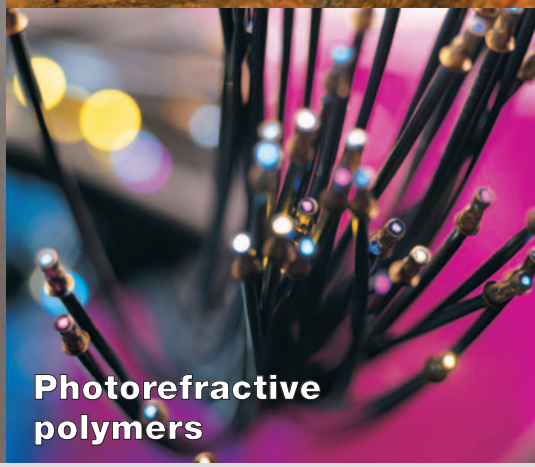
Microsurgery for microchips



Special 20-page section

Developments in thermal processing

Groundhog day



Photorefractive polymers

Also in this issue: ■ Active disassembly ■ Flying eye ■ Brazilian diamond renaissance ■ New Ti technology ■ Microtopography ■ PD News, including Diary of Courses ■ Focus on materials analysis, microscopy, metallography, image analysis and processing.

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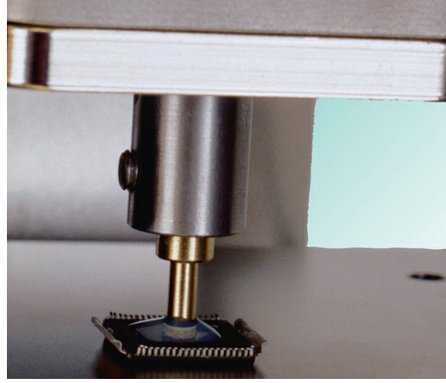
Microsurgery for microchips - new techniques for sample preparation



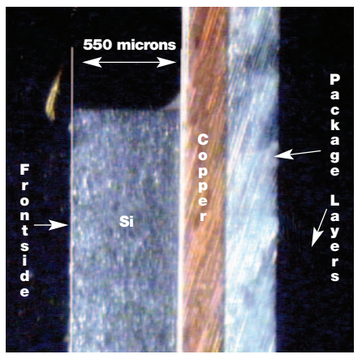
A standard selected area preparation system uses a small rotating tool, oscillating within a predefined amplitude to produce a cavity within the chip before polishing the surface.

Tim Hazeldine and Kim Duong discuss the main sample preparation disciplines required for electronic failure analysis, and the ways in which mechanical preparation equipment has evolved to meet the challenges offered by the complex set of materials that form the modern integrated circuit.

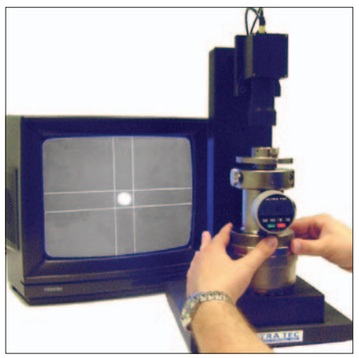
The seemingly unquenchable thirst of semiconductor manufacturers for faster and more powerful microchips puts great demands on the semiconductor manufacturing processes required. The increasing use of 300mm (12 inch) diameter silicon wafers that offer improved production yields, coupled with the dizzying increase in the number and packing density of transistors on each dice further increases the demand on materials, chemical and mechanical engineers to provide accompanying scaleable process solutions.

To achieve the necessary processing performance speeds, circuitry in modern integrated circuits (ICs) is produced by applying multiple layers of metallisation – six to eight metal layers is becoming increasingly common. This again raises the bar for production and consequently for the failure analyst whose job it is to find sub-micron defects hidden within the maze of circuitry.

Key to the failure analysis (FA) field are techniques that are the long standing preserve of the materials engineer – precision sawing, lapping and polishing. However, FA personnel typically have an electronic engineering (ie not materials) background and need specific training to adopt a mechanical/hands-on mindset. Also of importance to the field is the availability of a new toolkit of sample preparation and analysis equipment that offers the sensitivity required to reveal such tiny defects.



Cross-section of a semiconductor package – annotated to show typical layer types and thicknesses.



Optical tools such as an ultracollimator allow for increased parallelism of the sample during topside deprocessing.

Precision sawing

The production of quality cross-sections on package-, wafer- and board-level devices generally starts with a saw cut. The precision sawing operation dictates the resultant level of surface damage and the level of surface features that are retained. The resulting surface may be an end in itself – a good sawed surface offers sufficient information for generating a selected area preparation process – or the starting point for polishing.

By optimising the control of all parameters that affect cut quality, precision saws achieve a match of performance and cost-effectiveness. Saws range from a manually-fed trim saw to an advanced Z-spindle semi-automatic unit that allows for multiple passes and precise height control. Systems should feature coolant provision for enhanced surface finishes, together with feed and speed controls.

Cross-sectioning

Successful cross-sectioning techniques maintain the important information within the die or package, while being sufficiently controllable and reproducible so as to reveal the required features. Non-encapsulated cross-sectioning, particularly on die-level devices, is faster and easier to perform than encapsulated techniques, and can yield suitable results for SEM and TEM analysis.

Product offerings for cross-sectioning encompass manual techniques, through to semi-automatic approaches, with advanced wedge angle and low-inertial sample loading controls. These systems suit both encapsulated and non-encapsulated sample types. Techniques are available for the various key process steps of precision sawing, grinding and polishing that allow for low-relief preparation of materials of often widely disparate hardness and other mechanical properties.

Deprocessing

As electronic device sizes become smaller, the deprocessing operation becomes more exacting. During the last few years, metallisation layers have moved into the sub-micron realm. This means that the one-micron resolution limit available with mechanical indicators has become essentially obsolete.

Methods have been developed that ensure sub-micron parallelism of the device under preparation can be maintained – even down to 0.1 microns for die sizes less than 9mm.

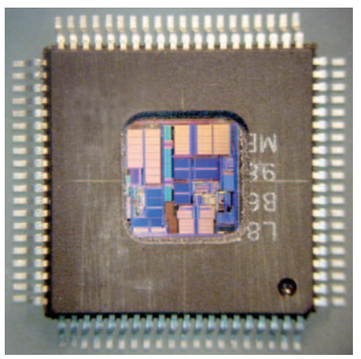
To tackle the other key weakness of previous (metallurgical-polisher based) systems in the marketplace – namely sample edge rounding – a true flat lapping bench-top CMP approach is used. This uses a harder, zero-nap, polyurethane-based pad material, which improves the overall flatness and removes edge rounding.

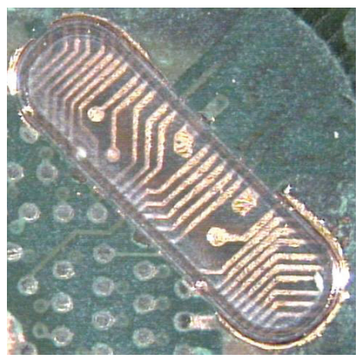
The majority of mechanical deprocessing relies on a skilled analyst working with manual polishing tools. Cost-effective manual tools are available for use with manual polishing stations and provide a no-frills polishing consistency.

Decapsulation

Topside decapsulation (analysis that is carried out on the circuitry populated side of the wafer material) using primarily chemicals is a well-established application that is carried out with manual protocols, or more frequently with automated acid etch systems. These methods produce fast and effective results on standard plastic packaged parts. However, several factors make acids incapable of processing all package styles. For instance, when the package contains materials that are slow or impossible to remove with acids, or when the total packaging cross-sectional thickness is large (this exacerbates the non-directionality of the acid attack and potentially leads to harmful corrosion of the bond pads and wires) it has been found that initial mechanical decapsulation offers key advantages.

After discovering an increasing number of decapsulation applications that benefit from initial mechanical operations, dedicated processes based on the selected area preparation product platforms have been developed for MCM, stacked die CSP/MCPs and power devices. These systems provide control of all required parameters to increase electrical survivability and yield in many decapsulation applications.





Electronic package after mechanical decapsulation and a 10 second chemical etch reveals the topside circuitry ready for analysis, left. Precisely milled sections of multi-layer PCBs allow for electrical connection of circuitry that would ordinarily be unreachable, right.

Backside analysis

The increasing number of metallisation layers used in modern ICs, which physically block the view of microscopes from seeing faults and point defects, has caused frontside techniques to become inadequate for complete failure analysis. Backside imaging, ie imaging through the silicon substrate, allows access to all the transistors (which are implanted in a single layer into the silicon wafer) within an IC and so can complete the analytical picture.

Backside imaging is possible as pure silicon is transparent at near infra-red (NIR) wavelengths. Dopants, which are added to the silicon substrate to alter electronic

Typical backside image without anti-reflective coat, left. Same area of sample after antireflective coating, right.

characteristics of the wafer, reduce this transparency. This means that to image a modern die effectively with a backside microscope generally requires the planar thinning of the wafer from a nominal 500 micron starting thickness, down to 80 microns or less, followed by polishing.

Backside microscopy is a highly evolving field that encompasses emission microscopes, with silicon CCD, or compound semiconductor detectors. More frequently laser scan methods are also being used to find still smaller defects by a characteristic generation of light, voltage/current change or thermal changes, which sets the defective site apart from areas behaving normally. Focussed ion beam (FIB) equipment is also being used to make topside and backside circuit modifications by overlaying the backside image over the part's circuit diagram.

For backside analysis, package-level applications generally require the decapsulation, thinning and polishing of a selected area. However, the circuit can remain electrically intact after preparation.

Backside selected area preparation

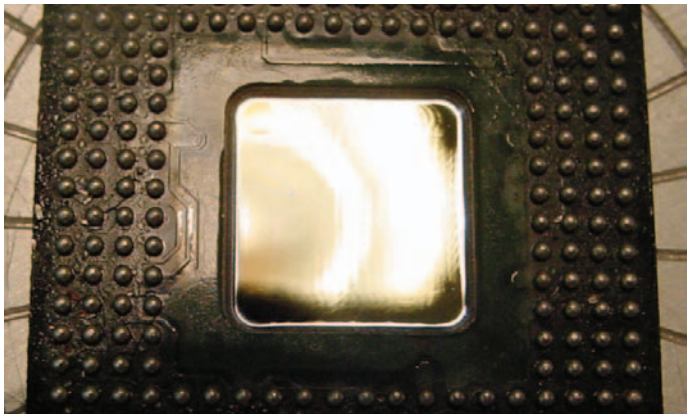
To enable backside analysis on packaged or encapsulated dice requires decapsulation and heat sink milling prior to substrate thinning. Processes have been developed that allow for effective low damage backside preparation techniques for dice of all sizes, with all encapsulation techniques.

After producing a mirror polish on the decapsulated and substrate-thinned package/die, the resulting sample may be backside imaged under NIR illumination. However, the glare from the polished surface reflected into standard objective lenses means that good image contrast is impossible. The addition of an antireflective coat (ARC) provides improved contrast, as well as a significant increase in the photon efficiency evident from the emission sites, which improves the overall sensitivity of the microscope. Until recently, ARC required expensive sputtering equipment and subsequent baking at highly elevated temperatures.

After extensive research and development to optimise the entire backside sample preparation process, a technology solution is now available that puts quality ARCs within easy reach of every sample preparation laboratory. The technology solution, dubbed ARC-lite, offers a fast (less than one minute), one-step, room temperature, chemical process that can be modified by the user to enhance coatings for various observation wavelengths. The range of imaging fluids available includes a standard solution and also a highly thermal stable 'FIB friendly' solution.

Due to the continued evolution of semiconductor manufacture, the sample preparation of electronic materials in packaged and wafer forms is increasingly challenging. Metallurgical-grade equipment no longer provides the flatness and parallelism results required to delineate layers of modern circuitry for frontside applications. The required finishes are achieved by use of true flat lapping equipment and optical measurement tools.

In backside applications, the use of selected area preparation systems enables total access to the circuitry for 'through the wafer' analysis, which continues to grow as an important primary analysis method.



BGA package after thinning and mirror polishing. Thinning the silicon substrate to under 80 microns allows for the backside microscope to image circuitry under infra red illumination.

Acknowledgements

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Further reading

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