FOUNDRY LEADERSHIP FOR THE SoC GENERATION

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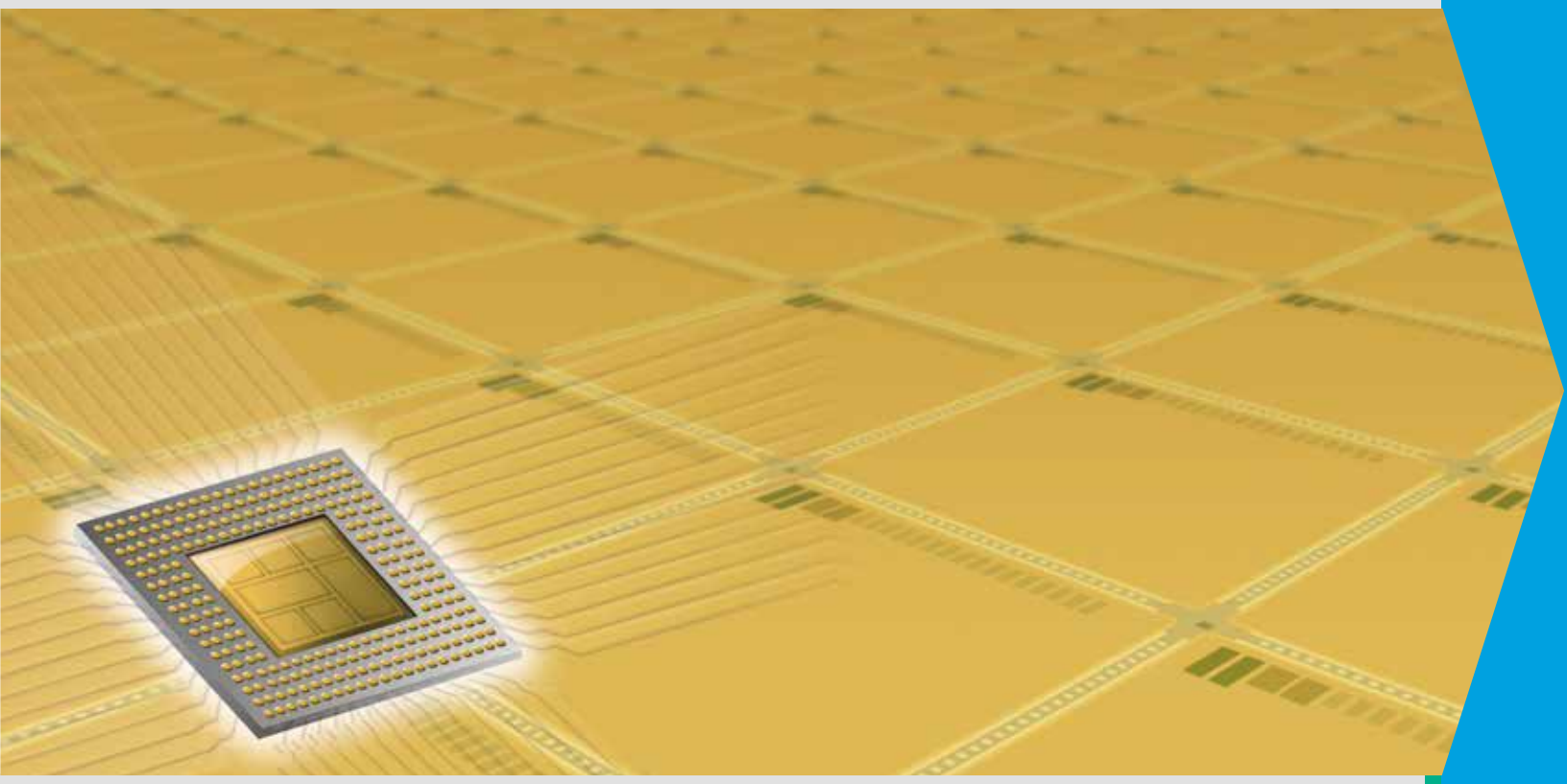
65 Nanometer

65



UMC

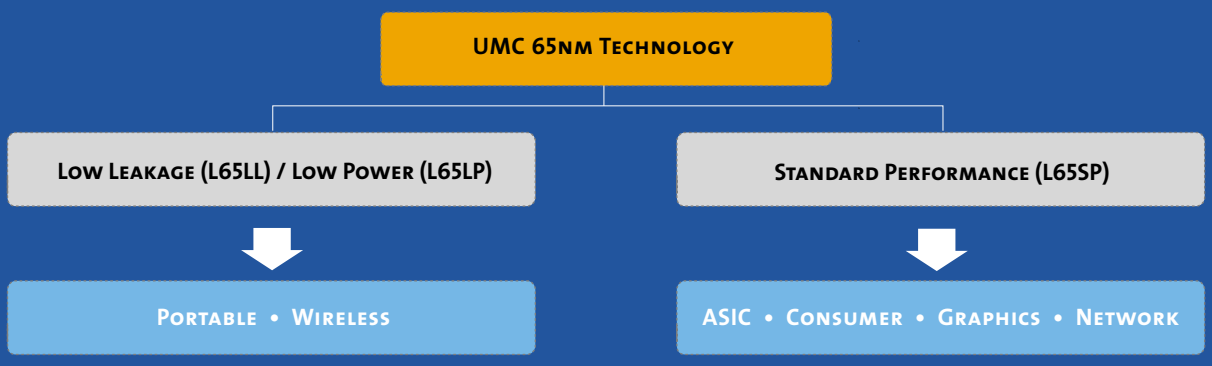
65 Nanometer

UMC is the foundry leader in 65nm process technology, having delivered the foundry industry's first 65nm customer products in June of 2005. UMC's 65-nanometer SoC solution begins with a flexible technology design platform. Customers are able to choose the process device options that are optimized for their specific application, such as Standard Performance (SP), Low Power(LP) or Low Leakage (LL) transistors. The high performance characteristics of UMC's 65nm SP process enable designers to utilize the technology to power a broad range of applications from consumer products to graphics ICs. Technology options can then be implemented including mixed signal/RFCMOS and embedded memories to further customize the process.

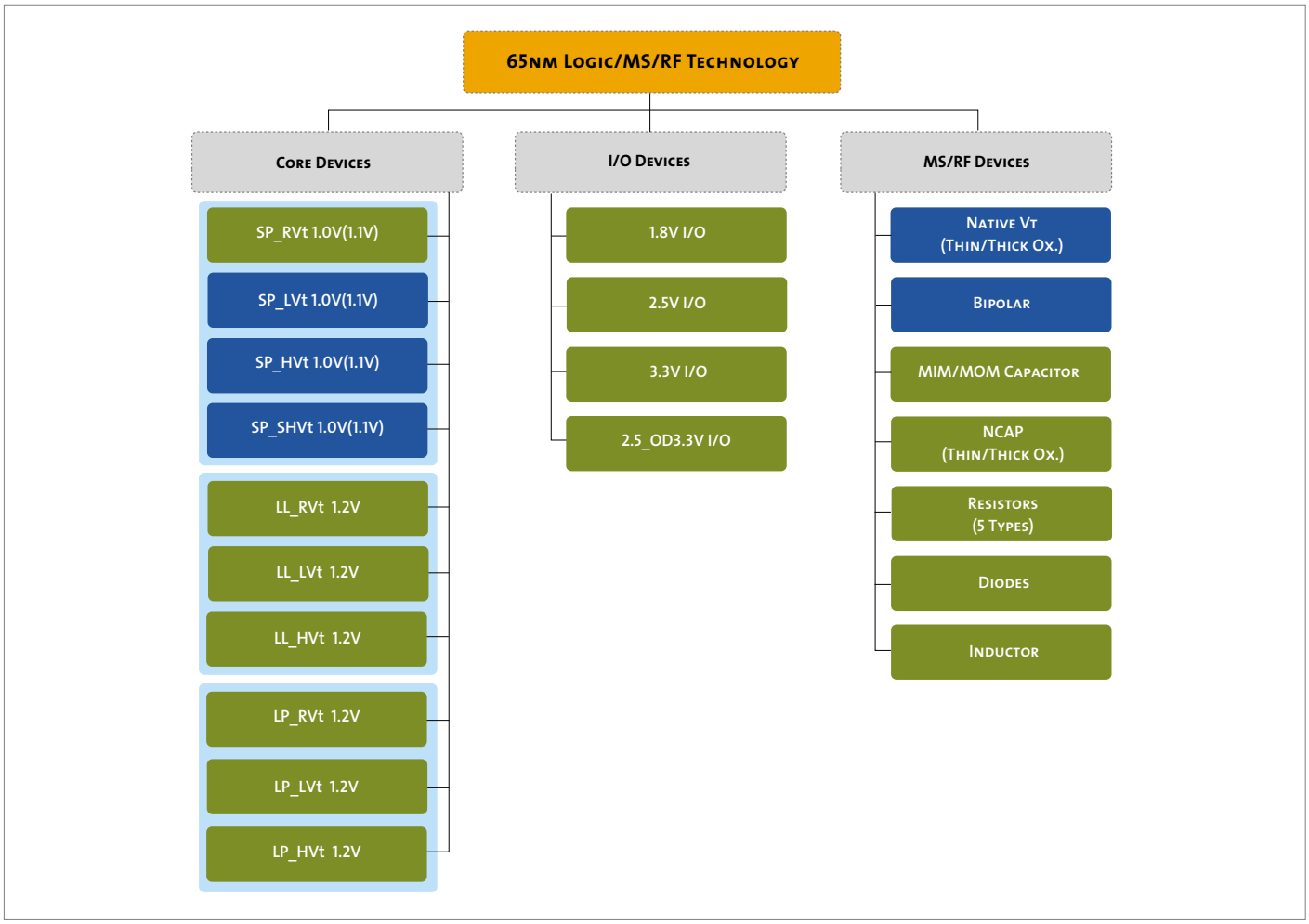
65nm Key Features

- *Integrated flows for logic, Mixed-Signal/RF*
- *6T/8T e-SRAM bit cells; URAM™ option (0.12um²)*
- *e-Fuse option*
- *Shallow trench isolation*
- *Retrograde twin well (Triple well option)*
- *193nm litho for all critical layers*
- *Enhanced nitrided gate oxide*
- *40nm min. poly length*
- *Multiple Vt options*
- *NiSi process*
- *Mobility enhancement techniques*
- *1P10M Cu/Low K (K=2.9)*
- *BOAC (Bonding Over Active Circuit)*
- *Wire Bond/Flip Chip option*

Technology to Meet Broad Applications



65nm Logic/MS/RF Devices



SP: Standard Performance LL: Low Leakage LP: Low Power ■: RF Model Available (LL and SP)

Silicon Verified IP Solutions

UMC offers comprehensive design resources that enable our customers to fully realize the advantages of UMC's advanced technologies. UMC's silicon verified fundamental IPs (standard cells, I/Os, and memory compilers) help customers easily migrate their designs to the next process generation to realize significant performance advantages while also reducing die size.

Customers can also leverage application specific IPs that are specialized for all types of mainstream applications such as digital TVs, cellular baseband controllers, digital cameras, and audio players to overcome time-to-market challenges.

Fundamental IP Support for SoC Designs

UMC offers comprehensive design resources that support our 65nm process technology. Silicon verified fundamental IPs (standard cells, I/Os, and memory compilers) optimized to UMC technologies are available free-of-charge from several leading vendors. Customers can also leverage application specific IPs for DTV, video/audio, etc. IPs available through UMC are DFM (Design for Manufacturing) compliant for better manufacturability.

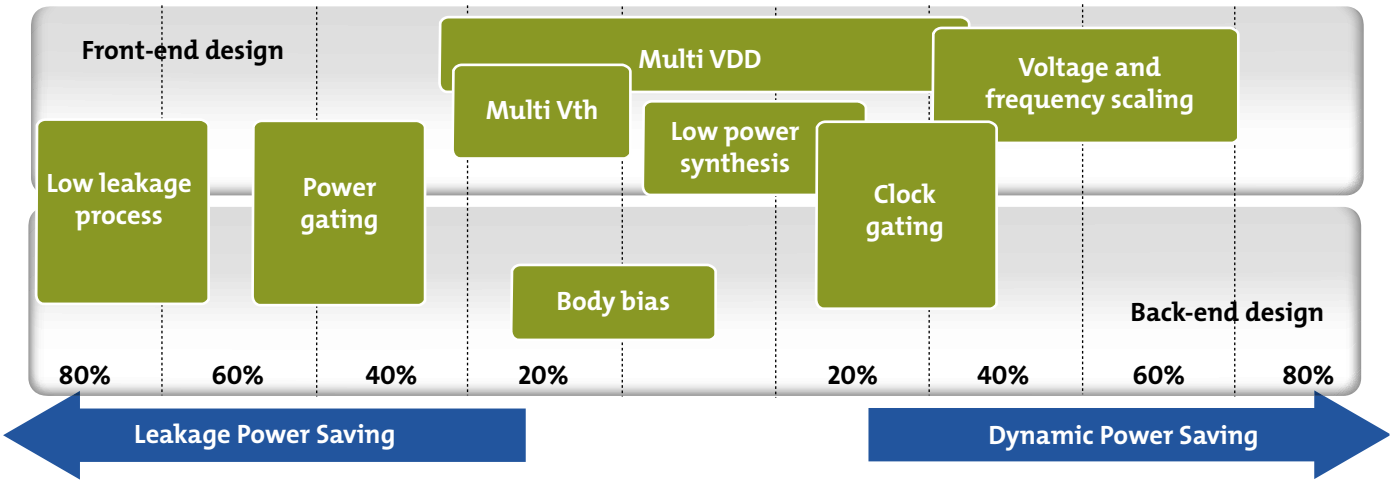
Library Provider		65nm						
		Faraday	VIRAGE		ARM	UMC		
Library		LL	SP	LP	SP	SP	LL	LP
Standard Cells	LVT					✓	✓	
	RVT				✓	✓	✓	✓
	HVT				✓	✓	✓	✓
I/O	1.8Vdd					✓	✓	
	3.3Vdd						✓	
	2.5V / 3.3V				✓	✓	✓	
	1.8V / 2.5V / 3.3V					✓	✓	✓
Single Port SRAM Compiler		✓	✓	✓	✓			
Dual Port SRAM Compiler		✓	✓	✓	✓			
Single Port Register File		✓	✓	✓	✓			
Dual Port Register File		✓	✓	✓	✓			
ROM Compiler		✓	✓	✓	✓			

Low Power Features of Standard Cell Library

With today's proliferation of low power applications, lowering energy consumption without sacrificing performance has become a critical concern for designers of power management chips for portable electronics. UMC supports its standard cell library with low power design features, including multiple Vt, clock-gating, level shifter and other features to complement UMC's complete low power solution.

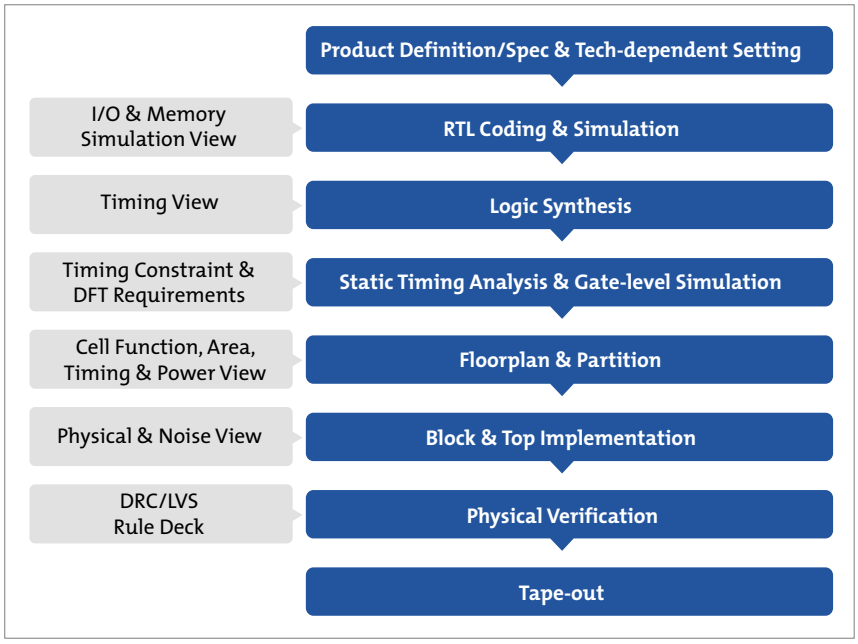
Type		Support Features		Support				
				28nm	40nm	65nm	90nm	0.13um
Operating Power	Voltage Island & Scaling	Level Shifters w / Insulator	Power & Timing Model @ 80% of Vdd	√	√	√	√	√
	Clock Gating & Frequency Scaling	Clock Gated F/F		√	√	√	√	√
Leakage Power	Multi-Vt	Multi-Vt cells		√	√	√	√	√
	Power Gating	Isolation cells, Retention F/F Headers / Footers, etc.		√	√	√	√	√
	Body Bias	Tapless cells	Timing / Power Model	√	√	√	√	√

Low Power Design Support



UMC Reference Design Flow

UMC Reference Design Flow provides a design methodology and flow validated with a "Leon2" system demonstration board. The flow incorporates 3rd-party EDA vendors' baseline design flows to address issues such as timing closure, signal integrity, leakage power and design for manufacturability and adopts a hierarchical design approach built upon silicon validated process libraries. UMC Reference Design Flow covers from schematic/RTL coding all the way to GDS-II generation and supports Cadence, Magma, Mentor and Synopsys EDA tools. All of these tools have been correlated to UMC silicon and can be interchanged for added flexibility.



SYNOPSYS®

Mentor Graphics®

cadence®

Reference Design Flow and Vendor Support

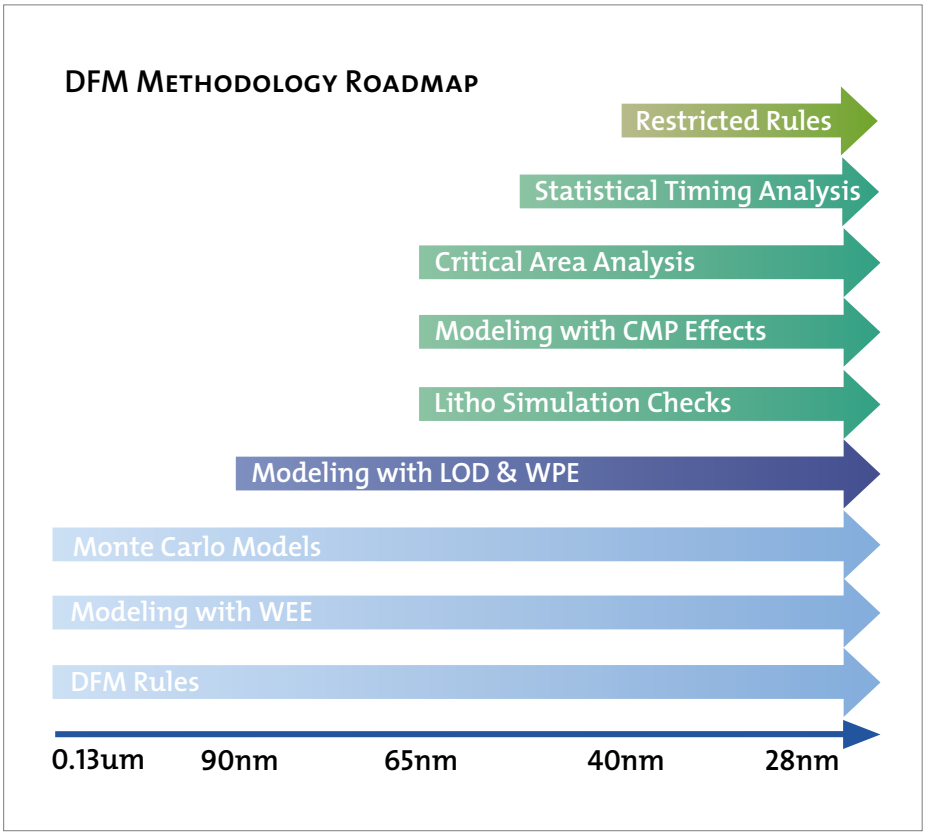
UMC works with leading EDA tool companies to provide a verified Reference Design Flow program to ensure the accuracy of customer designs in a proven environment. UMC Reference Design Flow program integrates solutions for digital and analog designs and low power solutions that incorporate the latest DFM resources available from leading third-party providers. Tools can be interchanged for added flexibility.

Features of Design Flow	Cadence	Synopsys	Mentor
Functional Logic Simulation	▲	▲	▲
Schematic Entry	▲	-	-
Logic Synthesis	▲	▲	-
Static Timing Analysis	▲	▲	-
Timing Closure	▲	▲	-
Signal Integrity	▲	▲	-
Floor Planning	▲	▲	-
Physical Synthesis	▲	▲	-
Multi-Vt Low Power	▲	▲	-
Multi-Vdd Low Power	▲	▲	-
Design For Test	▲	▲	▲
Design For Diagnosis	▲	▲	▲
DFM - double via insertion	▲	▲	▲
DFM - dummy metal filling	▲	▲	▲
Circuits Simulation	▲	▲	▲
Power Analysis	▲	▲	-
Layout Editor	▲	-	▲
Place & Route	▲	▲	-
Physical Verification	▲	▲	▲
Formal Verification	▲	▲	-
Parasitic Extraction	▲	▲	▲
Noise Analysis	▲	▲	-
RFCMOS/EMDM	▲	-	-
Analog/Mixed Signal	▲	-	▲

Note: ▲ Available

DFM Methodology

UMC offers optimal DFM (Design For Manufacturability) solutions to effectively and efficiently address factors that may negatively affect yield and performance for advanced technology designs. UMC's DFM solutions include advanced process models incorporated in SPICE and extraction decks for predicting random and systematic variations, technology files, DFM-compliant libraries and IP that embrace the intricacies of the fabrication process. Concise DFM recommendation rules are available along with a comprehensive rule-deck runset strategy to fulfill various design requirements.



UMC also offers pre-tapeout Optical Proximity Correction (OPC) and Litho Rule Check (LRC) for custom designs in addition to our standard post-tapeout services that include OPC, Litho Simulation Check (LSC), dummy fill, and metal slotting. At 65nm and below, UMC offers a DFM Design Enablement Kit (DEK) to seamlessly support model-based DFM tools. The DEK has a built-in Graphic User Interface (GUI) for DFM design database setup, and is completed with application notes and qualification reports for design reference.

UMC High Density Embedded Memory Solution - URAM™

To meet the future SoC trend of smaller form factor, higher bandwidth/speed and lower power consumption, UMC has developed its own high density memory solution, URAM, to fulfill market needs. Building on a logic compatible process, URAM adopts trench architecture as the cell capacitor with no new materials required. This backend-transparent structure also minimizes the backend model impact and ensures seamless integration with existing IPs. The macro implements the Error Correction Code (ECC) repair scheme with a byte-write feature to eliminate the need for redundant laser fuse/efuse and enhance the Soft Error Rate (SER). The wide on-chip bus boosts overall system performance. Pin count can be reduced by eliminating I/O devices, which can also lower the power consumption.

This enabling technology for SoC is now ready for customers to design in. Different solutions, Standard Performance (SP) and Low Leakage (LL), can be utilized to meet customers' speed/power requirements.

URAM for Broad Applications

Communications	**Networking, Wireless**
Graphics & Imaging Systems	**Frame Buffer for Image Processors**
Storage Devices	**Cache Memory**

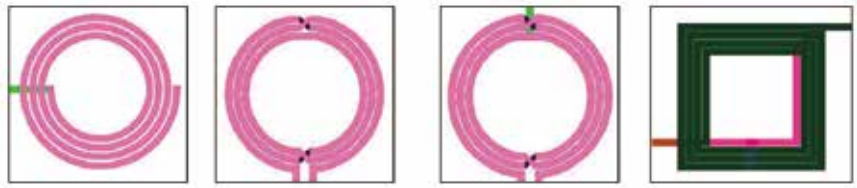
UMC e-Fuse Features

To reduce chip area, achieve better reliability performance, and shorten repair time compared to conventional Al fuse, UMC has developed an e-fuse solution to target the needs of a broad range of applications. The fuse array and complete functional macro are offered to ease the integration process for customers. Both wafer level and package level fuse are supported. Moreover, customers can use e-fuse for the OTP (one time programming) function to save overall costs.

Logic Compatible	• No extra masks necessary • Only one extra pad required
Complete Functional IP Macros	• Fuse array, programming circuit, sensing amplifier • Serial and parallel architecture
Design-Friendly Features	• Allows metal routing over fuses (M6 and above) • Programmable at package level
Flexibility	• Wafer level fuse options • Package level fuse options

Virtual Inductor Library

UMC has worked with its EDA tool partners to deliver the industry's first parameterized inductor design kit based on full-wave simulation: the Virtual Inductor Library (VIL). The VIL enables RFCMOS designers to create and simulate custom inductor geometries that are compatible with UMC's processes. It is built upon UMC's Electromagnetic Design Methodology (EMDM), which allows engineers to easily and accurately create any RF structure. EMDM gives designers the flexibility to innovate new geometries simply by editing parameters such as diameter, number of turns or width.

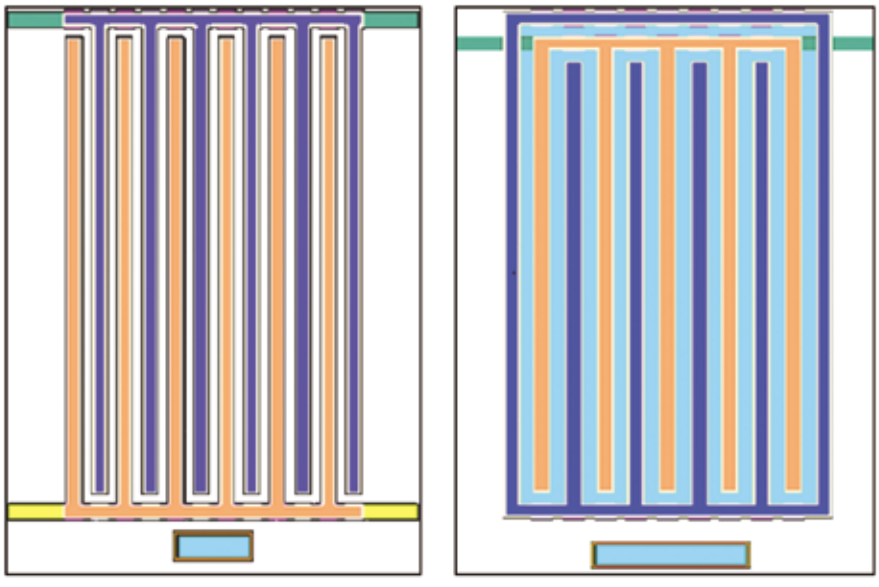


Spiral | Differential w/o center tap | Differential with center tap | Stack

The GUI based VIL can be used to simulate all types of RF inductors.

Virtual Capacitor Library

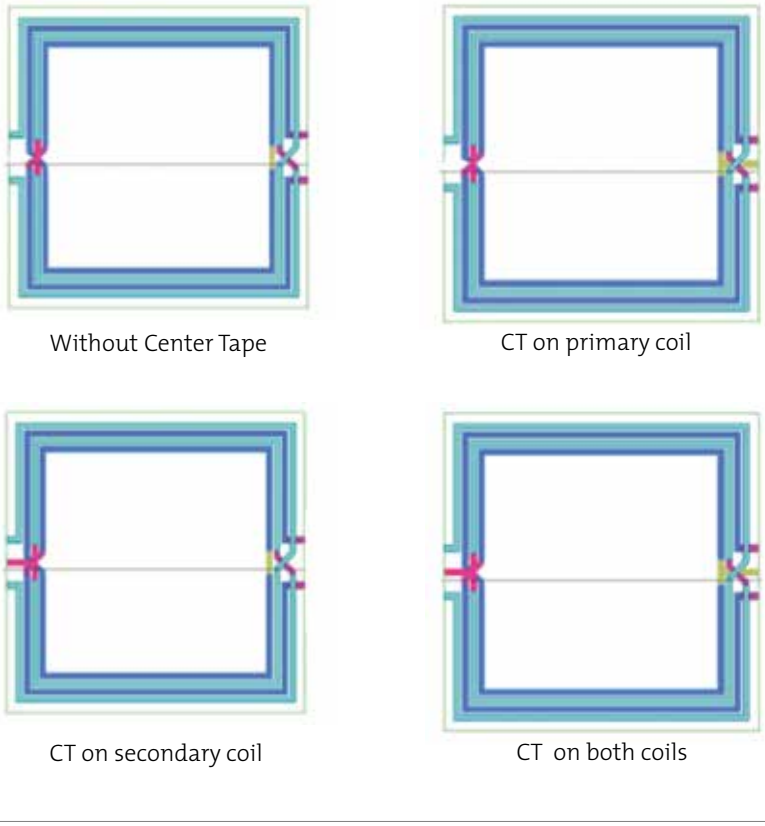
UMC and its EDA tool partners have delivered the industry's first parameterized MOM capacitor design kit based on full-wave simulation: the Virtual Capacitor Library (VCL). The VCL enables RFCMOS designers to create and simulate custom capacitor geometries that are compatible with UMC's processes. It is built upon UMC's Electromagnetic Design Methodology (EMDM), which allows engineers to easily and accurately create any RF structure. EMDM gives designers the flexibility to innovate new geometries simply by editing parameters such as number of metal and fingers, arrays, and length of fingers for capacitor.



The GUI based VCL can be used to simulate all types of RF capacitors.

Virtual Transformer Library

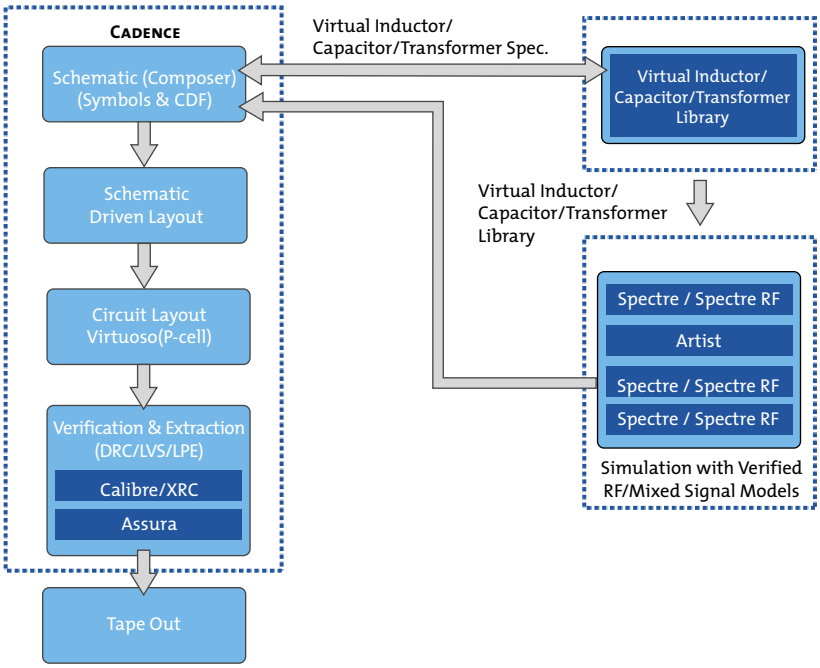
UMC has also worked with its EDA tool partners to deliver the industry's first parameterized transformer design kit based on full-wave simulation: the Virtual Transformer Library (VTL). The VTL enables RFCMOS designers to create and simulate custom transformer geometries that are compatible with UMC's processes. It is built upon UMC's Electromagnetic Design Methodology (EMDM), which allows engineers to easily and accurately create any RF structure. EMDM gives designers the flexibility to innovate new geometries simply by editing parameters such as primary impedance, secondary impedance, number of turns, mode, and frequency for transformer.



The GUI based VTL can be used to simulate all types of RF transformers.

MS/RF Design Flow and FDK

The FDK (Foundry Design Kit) provides IC designers with an automatic design environment. The methodology provides access to circuit-level design and simulation, circuit layout, and layout verification with accurate RF device models. In the front-end, fundamental components of UMC's MS/RF process are implemented in common design environments and simulation tools. The back-end includes parameterized cells (P Cell), which include a schematic driven layout to provide an automatic and complete design flow. Callback functions are also provided in the design flow to minimize data entry. EDA tools for MS/RF designs are also supported.



Optimum Inductor Finder (OIF)

UMC offers the Optimum Inductor Finder (OIF) in the FDK package. The OIF gives designers the ability to quickly access a large library of inductors calibrated to UMC's silicon. It also allows users to perform inductor optimization through just a few simple steps with the user-friendly interface. For instance, customers can define a desired inductor and make trade-offs between Q-factor and area. The OIF will select a design that best fits the specifications in a matter of seconds.

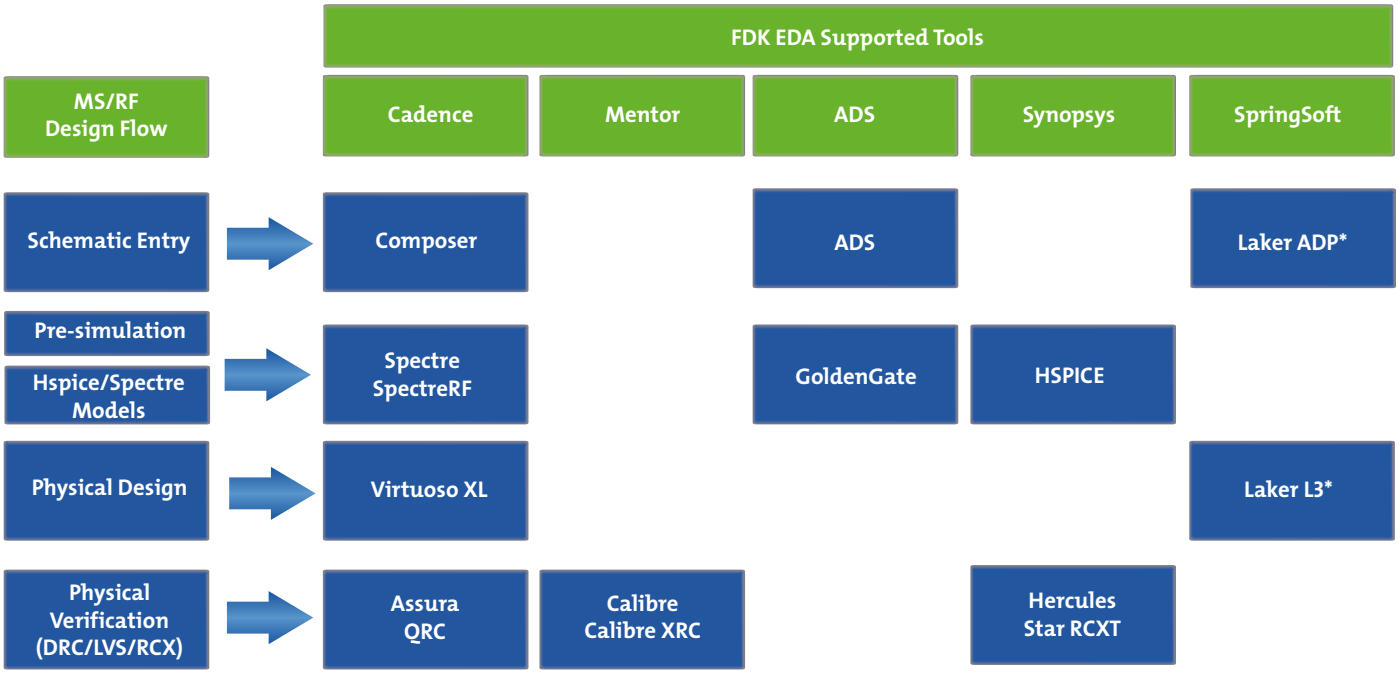
Optimum Capacitor Finder (OCF)

UMC offers the Optimum Capacitor Finder (OCF) in the FDK package. The OCF gives designers the ability to quickly access a large library of capacitors calibrated to UMC's silicon. It also allows users to perform capacitor optimization through just a few simple steps with the user-friendly interface. For instance, customers can define a desired capacitor and make trade-offs between Q-factor and area. The OCF will select a design that best fits the specifications in a matter of seconds.

Optimum Transformer Finder (OTF)

UMC offers the Optimum Transformer Finder (OTF) in the FDK package. The OTF gives designers the ability to quickly access a large library of transformers calibrated to UMC's silicon. It also allows users to perform transformer optimization through just a few simple steps with the user-friendly interface. For instance, customers can define a desired transformer and make trade-offs between impedance and area. The OTF will select a design that best fits the specifications in a matter of seconds.

Analog Design Methodology



Note: *is available by request

MEMO:

New Customers
For new customer inquiries, please direct all questions to **sales@umc.com**

Worldwide Contacts

Headquarters:
UMC
No. 3, Li-Hsin 2nd Road,
Hsinchu Science Park,
Hsinchu, Taiwan, R.O.C.
Tel: 886-3-578-2258
Fax: 886-3-577-9392
Email: foundry@umc.com

In China:
UMC Beijing:
Room #512, 5F, South Block,
Raycom InfoTech Park, No.2,
Kexueyuan South Road,
Zhongguancun,
Haidian District,
Beijing 100190, China
Tel: 86-10-59822250
86-18913138053
Fax: 86-10-59822588

HeJian Technology (Suzhou):
No. 333, Xinghua Street, Suzhou
Industrial Park, Suzhou, Jiangsu
Province 215025, China
Tel: 86-512-65931299
Fax: 86-512-62530172

In Japan:
UMC Group Japan
15F Akihabara Centerplace Bldg.,
1 Kanda Aioi-Cho Chiyoda-Ku
Tokyo 101-0029 Japan
Tel : 81-3-5294-2701
Fax: 81-3-5294-2707

In Singapore:
UMC-SG
No. 3, Pasir Ris Drive 12,
Singapore 519528
Tel: 65-6213-0018
Fax: 65-6213-0005

In Korea:
UMC Korea
1117, Hanshin Intervally24, 322,
Teheran-ro, Gangnam-gu,
Seoul, Korea
Tel: 82-2-2183-1790
Fax: 82-2-2183-1794
Email:korea@umc.com

In North America:
UMC USA
488 De Guigne Drive,
Sunnyvale, CA 94085, USA
Tel: 1-408-523-7800
Fax: 1-408-733-8090

In Europe:
UMC Europe BV
De entree 77
1101 BH Amsterdam Zuidoost
The Netherlands
Tel: 31-(0)20-5640950
Fax: 31-(0)20-6977826

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FOR MORE INFORMATION: VISIT **WWW.UMC.COM** OR E-MAIL **SALES@UMC.COM**