


Helping Customers Innovate, Improve & Grow



Description

Vectron's VC-840 Crystal Oscillator (XO) is a quartz stabilized square wave generator with a CMOS output. The VC-840 is a fundamental oscillator resulting in very low jitter performance, and a monolithic IC which improves reliability and reduces cost.

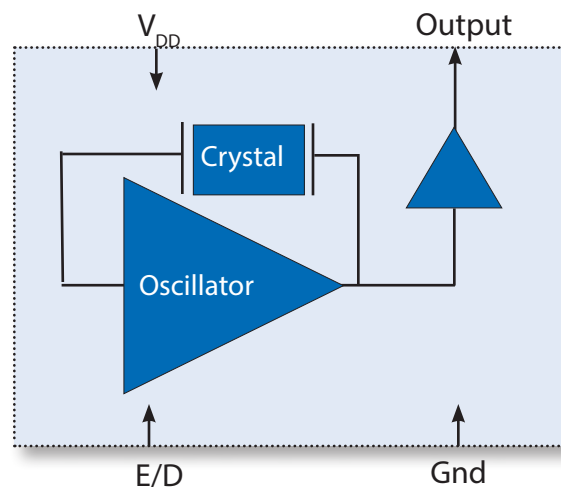
Features

- CMOS output XO
- 1-60.0000 MHz Output Frequency
- 1.8, 2.5 or 3.3 V Operation
- Fundamental Crystal Design with low Jitter Performance
- Output Disable Feature
- Small Industry Standard Package, 2.5x2.0x0.9mm
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

Applications

- SONET/SDH/DWDM
- Ethernet, GE, SynchE
- Storage Area Networking
- Fiber Channel
- Digital Video
- Broadband Access
- Base Stations, Picocells

Block Diagram



Specifications

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage ¹	V_{DD}		3.3		V
Maximum Voltage		-0.5		7	V
Current ² , <20.000MHz 20.000-40.000MHz 40.001-60.000MHz 60.001-75.000Mhz	I_{DD}			7 13 19 24	mA
Current, Output Disabled				10	uA
Frequency					
Nominal Frequency	f_N	0.75		60	MHz
Stability ³ , <i>Ordering Information</i>		$\pm 25, \pm 50$ or ± 100			ppm
Outputs					
Output Logic Levels ² Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive	V_{OH} V_{OL} I_{OH} I_{OL}	0.9* V_{DD} 4 4		0.1* V_{DD}	V V mA mA
Load	I_{OUT}			15	pF
Output Rise /Fall Time ²	t_R/t_F		2.5	5	ns
Duty Cycle ^{2,4}		45		55	%
Period Jitter ⁵ RMS Peak-Peak	ϕJ		1.5 12		ps
Enable/Disable					
Output Enable/Disable ⁶ Output Enable Output Disable	V_{IH} V_{IL}	0.7* V_{DD}		0.3* V_{DD}	V V
Disable Time				150	ns
Start-Up Time	t_{SU}			10	ms
Operating Temp, <i>Ordering Information</i>	T_{OP}	-20/70 or -40/85			°C

- 1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01uF.
- 2] Parameters are tested with production test circuit below , Figure 1.
- 3] Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging
- 4] Duty Cycle is measured as On Time/Period (Fig 2).
- 5] Broadband Period Jitter measured using LeCroy Waverunner 610Zi, 200k minimum samples
- 6] The Output is Enabled if the Enable/Disable is left open.

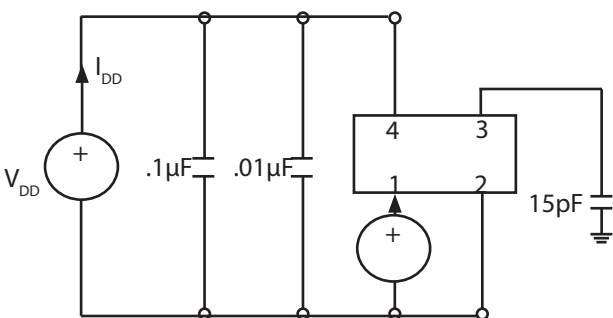


Fig 1: Test Circuit

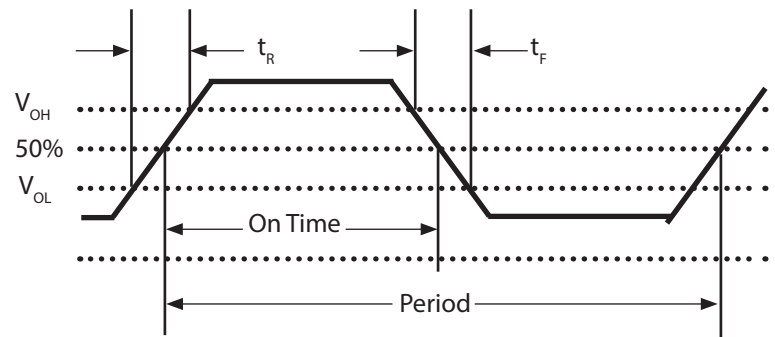


Fig 2: Waveform

Specifications

Table 2. Electrical Performance					
Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage ¹	V_{DD}		2.5		V
Maximum Voltage		-0.5		7	V
Current ² , <20.000MHz 20.000-40.000MHz 40.001-60.000MHz 60.001-75.000Mhz	I_{DD}			5 9 11 14	mA
Current, Output Disabled				10	uA
Frequency					
Nominal Frequency	f_N	0.75		60	MHz
Stability ³ , <i>Ordering Information</i>		±25, ±50 or ±100			ppm
Outputs					
Output Logic Levels ² Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive	V_{OH} V_{OL} I_{OH} I_{OL}	0.9* V_{DD} 4 4		0.1* V_{DD}	V V mA mA
Load	I_{OUT}			15	pF
Output Rise /Fall Time ²	t_R/t_F		2.5	5	ns
Duty Cycle ^{2,4}		40		60	%
Period Jitter ⁵ RMS Peak-Peak	ϕJ		1.5 12		ps
Enable/Disable					
Output Enable/Disable ⁶ Output Enable Output Disable	V_{IH} V_{IL}	0.7* V_{DD}		0.3* V_{DD}	V V
Disable Time				150	ns
Start-Up Time	t_{SU}			10	ms
Operating Temp, <i>Ordering Information</i>	T_{OP}	-20/70 or -40/85			°C

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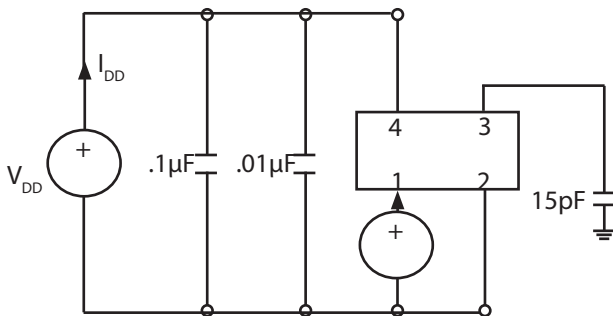


Fig 3: Test Circuit

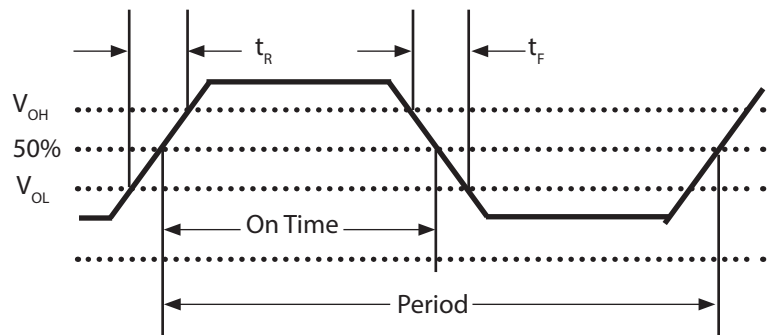


Fig 4: Waveform

Specifications

Table 3. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage ¹	V_{DD}		1.8		V
Maximum Voltage		-0.5		7	V
Current ² , <20.000MHz 20.000-40.000MHz 40.001-50.000MHz	I_{DD}			2.5 3.0 3.5	mA
Current, Output Disabled				10	uA
Frequency					
Nominal Frequency	f_N	0.75		60	MHz
Stability ³ , <i>Ordering Information</i>		±25, ±50 or ±100			ppm
Outputs					
Output Logic Levels ² Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive	V_{OH} V_{OL} I_{OH} I_{OL}	0.9* V_{DD} 4 4		0.1* V_{DD}	V V mA mA
Load	I_{OUT}			15	pF
Output Rise /Fall Time ²	t_R/t_F		2.5	5	ns
Duty Cycle ^{2,4}		45		55	%
Period Jitter ⁵ RMS Peak-Peak	ϕJ		1.5 12		ps
Enable/Disable					
Output Enable/Disable ⁶ Output Enable Output Disable	V_{IH} V_{IL}	0.7*VDD		0.3*VDD	V V
Disable Time				150	ns
Start-Up Time	t_{SU}			10	ms
Operating Temp, <i>Ordering Information</i>	T_{OP}	-20/70 or -40/85			°C

- 1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01 uF.
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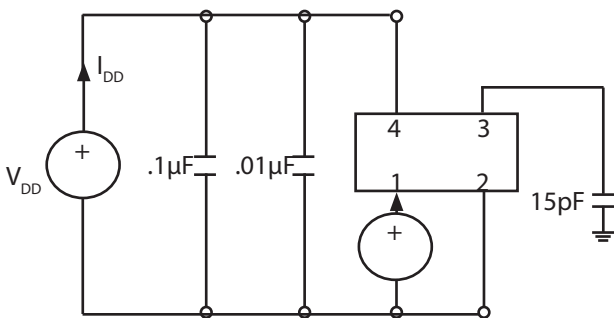


Fig 5: Test Circuit

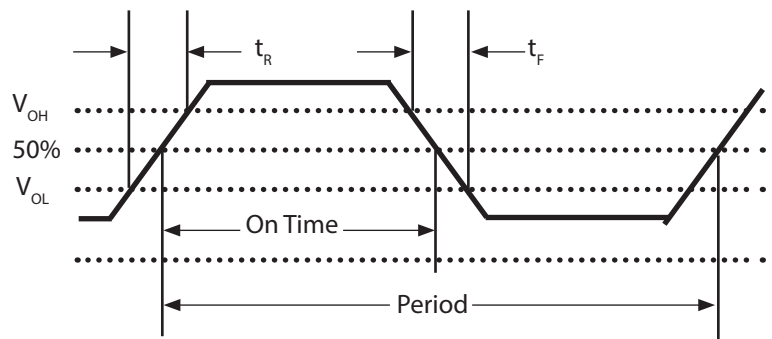
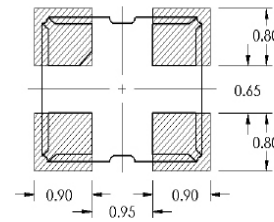
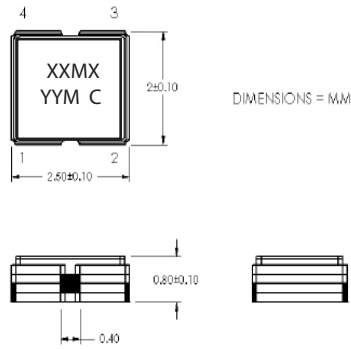


Fig 6: Waveform

Outline Drawing & Pad Layout



Dimensions in mm

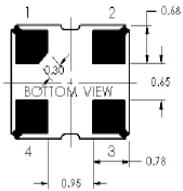


Table 4. Pin Out

Pin	Symbol	Function
1	E/D	Enable Disable
2	GND	Case and Electrical Ground
3	Output	Output
4	V _{DD}	Power Supply Voltage

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VC-840 family is capable of meeting the following qualification tests:

Table 5. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold over Nickel

Although ESD protection circuitry has been designed into the VC-840 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

Table 6. ESD Ratings

Model	Minimum	Conditions
Human Body Model	1500V	MIL-STD-883, Method 3015
Charged Device Model	1000V	JESD22-C101

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if E/D is applied before V_{DD}.

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Storage Temperature	T _S	-55 to 100	°C
Soldering Temp/Time	T _{LS}	260 / 10	°C / sec

IR Reflow

The VC-840 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VC-840 device is hermetically sealed so an aqueous wash is not an issue.

Solderprofile:

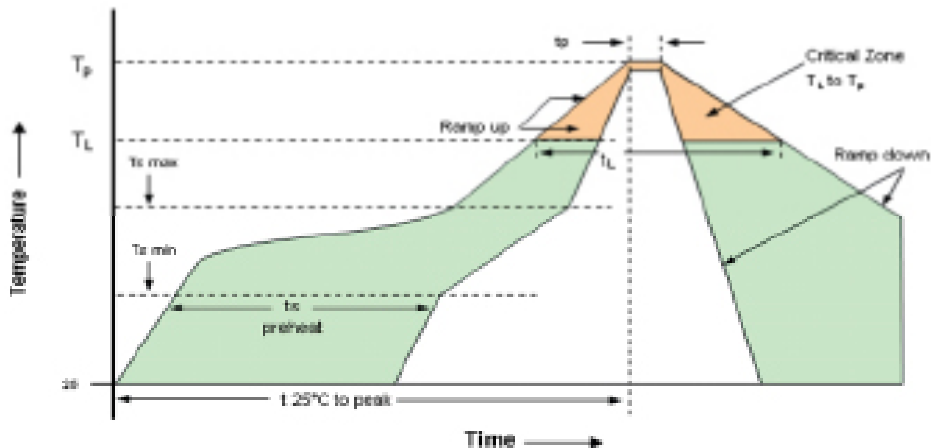


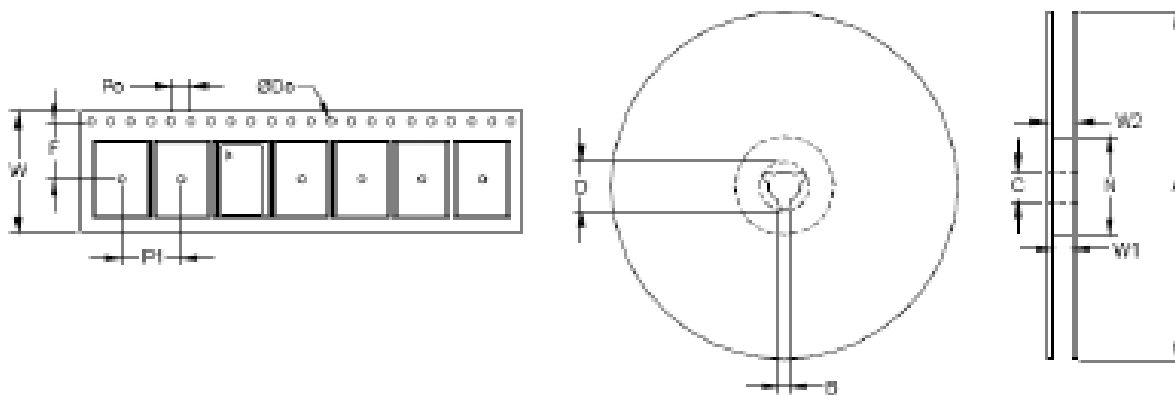
Table 8. Reflow Profile

Parameter	Symbol	Value
PreHeat Time Ts-min Ts-max	t_s	60 sec Min, 260 sec Max 150°C 200°C
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	T_{AMB-P}	480 sec Max
Time at 260 °C	t_p	30 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

Tape and Reel

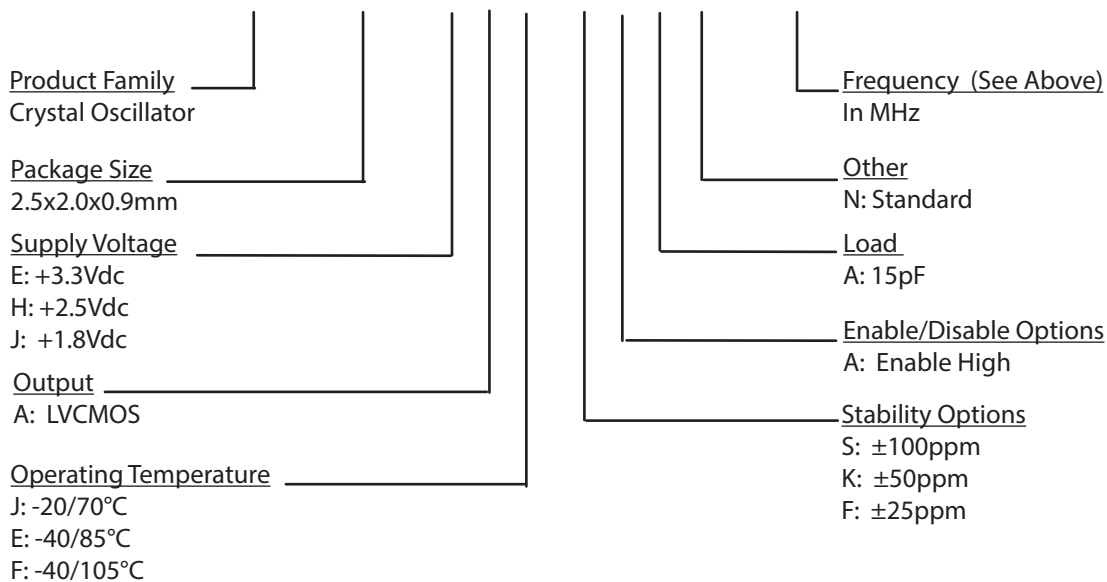
Table 9. Tape and Reel Dimensions

Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VC-840	8.0	3.5	1.5	4.0	4.0	180							1000 2000



Ordering Information

VC-840-EAE-KAAN- xxMxxxxxxx



Example: VC-840-EAE-KANN-25M0000000 = 2.5x2.0, +3.3V, LVCMOS output, ±50ppm over -40/85°C with a 25.000MHz output

Note: Not all combinations of options are available. Other specifications may be available upon request. Consult with factory.

For Additional Information, Please Contact

USA:

Vectron International
267 Lowell Road Unit 102
Hudson, NH 03051
Tel: 1.888.328.7661
Fax: 1.888.329.8328

Europe:

Vectron International
Landstrasse, D-74924
Neckarbischofsheim, Germany
Tel: +49 (0) 3328.4784.17
Fax: +49 (0) 3328.4784.30

Asia:

Vectron International
68 Yin Cheng Road (C), 22nd Floor
One LuJiaZui
Pudong, Shanghai, 200120 China
Tel: 86.21.6194.6886
Fax: 86.21.6194.6699

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Rev: 01/17/2017

Revision History

Revision Date	Edited	Approved	Description
May 14, 2014	VN	TG	Corrected Operating Temperature in Specification Tables 1, 2 and 3 to show -20/70C. Removed Standard Output Frequencies Table 10 (Empty)
Aug 4, 2015	EM	DL	Added temp range -40/105°C and note in RED on page 7
Aug 16, 2015	EM	DL	Updated Rise/Fall time.
Jan 17, 2017	RC	RC	Update IR Reflow Table