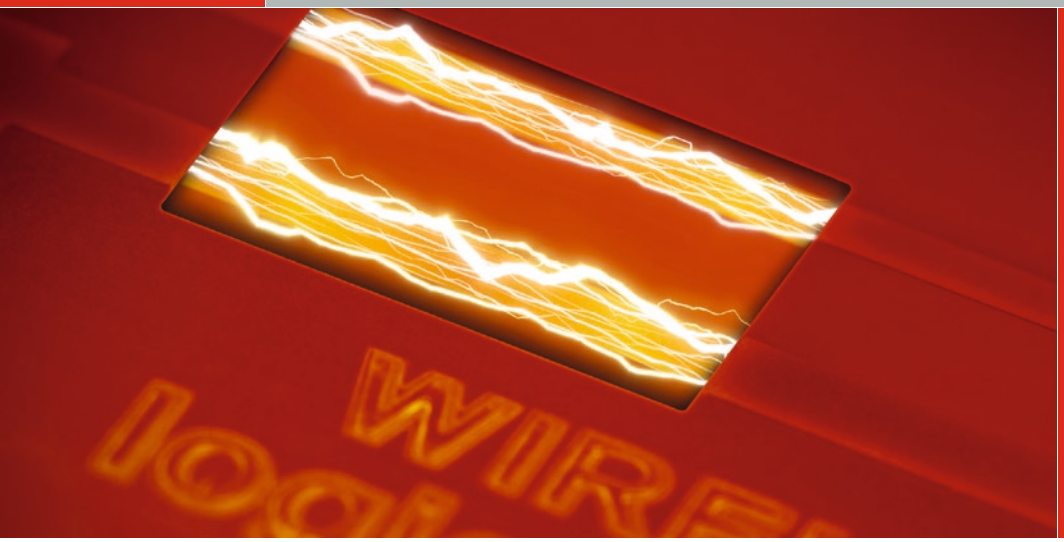
DESIGN GUIDE
Version 1.4

WÜRTH ELEKTRONIK

Design Guide for

High Current Solutions with WIRELAID®



High Current Solutions with WIRELAID® Technology

Your benefit

Caused by the increasing requirements of power and digital control electronics in almost every industry, PCB manufacturers are facing new challenges. To combine high currents and signals at the same time, the Wirelaid technology provides a **partial power management** as a competitive alternative to PCBs with thick copper technology or a parallel arrangement of additional layers. The concept of the Wirelaid technology is the use of embedded copper wires in a PCB.

As a result, standard conductors, which can only manage low currents, become high current tracks. This allows for the combination of power and signal processing electronics on one single board.

c UL® us

Available with UL listing type WE51 (UL 94 V-0).

Your advantages

- Reduced system volume
- Wires replacing the thick copper
- Heat reduction due to smaller cross-sectional area of copper
- Elimination of connectors
- Reduction of number of layers
- Combination of power and signal processing electronics on one single layer
- Reduction of system costs
- Better soldering process in comparison with traditional thick copper technology
- Thinner copper layers
- Fewer thick copper areas through the use of partial power management

Content

Wire types

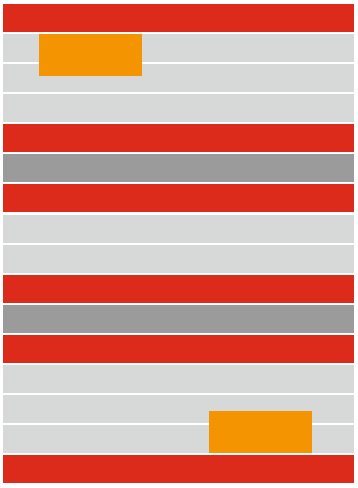
F 14	1.4 x 0.35 mm²
Cross-section area	Ø 0.49 mm²

For combining with Semiflex, 0.1 mm thick wires of different widths are available.

Nomenclature

Outer layer

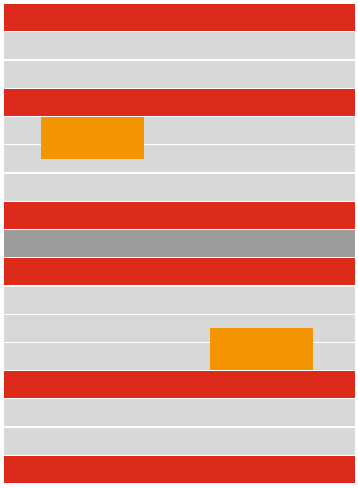
ML6 Wire@1@6



The example shows a multilayer with 6 layers and wires beneath layer 1 and layer 6.

Inner layer

ML6 Wire@2@5



The example shows a multilayer with 6 layers and wires beneath layer 2 and layer 5.

The following considerations apply when selecting a Wirelaid variant:

- More complex logic circuits use SMD components, such as controllers and memory with fine contact pitches. To keep the supply layers free for ultra-fine conductive components, Wirelaid wires are moved to interior layers. EMC requirements and requirements for multiple supply voltages on inner layers can only be met with standard cores and lower copper thicknesses. The number of layers is mostly the same when compared with the multilayer standard, see layout ML6 Wire@2@5.

- If heat dissipation because of direct contact with the housing plays a part, or if power semiconductors such as IGBT or D²PAK are fitted directly on the outer layer, then this outer layer is used as a Wirelaid layer with soldered wires. See layout ML6 Wire@1@6. This should also be the goal for simpler logic circuits. Furthermore, many through-contacts and therefore costs are saved, if the power components can be attached directly on the land pad of the Wirelaid wires.

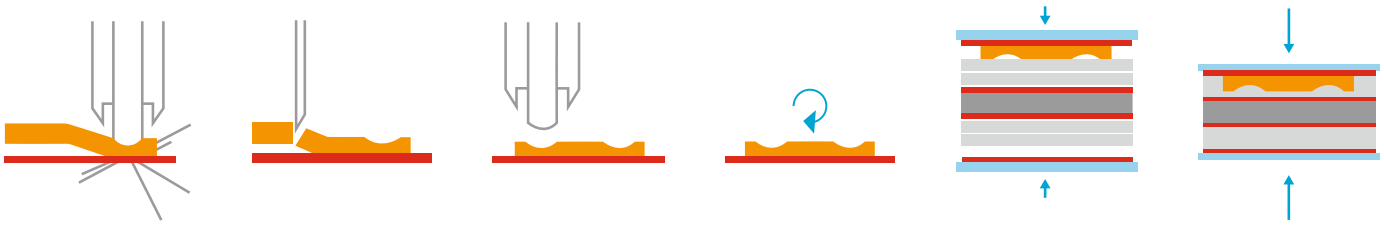
- For simple circuits, it may be possible to reduce the number of layers.

Outer layer?
Inner layer?

Production processes

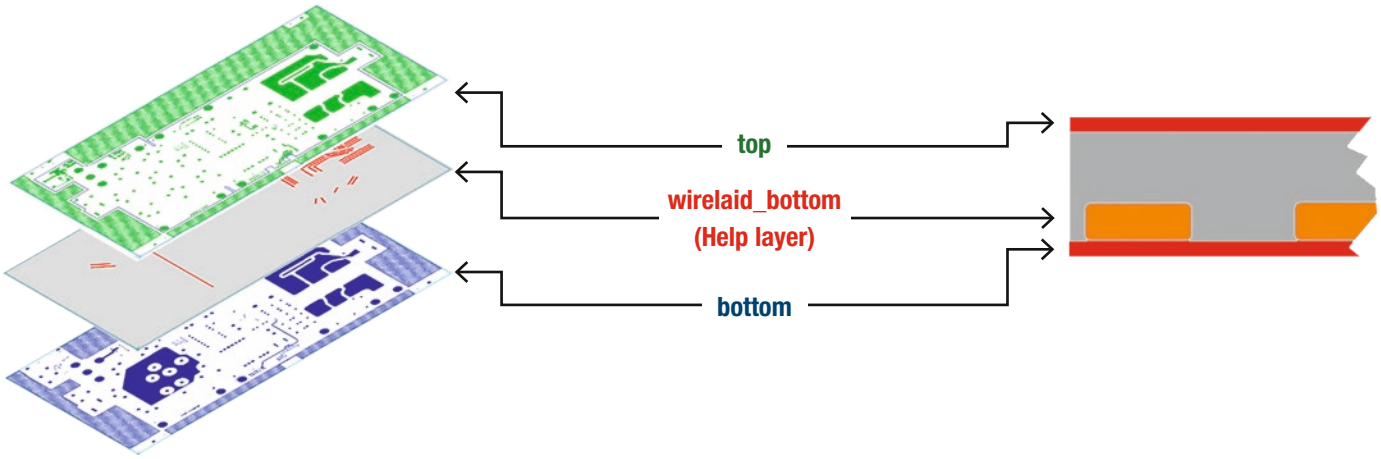
At the beginning of the Wirelaid process, the wires are fixed onto the under side of the copper foil using resistance welding. The wire is then welded again at the end of the trace and cut to the appropriate length.

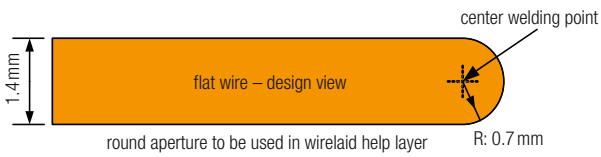
The Wirelaid copper foil is then laminated onto a multilayer PCB using standard production processes. As a result the Wirelaid copper foil forms the external layer of the PCB. The Wirelaid wires are completely embedded. Finally the outer tracks are created using standard PCB processes.

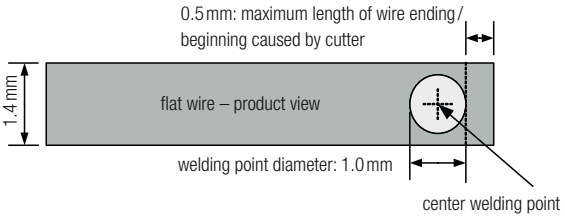


PCB creation and technical specification

When using Wirelaid technology in your PCB stack up, add an additional help layer in Gerber format showing the relevant wires and widths. The wires are visible through circular apertures with a wire width of 1.4 mm. On the bottom layer, a pad must be positioned centrally to the point of welding. The wire should be covered in the design by a copper conductor.

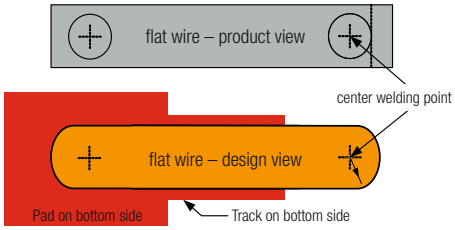






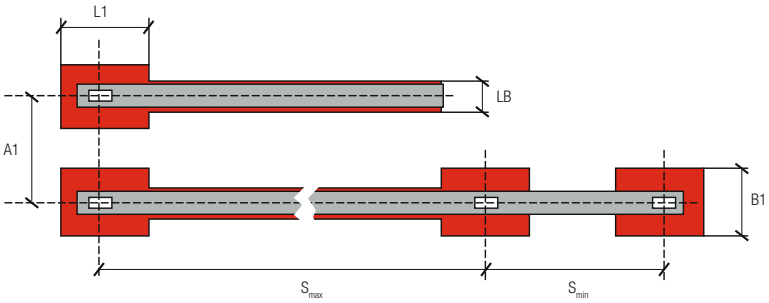
Design Rules

	Dimensions (minimum)	F 14 350 x 1400 µm²
L_1 x B_1	Pad size	3.5 x 3.0 mm²
LB	Track width above wire	1.9 mm
A_1	Distance of pitch between wires of separate potentials (considering the positioning of the pad)	1.9 mm + Iso distance*
A_2	Distance pitch of wires for same potential	1.8 mm
S_{max}	Max. length of wire between welding points	100 mm
S_{min}	Min. length of wire between welding points	7.5 mm

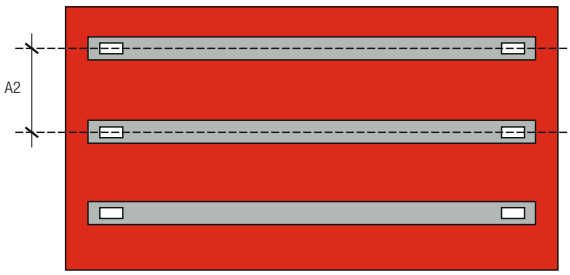


*Dependent on the thickness of copper layer according to the current Basic Design Guide of Würth Elektronik at **www.we-online.com**

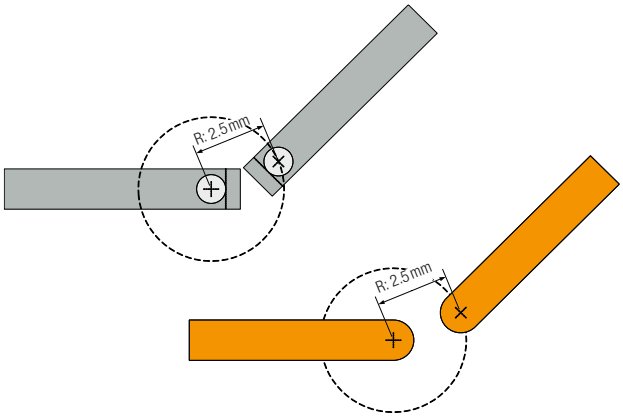
Separate potentials

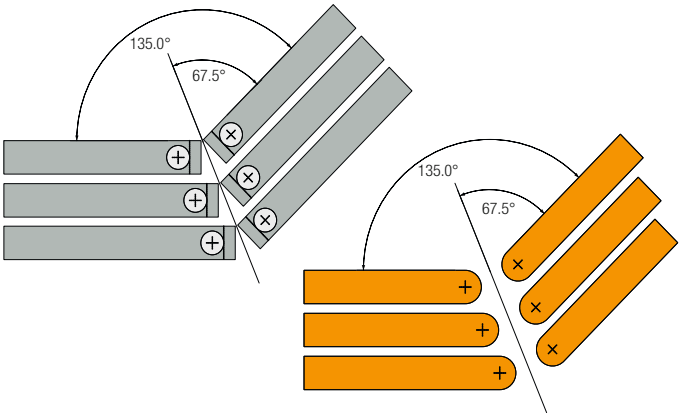


Same potentials



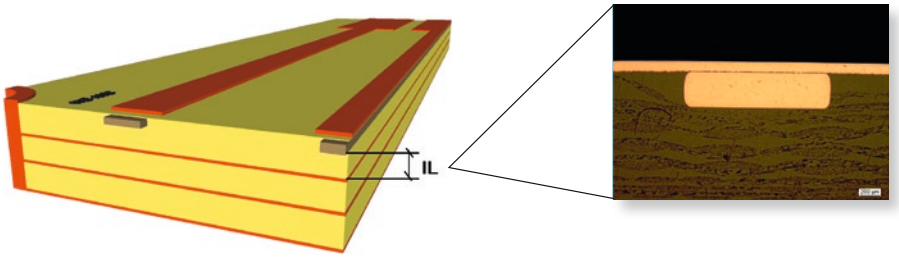
Structure with angled wire path





Isolation distance between wire and inner layer

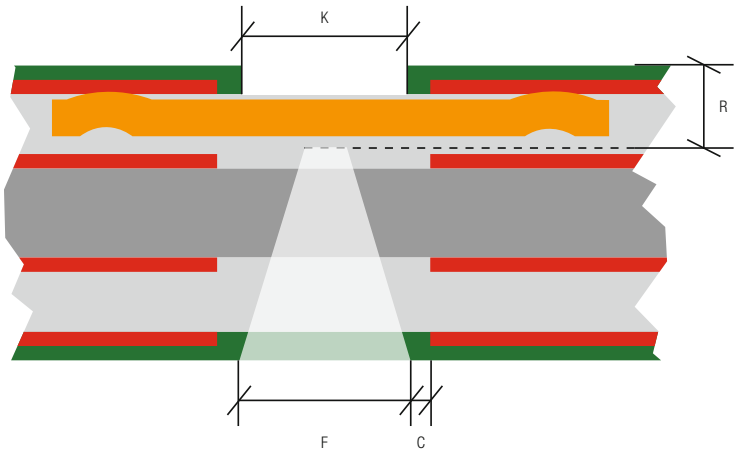
Dependent on the specific stack up of the customer, which we are pleased to create for you.



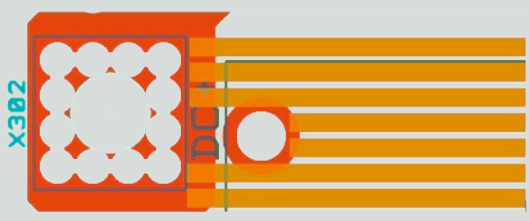
3D Design Rules

	Dimensions (minimum)	
C	Distance copper to milled edge	0.3 mm
F	Width of milled slot	F = 0.4 x (thickness of PCB – R) + 200 µm
K	Solder mask clearance in bending area	1.0 mm
R	Thickness of residual material	Thickness of wire + copper + solder mask + 150 µm

- Wires need to be arranged at right angles to the bending area
- The usage of an applicable bending (forming) tool is recommended
- Bending radius ≥ 0.1 mm
- Care has to be taken so that the bent parts are secured in the installed application to avoid further movement



! Please include in the layout:
The Wirelaid wires may not be drilled through.



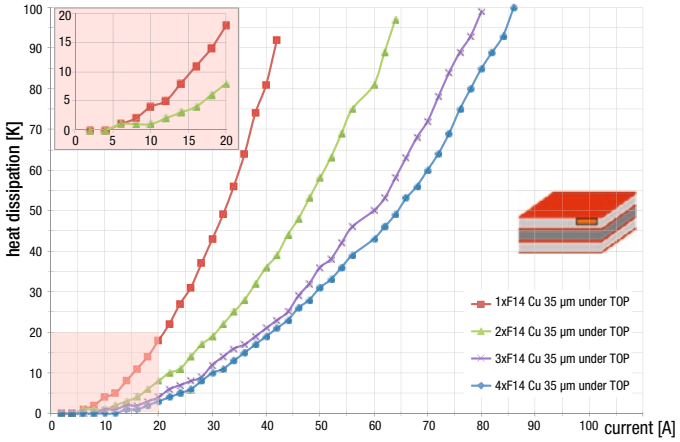
Ampacity

The following diagrams show real measurement values under laboratory conditions and with a steady current. They serve as guidelines for a first layout without taking into account the power loss of components, layout influences and environmental conditions such as orientation and housing influences.

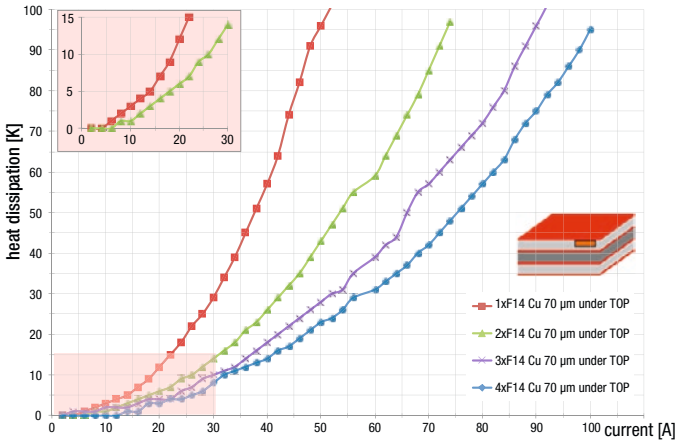
Where there are more than four F14 wires, the following can be assumed: per wire 12 A at $\Delta T = 20$ K

Wires welded under the external layer

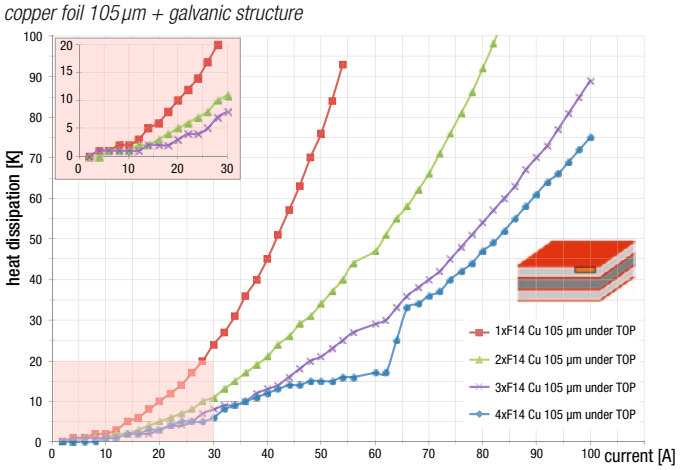
copper foil 35 µm + galvanic structure



copper foil 70 µm + galvanic structure

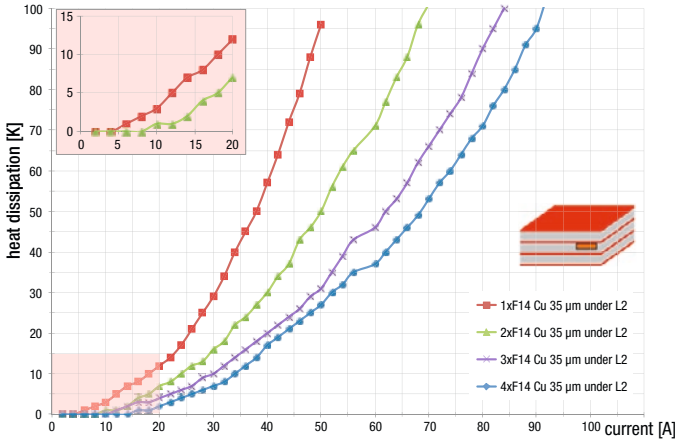


copper foil 105 µm + galvanic structure

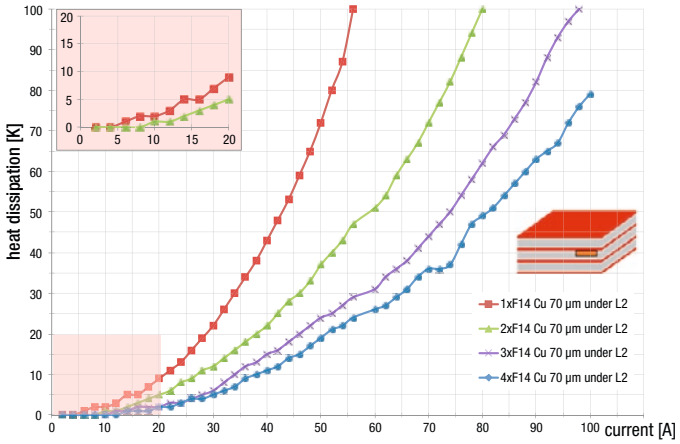


Wires welded under the internal layer

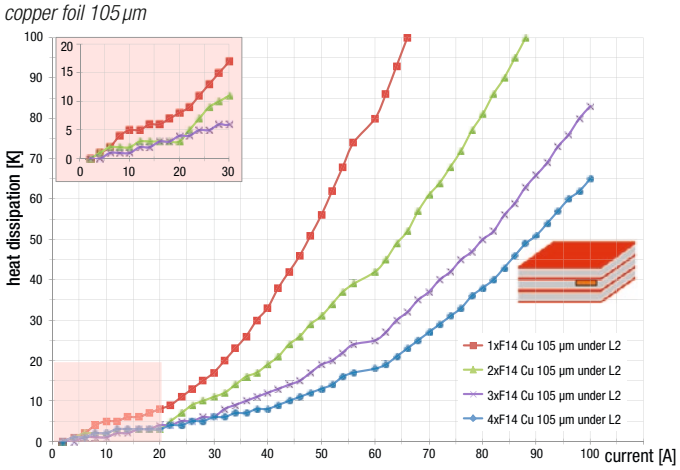
copper foil 35 µm



copper foil 70 µm



copper foil 105 µm



Investigative procedure for the calculation of the ampacity tables

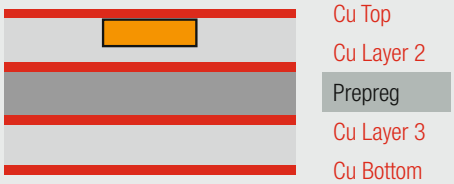
Test set-up

- FR4 base material
- PCB thickness: 2.2 – 2.5 mm
- PCB profile: 115 x 80 mm²
- Equal copper flooding of 40 % on each layer

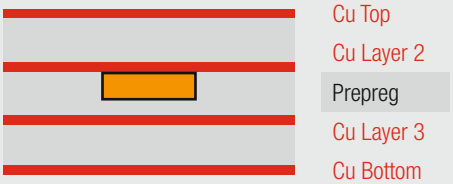
For the test set-up the PCBs were measured in a temperature-controlled loading gage at a constant environmental temperature of 22 C°. Solder pads were used for the power supply. The different currents are applied for five minutes to stabilise the thermal gradients, after which an infrared image was recorded.

For the test series, the design versions shown below were used.

Wires welded under the external layer



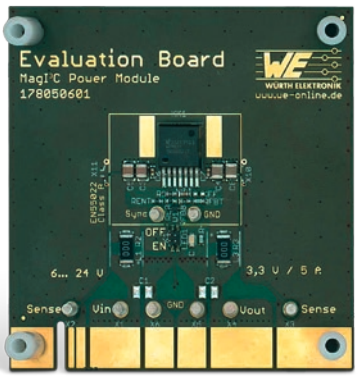
Wires welded under the internal layer

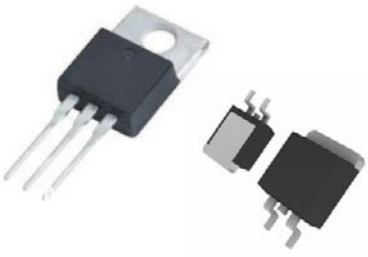


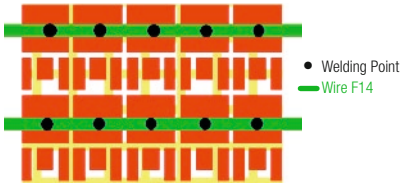
Heat dissipation

Passive heat dissipation extends the service life of the power semiconductors.

This is achieved by a massive increase in heat sink directly below the component, for example, the types TO2xy or D2PAK over the wires that are welded there. This is optimally suited to the SMT components. The following is the results from a practical trial:

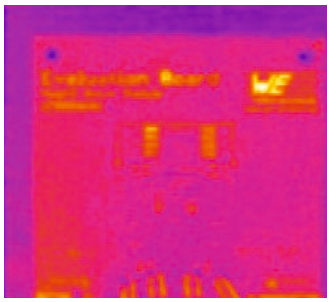




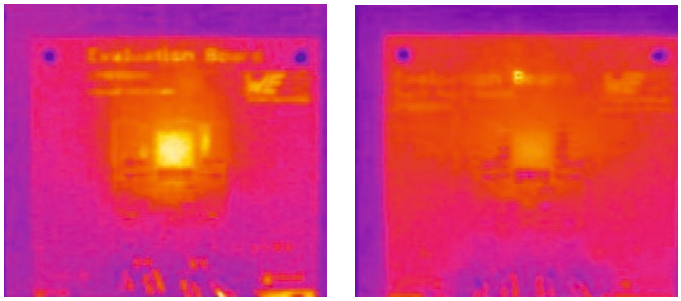


Heat dissipation of an array through a common Wirelaid wire with welding points below the components.

With Wirelaid®



After approximately 5 seconds, one recognises the wires that conduct the power loss in the component. Heating of chip from Tu = 20°C to Tmax at nominal power loss (16.5 W/cm²):



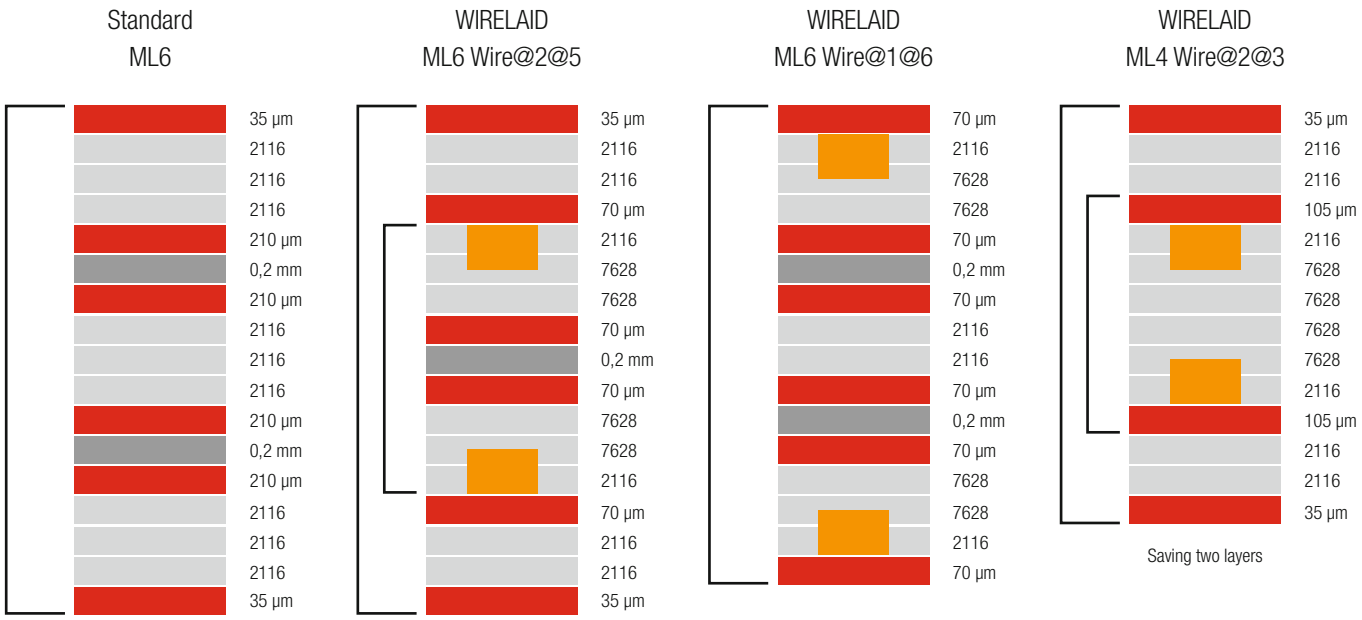
Left Tmax = 55°C without wires, right Tmax = 38°C with wires. Significantly improved hot spot situation: According to Arrhenius, a temperature lower by 17 K corresponds to an **extension in the life span by a factor of 4!**

Cost comparison

In order to be able to decide whether to use a “standard” thick copper technology or Wirelaid for a serial production, it is important to have a reliable cost assessment or cost comparison at an early stage.

The following is a comparison of a frequently used design with partial high-current technology at the same current-carrying capacity.

6-layer: internal 210 µm / external 70 µm ↔ WIRELAID



Number of wires per production panel until cost parity is achieved

Basics	1.272	1.304	1.404

In all other variants, the price advantages for partial high-current solutions with Wirelaid technology are clear. The price advantage comes from the saving on 210 µm of copper on the inner layers and a significant reduction in material and etching costs. It is only with the use of 1,272, 1,304 or 1,404 Wirelaid wires per manufactured panel that the price advantage is really “exhausted”, in which case it is still not worth using the standard technology because Wirelaid offers tangible benefits in terms of both weight and the soldering process.

In the first Wirelaid variant (the second diagram from the left) with wires on the inner layer, an additional multilayer lamination is necessary. The cost advantage compared with thick copper construction are somewhat smaller as a result, but the design offers decisive advantages for logic layout on the outer layer because the Wirelaid wires are placed internally and the outer layer can be carried out with a thinner 35 µm or even a 18 µm copper foil. In this way, even ultra-fine lines on the outer layer are possible without any problems.

Further cost comparisons are available on request.

Wirelaid always simplifies the drilling process in the further manufacture of the circuit board and as a result reduces the drilling costs because the copper thickness to be drilled is more than halved!

“We would like to highlight both the technological benefits and the cost advantages to our customers.”

Andreas Schilpp, responsible product manager for high current applications at Würth Elektronik

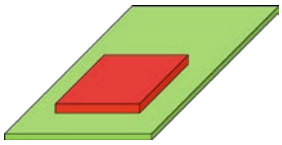
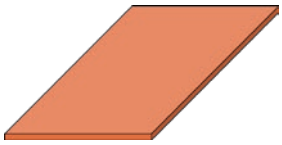
Cost comparison at system level

For more complex systems the greatest saving potential exists at system level. Logic modules may be integrated due to the possibility of combining high current and logic on a circuit board. Alongside a simpler Wirelaid circuit board, this enables the entire system to be optimised. The following example should make this clear:

Starting situation:
A multilayer circuit with six layers, each 105 µm copper, handles the high current job. The logic is implemented on a module with fine-conductor technology and by means of a plug connector on the main circuit board.

New solution with Wirelaid:
The logic module can be fully integrated thanks to the fine-conductor structures on the mounting position. The jointing technology is no longer required along with all other system costs for the module and the "marrying up".

The simpler system now offers the following savings (sample calculation):

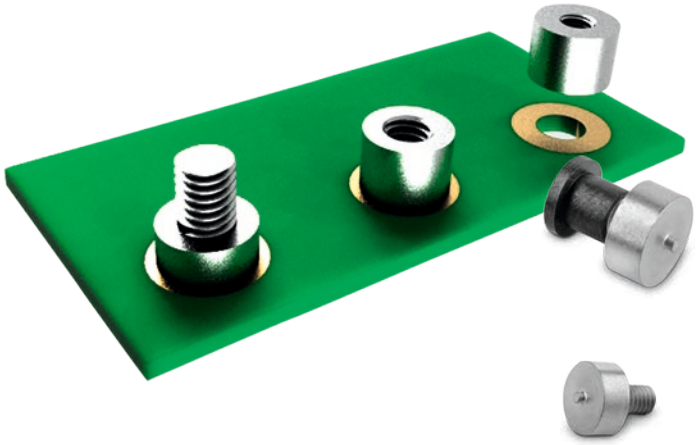
	Previous solution	**New solution**
System	 ML6 105µm power board, logic module and jointing technology	 WIRELAID circuit board ML6 wire@1
Main circuit board	**€ 6.50**	**€ 5.90**
Logic module	**€ 1.00**	**–**
Connection parts	**€ 2.00**	**–**
Assembly setup costs	**€ 1,000**	**€ 500**
Paste stencils	**€ 400**	**€ 200**
AOI test	**€ 250**	**€ 125**
Test costs	**€ 500**	**€ 250**
Setup costs per order	**€ 400**	**€ 200**
Storage and logistics	**3 x**	**1 x**

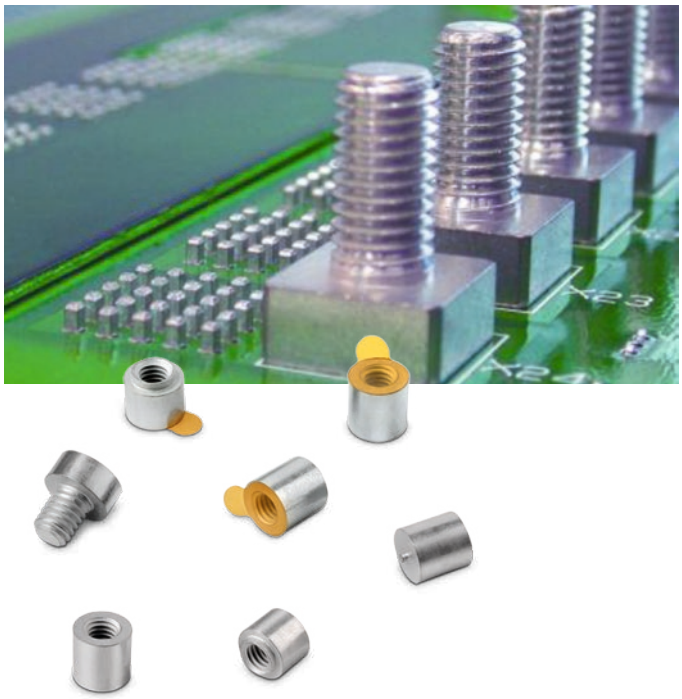
The costs in this example can be practically halved. Also impressive is the enormous potential for savings in the set-up costs that are, in absolute terms, especially crucial for small quantities.

Further system-dependent benefits result from the lower copper content = lower thermal capacity:
- Clear simplification of the soldering process, saving on processing costs for special soldering processes, higher yield
- Manual and selective soldering is now possible, also in the case of repairs
- Noticeable weight reduction

Power elements

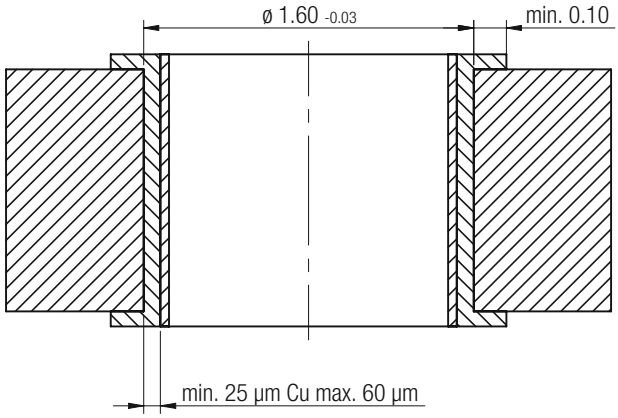
Power elements are suitable for connecting to Wirelaid circuit boards. In SMD technology, they can be fully automatically assembled, can be used up to 50 A and offer very high retention forces and torques. In press-fit technology, they are also available for currents up to 300 A and down to an M10 connection thread.



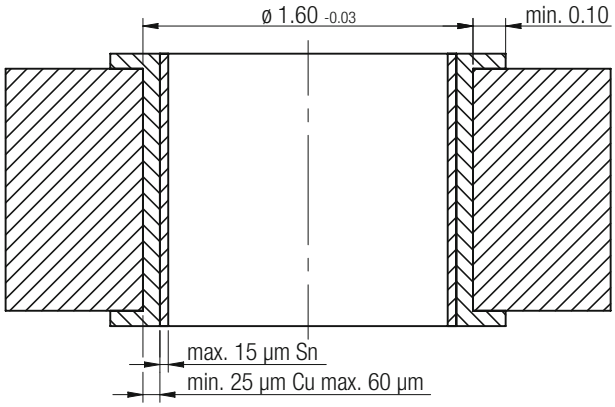


The following specifications apply to press-fit technology:

Borehole specification for chemical surfaces



Borehole specification for HAL



! More information about high-current applications in combination with logic can be found here: www.we-online.de/power

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