YAMAHA

YMF807

APL-3
Automobile PLayer-3

■ General Description

YMF807 is a synthesizer LSI designed with in-car use, which is for playing back high-quality operational sounds, alarm sounds, etc. The synthesizer block includes Yamaha-original FM synthesizer and ADPCM decoder. The FM synthesizer allows for high-quality sound creation by parameter designation with only several tens of bytes, and the ADPCM decoder allows for a playback of voice guidance etc.

The built-in hardware sequencers allow up to four kinds of sound contents to be played back simultaneously without giving heavy load to a host CPU. Even in the middle of a playback, its playback time and volume can be controlled by using simple commands; therefore, it is possible to vary an alarm sound etc. in accordance with degree of risk in real time.

In addition, a speaker amplifier with 520mW output supports direct connection of a speaker. This allows an in-car sound system to be configured with a few components.

YAMAHA CORPORATION

YMF807 Catalog
CATALOG No.: LSI-4MF807A42
2009.6

■ Features

- **CPU Interface**
  - ▼ Clock-synchronized Serial Interface (SPI-compliant interface)
  - ▼ Data Communication at up to 20MHz

- **Synthesizer Function**
  - ▼ FM synthesizer capable of generating up to 16 tones simultaneously, and Monaural Hybrid Synthesizer of ADPCM Decoder
    - ➢ Supports 8bitPCM / 4bitADPCM stream playback
    - ➢ FM synthesizer supports 16-tone simultaneous playback

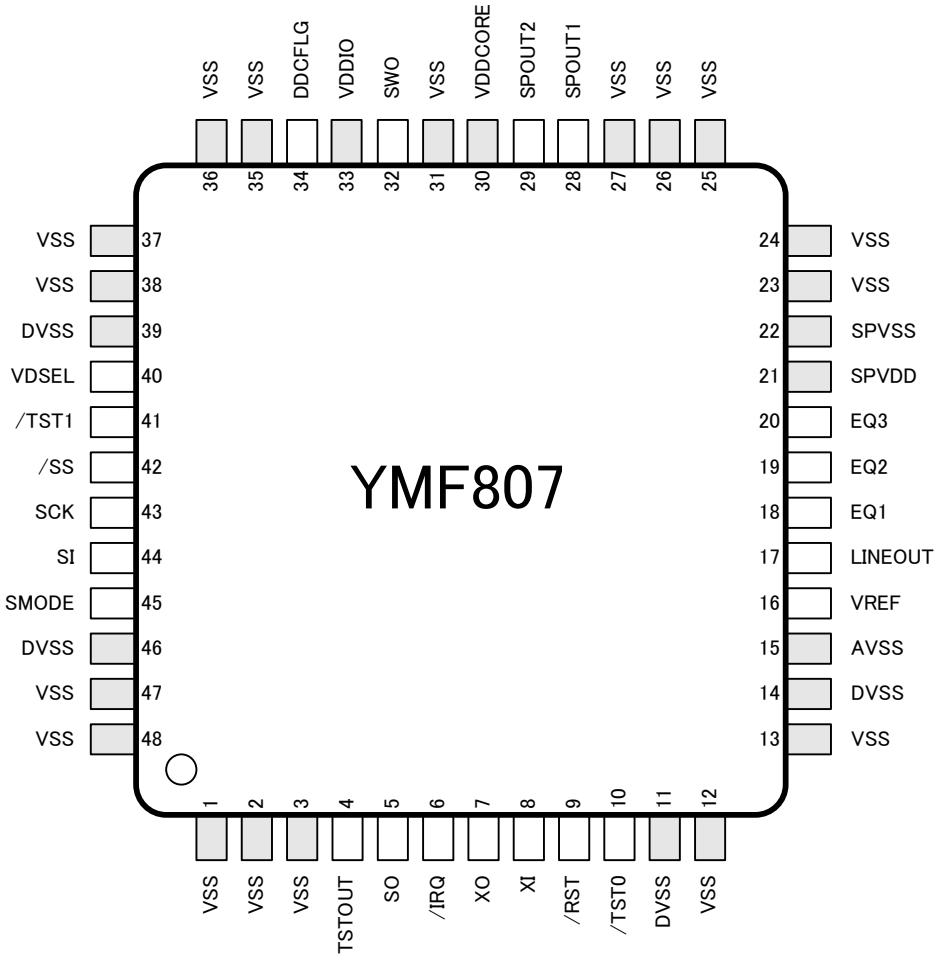
- **Sequencer Function**
  - ▼ 4 sequencers: each of them plays back one sound content.
  - ▼ 1kbyte buffer for each sequencer
    - ➢ For FM contents, basically its data size is within 1kbyte, and this allows it to be downloaded into the buffer whole for playback.
    - ➢ For sound contents beyond 1kbyte, it is played back while HostCPU is supplying data into the buffer by the interrupt processing.
  - ▼ Asynchronous overlapping playback with 4 types of sound contents
    Example: simultaneous playback of hazard sound, reverse sound, sonar sound, and operational sound
  - ▼ Simultaneous playback / Loop playback / Stop controls of multiple sequencers
  - ▼ Individual volume and playback time setting for each sequencer (sound contents)

- **Sound Contents**
  - ▼ 2 types: melody contents and voice contents
    - ➢ Melody Contents : Sound Contents of FM synthesizer
    - ➢ Voice Contents : Sound Contents of 8bitPCM / 4bitADPCM
  - ▼ Yamaha authoring tool realizes its creation. Hardware format for APL-3
  - ▼ No data size limitation. Download playback of data less than 1kbyte

- **Audio Output**
  - ▼ 16-bit monaural D/A converter
  - ▼ Monaural Line Output
  - ▼ Monaural Speaker Output (Built-in speaker amplifier: Max. 520mW, RL=8Ω)

- **Device Specification**
  - ▼ Package : Lead-free 48-pin SQFP (Exposed stage)
  - ▼ Supply Voltage : 5V /3.3V single power supply (5V to 3.3V Step-down DC converter is included.)
  - ▼ Operating Ambient Temperature: -40℃ to +105℃

Pin Configuration



< 48-pin SQFP TOP VIEW >

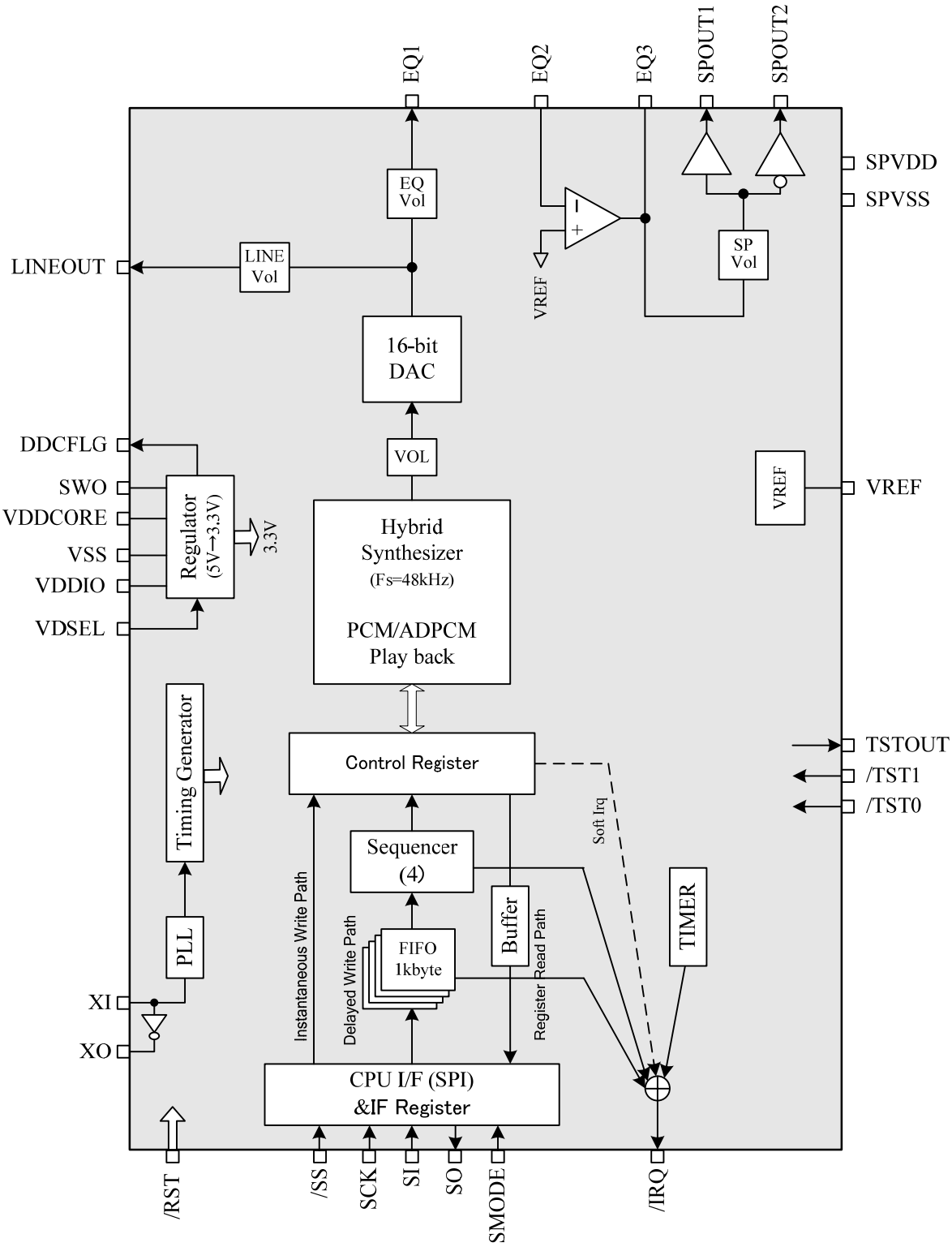
Pin Function List

No.	Pin Name	I/O	Power	Function
1	VSS	—	—	Ground, Heat Sink
2	VSS	—	—	Ground, Heat Sink
3	VSS	—	—	Ground, Heat Sink
4	TSTOUT	O	VDDIO	Test Output. This pin should be NC (No Connection).
5	SO	OT	VDDIO	CPU Interface Serial Data Output
6	/IRQ	O	VDDIO	Interrupt Output
7	XO	O	VDDIO	Clock Output Pin
8	XI	I	VDDIO	Clock Input Pin
9	/RST	Ish	VDDIO	Hardware Reset Input
10	/TST0	I	VDDIO	Test Input. This pin should be connected to VDDIO.
11	DVSS	—	—	Digital Ground, Heat Sink
12	VSS	—	—	Ground, Heat Sink
13	VSS	—	—	Ground, Heat Sink
14	DVSS	—	—	Digital Ground, Heat Sink
15	AVSS	—	—	Analog Ground, Heat Sink
16	VREF	A	VDDCORE	Analog Reference Voltage Connect a capacitor of 0.1μF between this pin and AVSS.
17	LINEOUT	A	VDDCORE	LINEOUT output pin
18	EQ1	A	VDDCORE	Equalizer pin 1
19	EQ2	A	VDDCORE	Equalizer pin 2
20	EQ3	A	VDDCORE	Equalizer pin 3
21	SPVDD	—	—	Supply Voltage for a speaker
22	SPVSS	—	—	Ground, Heat Sink
23	VSS	—	—	Ground, Heat Sink
24	VSS	—	—	Ground, Heat Sink
25	VSS	—	—	Ground, Heat Sink
26	VSS	—	—	Ground, Heat Sink
27	VSS	—	—	Ground, Heat Sink
28	SPOUT1	A	SPVDD	Speaker Output Pin 1
29	SPOUT2	A	SPVDD	Speaekr Output Pin 2
30	VDDCORE	—	—	Regulator Sense Input and Supply Voltage (3.3V) for internal core
31	VSS	—	—	Regulator Ground
32	SWO	A	—	Regulator Switching Output
33	VDDIO	—	—	Supply Voltage (Typ. +5.0V or +3.3V)
34	DDCFLG	O	VDDIO	Overcurrent Detection Flag Output Pin
35	VSS	—	—	Ground, Heat Sink
36	VSS	—	—	Ground, Heat Sink
37	VSS	—	—	Ground, Heat Sink
38	VSS	—	—	Ground, Heat Sink
39	DVSS	—	—	Digital Ground, Heat Sink
40	VDSEL	I	VDDIO	Supply Voltage Selection Input (L: 5V, H: 3.3V)
41	/TST1	I	VDDIO	Test Input. This pin should be connected to VDDIO.
42	/SS	I	VDDIO	CPU Interface Chip Select
43	SCK	I	VDDIO	CPU Interface Serial Transfer Clock Input
44	SI	I	VDDIO	CPU Interface Serial Data Input
45	SMODE	I	VDDIO	CPU Interface Mode Selection
46	DVSS	—	—	Digital Ground, Heat Sink
47	VSS	—	—	Ground, Heat Sink
48	VSS	—	—	Ground, Heat Sink

I : Digital Input Pin
O : Digital Output Pin
OT : Tri-state Output Pin
Ish : Schmitt Input Pin
A : Analog Pin

(Caution)
VSS, DVSS, AVSS, and SPVSS pins are interconnected in a device and used also as a heat sink.
Therefore, connect them on the same ground plane.

Block Diagram



● **CPU Interface**

SPI (Serial Peripheral Interface) is used as CPU interface.
The following four lines are expected to be connected to an external CPU: Chip Select (/SS), Serial Clock (SCK), Data Input (SI), and Data Output (SO).
This is a block that controls writing and reading data according to input data from SI pin.

● **I/F Register**

This is the register that can be directly accessed by an external CPU.
"Control Register" described in the next paragraph is accessed through this register.
There are many registers that control various functions in it.

● **Control Register**

This is the register that is accessed via a sequencer.
There are registers that mainly control synthesizer block located in the latter stage in it.
Basic waveform data for FM are stored in a ROM.

● **Delayed FIFO**

FIFO is an abbreviation of First In First Out, which is a memory from which data can be read in the same order of data written.
There are four FIFOs and each of them can be read through the I/F register.
This FIFO is used in the "Delayed Write Path", which is for accessing Control Register after time management in a sequencer. The size of an FIFO is 1024 bytes.

● **Sequencer**

This is the block that interprets data written into the delayed write path.
There are four sequencers and each of them supports four delayed FIFOs.
The structure of data written into the delayed write path is "Time information data + Register setting data". A sequencer interprets time information data to count time and makes the setting of registers after the time elapsed.
Generally, "Music data" is written into the delayed write path.
This sequencer has a role on playing back music by interpreting music data and controlling synthesizer block.

● **Synthesizer Block**

This block includes a synthesizer that is capable of simultaneous sound generation up to 16 tones in FM and up to four tones in PCM/ADPCM.
FM synthesizer has "four operation modes in 16 tones".
To create more complicated voices is possible because any waveforms for FM calculation can be set.
This synthesizer supports 8-bit PCM or 4-bit ADPCM data format, and this allows for stream playback.
The sampling frequency is 48 kHz.

● **DAC Block**

This block converts digital signals from the synthesizer block into analog signals. Its data length is 16 bits.

● **Line Out Output Block**

A monaural analog output is prepared for Line Out.

● **EQ Amplifier Block**

Adjusting registers and capacitors connected as external components allows filter characteristics and Gain to be changed.

- **Speaker Amplifier Block**

  A speaker amplifier with max. 520mW output at SPVDD=3.3V is included.

  There is a volume that controls its output level at the former stage of the amplifier.

- **Clock Generation Block**

  A clock ranging from 2 to 27MHz should be input.

  This is a block that generates clocks required for operation in LSI.

■ Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
VDDIO pin Supply Voltage	VDDIO	-0.3	6.0	V
VDDIO pin Current Limit	VDDIOA		4	A
VDDCORE pin Supply Voltage	VDDCORE	-0.3	4.6	V
SPVDD Supply Voltage	SPVDD	-0.3	4.6	V
Analog Input Voltage	V_{INA}	-0.3	VDDCORE+0.3	V
Digital Input Voltage	V_{IND}	-0.3	VDDIO+0.3	V
Power dissipation (*1)	Pd		2645	mW
Speaker Load Resistance	R_{LSP}	6.4		Ω
Storage Temperature	T_{STG}	-50	125	℃

Condition: VSS = 0V

(*1) Take this value as a reference because it is calculated by simulation based on a certain environment condition.
Top= 25℃, and when mounted on a glass epoxy PCB(114.3 mm×76.2 mm×1.6 mm) with the exposed bottom pad not soldered.
When operating above Top= 25℃, the value decreases 26.5 mW per 1 ℃.

(Ref.) The table below shows the maximum power dissipation calculated by a simulation based on the following conditions: bottom pad soldering (Soldered/Not Soldered), board wiring density, and operating ambient temperature (Top).

Bottom Pad Soldering	Wiring Density	PKG Thermal Resistance	Max. Power Dissipation	
			Top=25℃	Top=105℃
Not Soldered	150%	37.8℃/W	2645mW	529mW
Soldered	150%	22.0℃/W	4545mW	909mW
Not Soldered	200%	35.8℃/W	2793mW	558mW
Soldered	200%	20.3℃/W	4926mW	985mW

Recommended Operating Conditions

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
VDDIO operating voltage	VDSEL=0V	VDDIO	4.75	5.0	5.25	V
	VDSEL=VDDIO		3.0	3.3	3.6	V
VDDCORE operating voltage		VDDCORE	3.0	3.3	3.6	V
SPVDD operating voltage		SPVDD	3.0	3.3	3.6	V
Operating ambient temperature		T_{OP}	-40	25	105	℃

Condition: VSS = 0V

(Caution)

VDSEL=0V:
Connect SWO pin to VDDCORE and SPVDD pins through an external L and C.
A 5V switching voltage outputting to SWO pin is stepped down to 3.3V through the L and C.

VDSEL=3.3V:
Connect VDDCORE, SPVDD, and VDDIO pins to a 3.3V power supply.
SWO pin should remain open.

Consumption Current

● VDSEL=0V

Parameter	Conditions	Typ.	Max.	Unit
VDDIO consumption current	At normal operation (*) / No sound generation	20		mA
	At normal operation (*)/ SPOUT: at 8Ω load, 300mW output	154		mA
	At power-down state	1.4	2.0	mA

(*): VDDIO=5.00V, Top=25℃, Input Pins: V_{IL}=VSS, V_{IH}=VDDIO

● VDSEL=VDDCORE

Parameter	Conditions	Typ.	Max.	Unit
VDDIO+VDDCORE+ SPVDD consumption current	At normal operation (*) / No sound generation	19		mA
	At normal operation (*)/ SPOUT: at 8Ω load, 300mW output	195		mA
	At power-down state	10	27	μA

(*): VDDIO=VDDCORE=SPVDD=3.30V, Top=25℃, Input Pins: V_{IL}=VSS, V_{IH}=VDDIO

DC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage "H" level ①	V_{IH}	(*1)	0.7 × VDDIO			V
Input voltage "L" level ①	V_{IL}	(*1)			0.2 × VDDIO	V
Input voltage "H" level ②	V_{IH}	(*2)	0.7 × VDDIO			V
Input voltage "L" level ②	V_{IL}	(*2)			0.2 × VDDIO	V
Output voltage "H" level	V_{OH}	(*3) IOH = -1mA	0.8 × VDDIO			V
Output voltage "L" level	V_{OL}	(*3) IOL = +1mA			0.4	V
Schmitt Width	Vsh			0.5		V
Input Leakage Current	IL		-1		1	μA
Input Capacitance	CI				10	pF

Conditions: Top= -40 to 105℃, VDDIO=3.0 to 3.6V or 4.75 to 5.25V, Capacitor load=50pF

(*1) Target pins: /SS, SCK, SI, SMODE, /RST, VDSEL, /TST0, /TST1

(*2) Target pins: XI

(*3) Target pins: SO, /IRQ

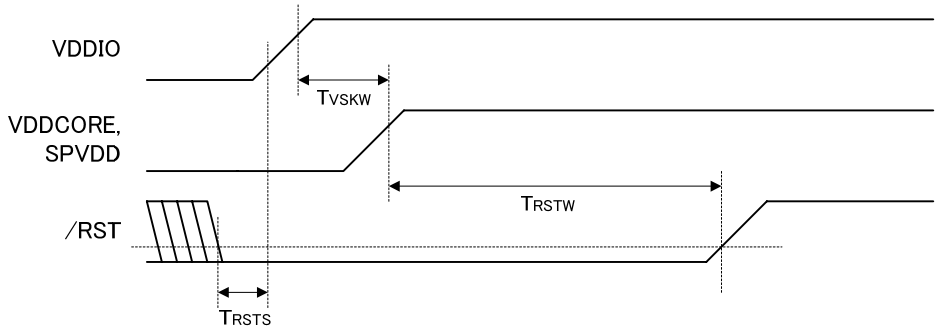
AC Characteristics

/RST, XI, and other input signals

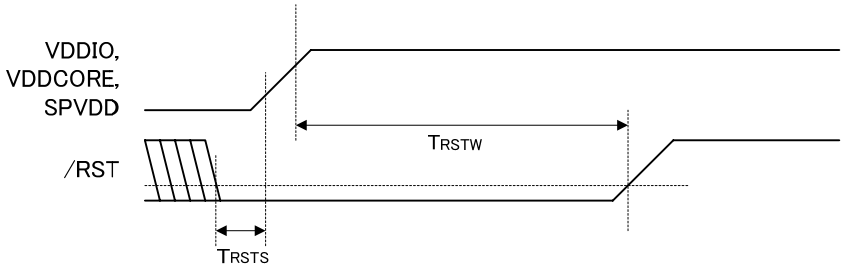
Parameter	Symbol	Min.	Typ.	Max.	Unit
/RST "L" Pulse Width	T_{RSTW}	100			µs
/RST (undefined → "L") Setup Time	T_{RSTS}	0			ms
Supply voltage Start-up Delay	T_{VSKW}			1	ms
XI frequency	1 / Tfreq	2		27	MHz
XI rise and fall time	Trckc, Tfckc			30	ns
XI duty	Th / Tfreq	30	50	70	%
Input signals other than XI rise and fall time	Tr, Tf			20	ns

Conditions: Top=-40 to 105℃, VDDIO=4.75 to 5.50[V], Capacitor load=50pF
The measurement points are at V_{IH}= 0.7×VDDIO, V_{IL}=0.3×VDDIO, V_{OH}=0.8×VDDIO, and V_{OL}=0.2×VDDIO.

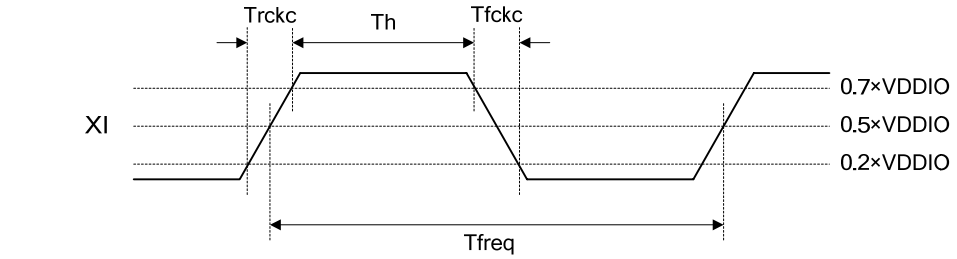
● VDSEL=0V

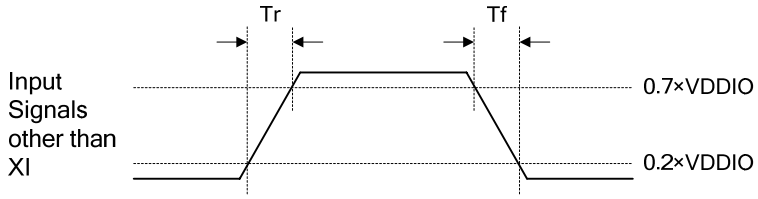


● VDSEL=VDDCORE



The width of a reset signal is defined from the time when VDDCORE rose up to the level of 70%.
/RST input must be already settled at "L" level when VDDIO rises up to the level of 30%.



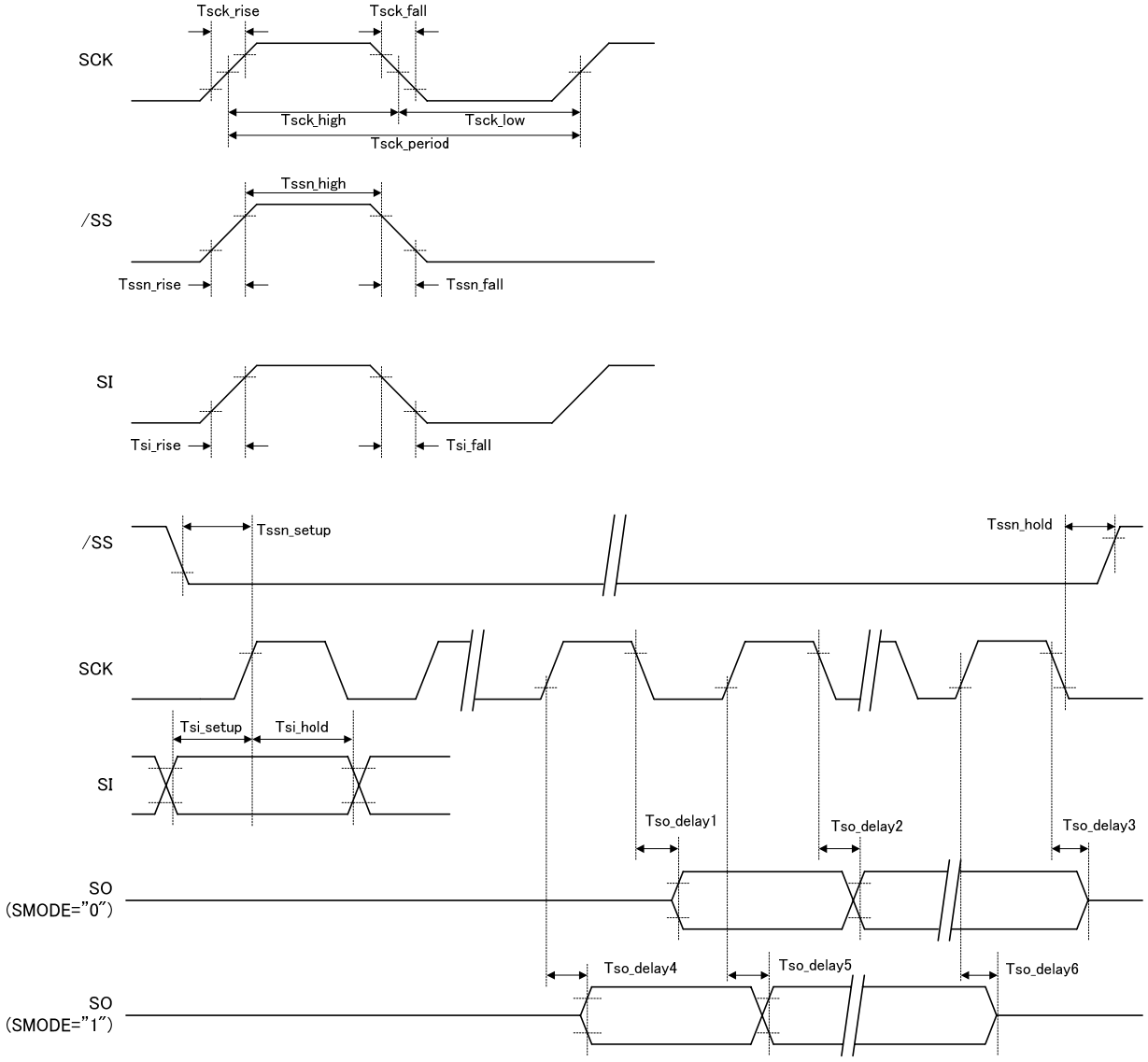


CPU Interface

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK Period	Tsck_period	50			ns
SCK "L" Pulse Width (*1)	Tsck_low	24			ns
SCK "H" Pulse Width (*1)	Tsck_high	24			ns
SCK Rise Time	Tsck_rise			5	ns
SCK Fall Time	Tsck_fall			5	ns
/SS "H" Pulse Width (*2)	Tssn_high	650 / 50			ns
/SS Rise Time	Tssn_rize			5	ns
/SS Fall Time	Tssn_fall			5	ns
SI Rise Time	Tsi_rize			5	ns
SI Fall Time	Tsi_fall			5	ns
/SS Setup Time	Tssn_setup	15			ns
/SS Hold Time	Tssn_hold	5			ns
SI Setup Time	Tsi_setup	15			ns
SI Hold Time	Tsi_hold	5			ns
SO Output Delay 1 (SMODE= "0")	Tso_delay1			12	ns
SO Output Delay 2 (SMODE= "0")	Tso_delay2			21	ns
SO Output Delay 3 (SMODE= "0")	Tso_delay3			12	ns
SO Output Delay 4 (SMODE= "1")	Tso_delay4			12	ns
SO Output Delay 5 (SMODE= "1")	Tso_delay5			21	ns
SO Output Delay 6 (SMODE= "1")	Tso_delay6			12	ns

Conditions: T_{OP}=-40 to 105℃, VDDIO=4.75 to 5.25[V], or VDDCORE=3.0 to 3.6[V], Capacitor load=50pF
I_{OH}=-2.0mA, I_{OL}=+2.0mA (S0 pin)
The measurement points are at V_{IH}= 0.7×VDDIO, V_{IL}=0.2×VDDIO, V_{OH}=0.8×VDDIO, and V_{OL}=0.2×VDDIO

(*1) Tsck_low + Tsck_high should be more than Tsck_period(min.).
(*2) To read data from the control register by using IF Register (BANK1/#11 and #12), a pulse width of /SS ("H") between #11 access and #12 access is 650ns (min.). In other cases, it becomes 50ns (min.).


Tsck_rise
Tsck_fall
SCK
Tsck_high
Tsck_low
Tsck_period
Tssn_high
/SS
Tssn_rise
Tssn_fall
SI
Tsi_rise
Tsi_fall
/SS
Tssn_setup
Tssn_hold
SCK
Tsi_setup
Tsi_hold
SI
Tso_delay1
Tso_delay2
Tso_delay3
SO
(SMODE="0")
Tso_delay4
Tso_delay5
Tso_delay6
SO
(SMODE="1")

Analog Characteristics

Conditions: T_{OP}=25℃, VDDCORE=3.3V, and VDDIO=5.0V

○ SP Amplifier

Parameter	Min.	Typ.	Max.	Unit
Gain Setting (fixed)		±2		times
Speaker Load Resistance (RL)		8		Ω
Maximum Output Voltage Amplitude (RL=8Ω)		5.7		Vp-p
Maximum Output Power (RL=8Ω, THD+N ≤ 1.0%)		520		mW
THD + N (RL=8Ω, f=1kHz, 400mW output)		0.025		%
Noise in no signal condition (A-filter: weighting filter)		-90		dBV
PSRR (f=1kHz)		90		dB
Amplitude Center Voltage		0.5×SPVDD		V
Differential Output Voltage		10	50	mV
Maximum Load Capacitance applicable to SPOUT1 and SPOUT2 pins (*)			1000	pF

(*): This means a capacitance up to 1000pF can be connected to both SPOUT1 pin and SPOUT2 pin.

○ EQ Amplifier

Parameter	Min.	Typ.	Max.	Unit
Available Gain Setting Range			30	dB
Maximum Output Voltage Amplitude		3.0		Vp-p
THD + N (f=1kHz)			0.05	%
Noise in no signal condition (A-filter)		-90		dBV
Input Impedance	10			MΩ
Feedback Resistance between EQ2 and EQ3	20			kΩ

○ SP Volume

Parameter	Min.	Typ.	Max.	Unit
Volume Setting Range	-30		0	dB
Volume Step Width		1		dB
Attenuation Rate at Mute	80			dB

○ EQ Volume

Parameter	Min.	Typ.	Max.	Unit
Volume Setting Range	-30		0	dB
Volume Step Width		1		dB
Attenuation Rate at Mute	80			dB
Minimum Load Resistance		20		kΩ
Maximum Output Voltage Amplitude		1.65		Vp-p
Output Impedance		300	600	Ω

○ LINE Volume

Parameter	Min.	Typ.	Max.	Unit
Volume Setting Range	-30		0	dB
Volume Step Width		1		dB
Attenuation Rate at Mute	80			dB
Minimum Load Resistance		20		kΩ
Maximum Output Voltage Amplitude		1.65		Vp-p
Output Impedance		300	600	Ω

○ VREF

Parameter	Min.	Typ.	Max.	Unit
VREF voltage		0.5×VDDCORE		V

○ DAC

Parameter	Min.	Typ.	Max.	Unit
Resolution		16		Bit
Full-scale Output Voltage		1.65		Vp-p
THD+N (f= 1kHz)			0.5	%
Noise in no signal condition (A-filter)		-90		dBV
Frequency Characteristics (f=50Hz to 20kHz)	-3.0 (*)		+0.5	dB

(*) This is because degradation of the high-frequency response due to aperture effect.

Step-down DC-DC Converter

○ Switching Power Supply Capacitor

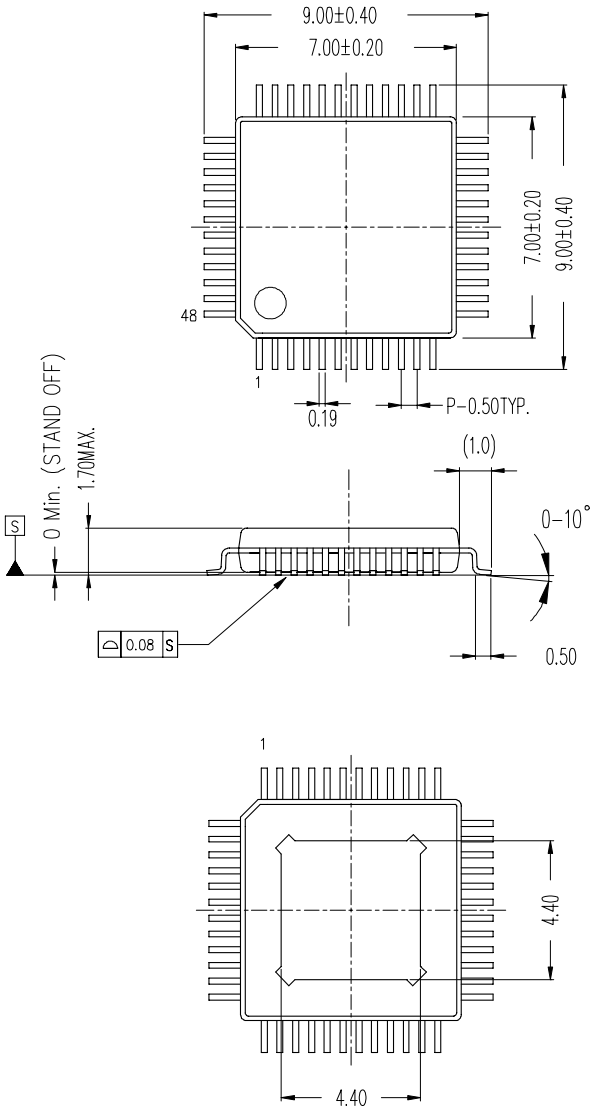
Parameter	Min.	Typ.	Max.	Unit
Rated Value	15.4	22	28.6	μF
Rated Ripple Current Value	3.0			A

○ Switching Power Supply Inductor

Parameter	Min.	Typ.	Max.	Unit
Rated Value	0.7	1.0	1.3	μH
Rated Current Value	3.0			A

■External Dimensions

C-PK48SP2-2



端子厚さ/Lead Thickness : 0.17

モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位： mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
For detailed information, please contact your local Yamaha agent.

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7. INFORMATION DESCRIBED IN THIS DOCUMENT: APPLICATION CIRCUITS AND ITS CONSTANTS AND CALCULATION FORMULAS, PROGRAMS AND CONTROL PROCEDURES ARE PROVIDED FOR THE PURPOSE OF EXPLAINING TYPICAL OPERATION AND USAGE. THEREFORE, PLEASE EVALUATE THE DESIGN SUFFICIENTLY AS WHOLE SYSTEM UNDER THE CONSIDERATION OF VARIOUS EXTERNAL OR ENVIRONMENTAL CONDITIONS AND DETERMINE THEIR APPLICATION AT THE CUSTOMER'S OWN RISK. YAMAHA SHALL ASSUME NO RESPONSIBILITY FOR CLAIMS, DAMAGES, COSTS AND EXPENSES CAUSED BY THE CUSTOMER OR ANY THIRD PARTY, OWING TO THE USE OF THE ABOVE INFORMATION.

PRECAUTIONS AND INSTRUCTIONS FOR SAFETY

⚠ WARNING

Prohibited	Do not use the device under stresses beyond those listed in Absolute Maximum Ratings (current, voltages, safety operation ranges, temperature, etc.). Such stresses may become causes of breakdown, damages, or deterioration, causing explosion or ignition, and this may lead to fire or personal injury.
Prohibited	Do not mount the device reversely or improperly and also do not connect a supply voltage in wrong polarity. Otherwise, this may cause current and/or power-consumption to exceed the absolute maximum ratings, causing personal injury due to explosion or ignition as well as causes of breakdown, damages, or deterioration. And, do not use the device again that has been improperly mounted and powered once.
Prohibited	Do not short between pins. In particular, when different power supply pins, such as between high-voltage and low-voltage pins, are shorted, smoke, fire, or explosion may take place.
Instructions	As to devices capable of generating sound from its speaker outputs, please design with safety of your products and system in mind, in case of the occurrence of unusual speaker output due to a malfunction or failure. A speaker radiates heat in a voice-coil by air flow accompanying vibration of a diaphragm. When a DC signal (several Hz or less) is input due to device failure, heat radiation characteristics degrade rapidly, thereby leading to voice-coil burnout, smoke, or ignition of a speaker even if it is used within the rated input value.

⚠ CAUTION

Prohibited	Do not use Yamaha products in a position close to burning materials, combustible substances, or inflammable materials, in order to prevent the spread of the fire caused by Yamaha products, and to prevent the smoke or fire of Yamaha products due to peripheral components.
Instructions	Generally, semiconductor products may malfunction and break down due to aging, degradation, etc. It is the responsibility of user to take actions such as safety design of products and the entire system and also fail-safe design according to applications, so as not to cause property damage and/or bodily injury due to malfunction and/or failure of semiconductor products.
Instructions	The built-in DSP may output the maximum amplitude waveform suddenly due to malfunction from disturbances etc. and this may cause damage to headphones, external amplifiers, and human body (ear). Please pay attention to safety measures for device malfunction and failure both in product and system design.
Instructions	As semiconductor devices are not nonflammable, overcurrent or failure may cause smoke or fire. Therefore, products should be designed with safety in mind such as overcurrent protection circuit etc. so that it does not keep on flowing during operation or failure.
Instructions	Products should be designed with fail safe in mind in case of malfunction of the built-in protection circuits. Note that the built-in protection circuits such as overcurrent protection circuit and high temperature protection circuit do not always protect the internal circuits. In some cases, depending on usage or situations, such protection circuit may not work properly or the device itself may break down before the start of the protection circuit.
Instructions	Use a stable power supply. The use of unstable power supply may lead to malfunctions of the protection circuit, causing device breakdown, personal injury due to explosion, or smoke or fire.
Instructions	Product's housing should be designed with the possibility of short-circuiting between pins of the mounted device due to foreign conductive substances (such as metal pins etc.). Moreover, the housing should be designed with spatter prevention etc. due to explosion or burning. Otherwise, the spattered substance may cause bodily injury.
Instructions	The device may be heated to a high temperature due to internal heat generation during operation. Therefore, please take care not to touch an operating device directly.

YAMAHA

CREATING 'KANDO' TOGETHER

Notice The specifications of this product are subject to improvement changes without prior notice.

AGENT

YAMAHA CORPORATION

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Printed in Japan