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PL-80150
Networking Appliance
User's Manual
Version 1.2

2U Rackmount Dual Inte l® Sandy Bridge-EP / Ivy Bridge-EP E5-26 600 Series Processor and C604 PCH Network System, 8 PCIe x8 supports LAN expansion modules, IPMI, 2 USB , 1 SATA HDD , 2 GbE, CF, 1 PCIe x8 slot, redundant PSU

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Revision History			
Date	**Version**	**Modification**	**Editor**
20113/08/07	1.0	First Release	Denny Huang
20113/08/17	1.2	Fixed one error to Operation for R287 screen information & System Screen supporting definition	Denny Huang

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1.11 Introduction

The PL-801500, an Intel® Sandy Bridge-EP / Ivy Bridge-EP Xeon processor-based platform, was developed for maximum performance, scalability and functionality in a 2U network service appliance. Two Intel® QuickPath Interconnects running up to 8.0GT/ss speeds which can combine with h Intel® Xeon® E5-2600 series processor (Socket RR) in their respective two sockets can reduce cross-socket memory I/OO latencies and increase throughput. Two E 5-2600 series processor with up to 10 cores, 20MBB cache an d latest PCIe 3.0 interface which provide a total of 80 PCIe lanes up to 8Gbps per lane. Each CPU socket supports 4 DDRR3 channels with speeds up to 16600/1866 MHz and maximum capacity up too128 GB of ECC memory when using the latest LR DDIMM technology. The Intel® C6004 chipset supports standard platform I/O and highest speed mass storage which supports one 33.5” SATA hard disks or solid state drives. The SCB-96550 platform can offer different types of expansion module; such as 10Gigabit SFP+, Gigabit copper with by-pass function and Gigabit fiber ports. Tithe max capacity can provide 644 ports.

1.22 Specifications

Processor System	CPU	Supports Quad Intel® Sandy Bridge-EP/Ivy Bridge-EP E5-2600 series, LGA 2011
	Chipset	Intel® Patsburg C604 PCH
	QPI	QPI up to 8GT/s
	BIOS	AMI® 64Mbit BIOS
Memory	Technology	Total 8 DIMMs (Four channels per CPU, one DIMM per channel, four DIMMs per CPU) 1. ECC/Registered DDR3 1600/1866 MHz memory, up to 16 GB per DIMM 2. LRDIMM: DDR3 1600 MHz, up to 16GB per DIMM
	Capacity	ECC UDIMM/RDIMM: up to 128GB LR-DIMM: up to 128GB

Expansion	Expansion Slots	1. One SO-DIMM slot IPMI card with VGA support 2. One PCIe x8 slots in PCIe x16 slot 3. 8 x PCIe x8 connector for expansion LAN module
Ethernet	Ethernet Modules (Optional)	R288: 8 x SFP GbE ports, Intel 82580EB R289: 8 x RJ45 GbE ports with two pairs bypass, Intel 82580EB R290: 2 x 10GbE SFP+ ports, Intel 82599ES R293: 2 x 10GbE RJ45 ports, Intel X540-BT2
Hardware Acceleration Modules	Crypto-graphics	Optional: Cavium CN3530 module
Storage	SATA HDD	One 3.5" SATA HDD
	RAID	Supports software, RAID 0,1,5,10
	CompactFlash	One CompactFlash Type I/II
Front Panel Accessible I/O	USB Port	Two external USB 2.0
	Console Port	One Rj45 console port (COM1, RS232)
	Management Port	One GbE port, Intel 82574L One IPMI port support
	Display Port	One VGA pin header R287 needs plug in R286 (optional)
Power Supply	Watt	2U 810W ATX redundant power supply
Mechanical and Environmental	Form Factor	2U rackmount appliance
	LCD Module	One 16 x 2 LCD display
	Keypad	Four-button keypad
	LEDs	One Power LED (Green) One HDD LED (Yellow) One Status LED (Green/Yellow via programmable GPIO)
	Dimensions Operating Temperature	430mm (W) x 626mm (D) x 88mm (H); 16.9" W x 24.6" D x 3.4" H 0° ~ 40°C (32° ~ 104°F)
	Storage Temperature	-20° ~ 75°C (-4° ~ 167°F)
	Humidity	10 ~ 85% relative humidity, non-operating, non-condensing
Weight	1 pc/CTN, 20 kgs	
Certifications	CE/FCC	
Ordering Information		

PL-80150	2U rackmount dual Intel Sandy Bridge-EP / Ivy Bridge-EP Xeon ES-2600 Series processor and C604 PCH Network System, 8X PCIe x8 expansion LAN module, 2 USB, 1 SATA HDD, 2 GbE, CF, 1 PCIe x8 slot
R287A	IPMI card with VGA support
R288A	Expansion module with 8 SFP, Intel 82580EB
R289A	Expansion module with RK45 GbE ports, Intel 82580EB
R290A	Expansion module with 2 SFP+ 10 GbE ports, Intel 82599ES
R293A	Expansion module with 2 RJ45 10GbE ports, Intel x540-BT2
DK002	**Cable Expansion Kit** CB-CO5204-00 cross over 2M CB-DB9200-01 null modem cable 2M CB-EC5200-00 Ethernet Cat. 5 cable 2M CB-IPS200-00 KBMS cable, 15cm CB-IUS2B-00USB cable, 25cm CB-IVGA-00 VGA cable, 20cm CB-RJDB91-00 RJ-45 to DB-9 cable 2M

1.44 Packaging

Please make sure that the following items have been included in the package before installation.

1 PL-80150 Appliance
2 Cables (Optional)
3 CD-ROM that contains the following folders:
- Manual
- System Driver
- Utility Tools

If any of the above items are missing or damaged, please contact your dealer or retailer from whom you purchased the PL-80150. Keep the box and carton when you probably ship or store PL-80150 in near future. After you unpack the goods, inspect and make sure the packaging is intact. Do not plug the power adapter to the appliance of PL-80150 if you already find it appears damaged.

Note: *Keep the PL-80150 in the original packaging until you start installation.*

1.55 Precautions

Please make sure you properly ground yourself before handling the PL-80150 appliance or other system components. Electrostatic discharge can be easily damage the PL-80150 appliance.

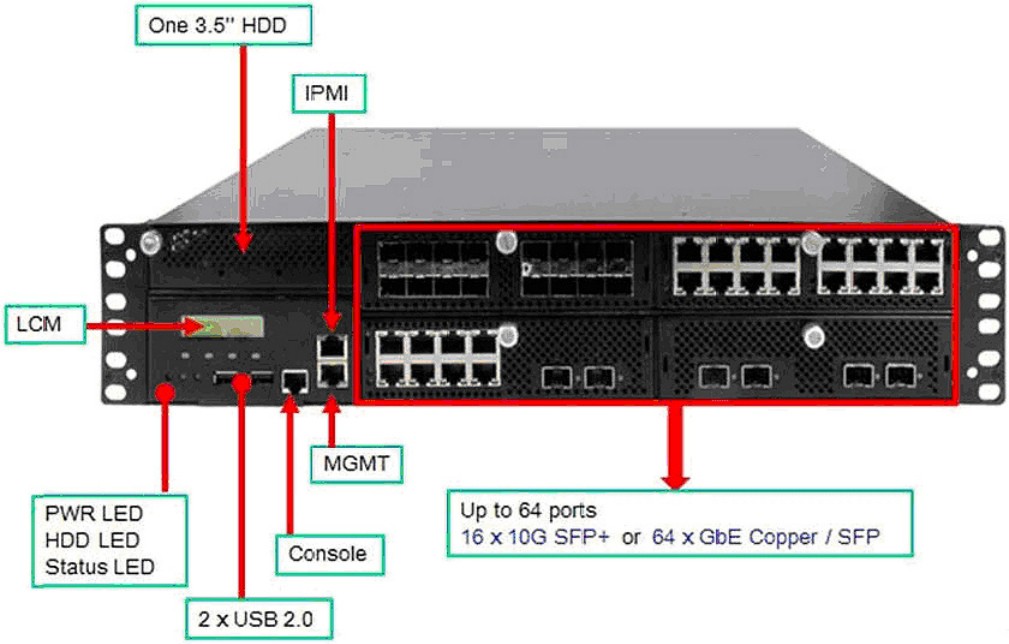
Do not remove the anti-static packing until you are ready to install the PL-80150 appliance.

Ground yourself before removing any system component from its protective anti-static packaging. To ground yourself, grasp the expansion slot covers or other unpainted parts of the computer chassis.

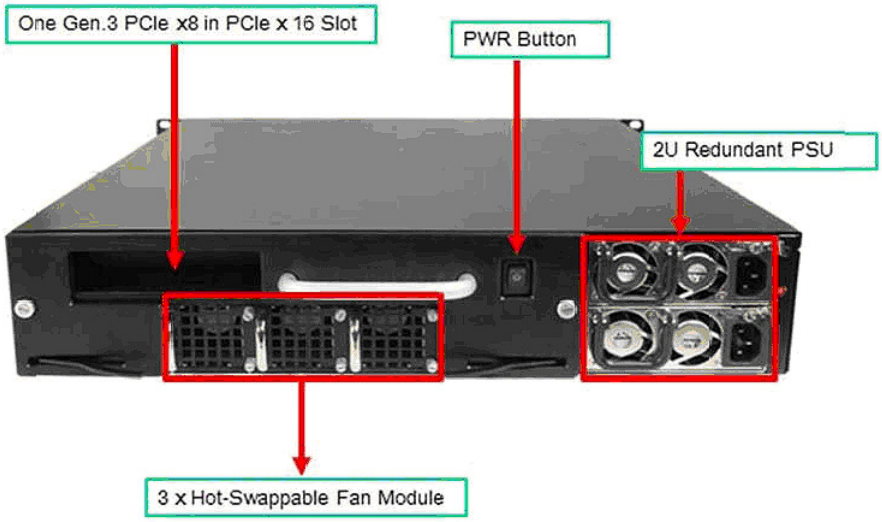
Handle the PL-80150 appliance by its edges and avoid touching the components on it.

1.6 System Layout

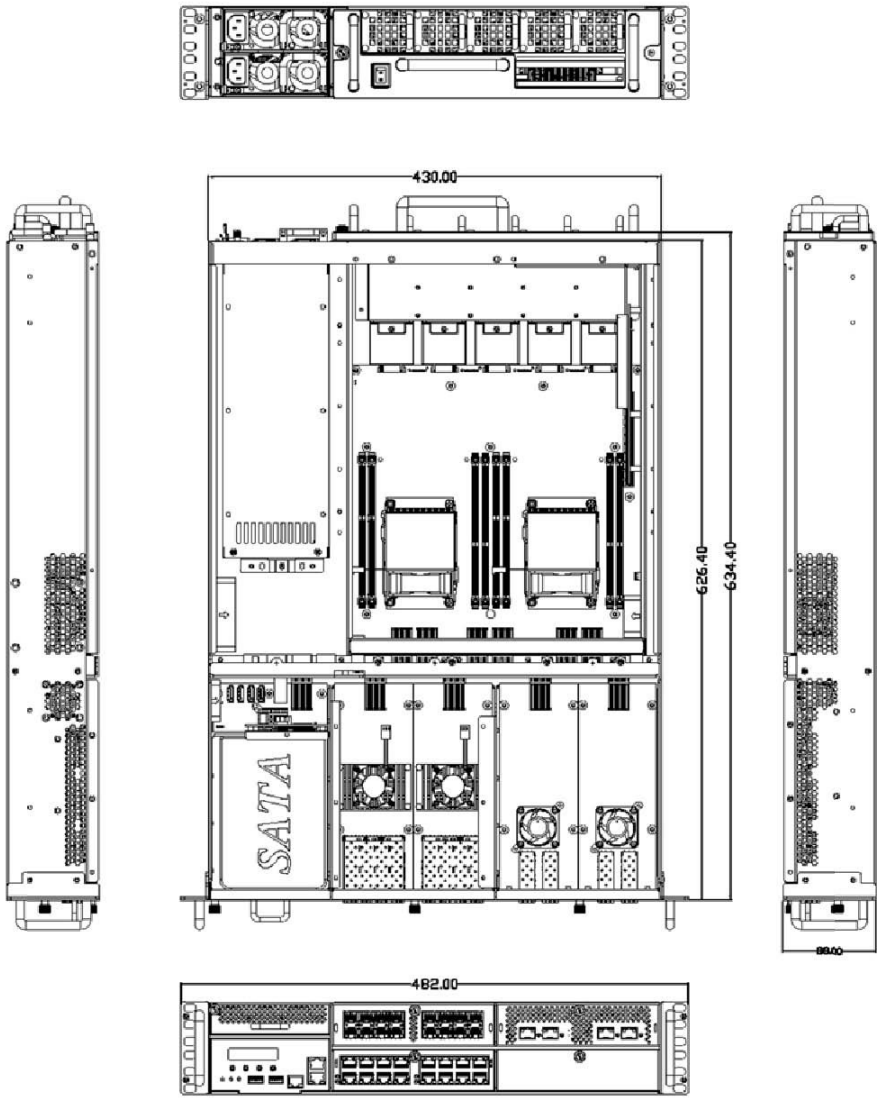
Front Panel Features



Rear panel features

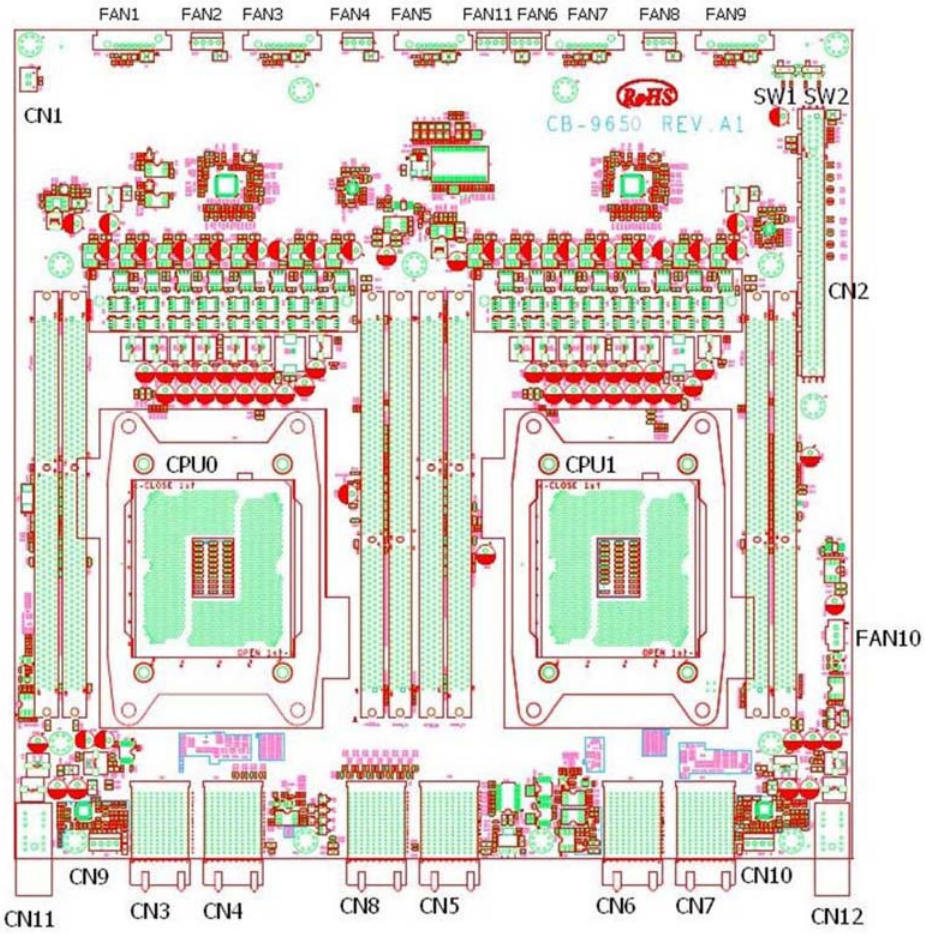


1.7 Dimensions



Chapter 22. Connector/Jumper Configuration

2.11 MB-80150 SBC Connector/Jumper Locations and Definitions

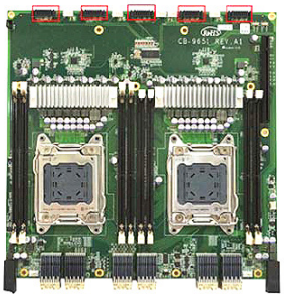


Connector/Jumper Locations & Definitions

Connector	Definitions
FAN, FAN3, FAN5, FAN7, FAN9	Smart Fan connector for Hot-swappable FAN
FAN2, FAN4, FAN6, FAN8, FAN11	4 pin Smart FAN Connector
FAN 10	FAN connector
CN1	ATX switch pin header
CN2	PCI-Ex16 slot (x8 signal)

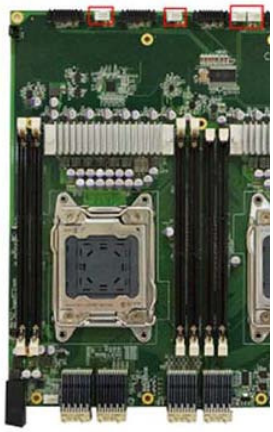
CN3-8	QPI & PCI-E BUS
CN9	CPU0 Smart FAN
CN10	CPU1 Smart FAN
CN11, CN12	+12V connector
SW1,2	CPU I D Switch

FAN1、FAN3、FAN5 、FAN7、FAN9: Smart FAN connector for Hot-swappable FAN module



Pin	Definitions
1	GND
2	Speed Detect2
3	++12V
4	N/A
5	Speed Detect1
6	N/A
7	Speed Control

FAN2, FAN4, FAN6, FAN8, FAN11: 4 pin Smart FAN Connector



Pin	Define
11	GND
22	+12V
33	Speed Detect
44	Control

FAN 10: FAN connector

Pin	Definitions
1	GND
2	+12V
3	Speed Detect

Pin	Define
1	GND
2	PS_ON#

CN9-10：CPU SMART FFAN

Pin	Definition
1 2	GND +12V
3	Speed Detect
4	Control

SW1, SW2: CPU ID

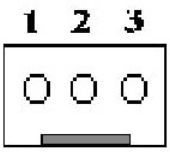
	
Pin B-C	**Setting** CPU0++1 (CB-96550)

2.22 R285 Connector/Jumper Location and Definition

Connector/Jumper Locations & Definitions

Connector	Definitions
FAN1	FAN connector
CN1,2	SATA POWER connector
CN3,4,7,8	CPU0 PCI-E connector
CN5,6,9,10	CPU1 PCI-E connector
CN11	DMMI & CPLD BUS For R2 86
CN12	+5V/+3.3V connector For RR286
CN13	ATX I2C p pin header
CCN14, 15, 16	+12V input (8Pin)
CN18-233	CPPU0/1 QPI & PCI-E BUS
CN24	+12V output for CPU1
CN25	+12V output for CPU0

FAN 1: FAN connector CN11-2：SATA power connector



Pin	Define
1	GND

2	+12V
3	Speed Detect

Pin	Define
1	+12V
2	GND
3	GND
4	+5V

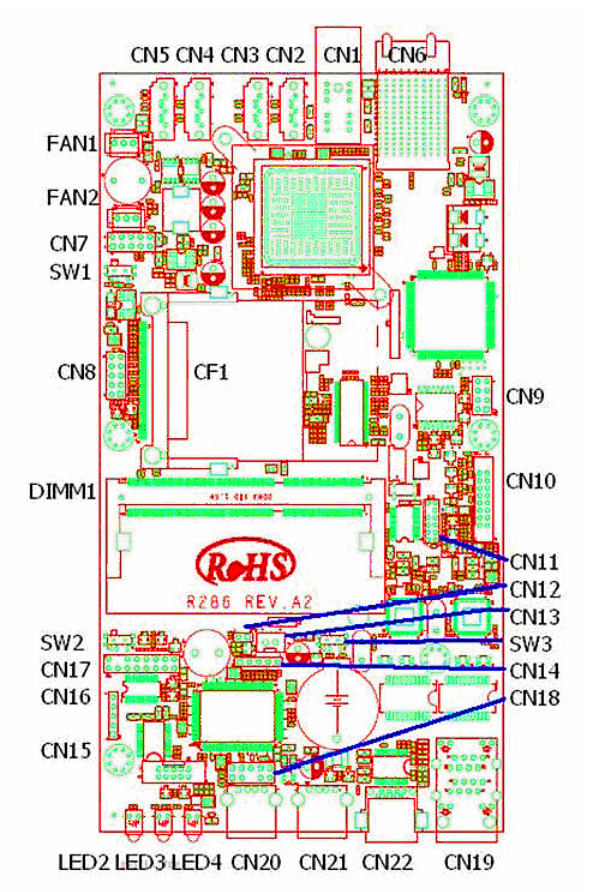
CN13：ATX I 2C pin header put (8Pin)

Pin	Define
1	SMBCLK
2	SMBDATA
3	PPCH_GP31
4	N/A
5	N/A

CN 14, 15, 16 +12V input (8Pin)

Pin	Define	Pin	Definitions
1	Ground	5	+12V
2	Ground	6	+12V
3	Ground	7	+12V
4	Ground	8	+12V

2.3 R286 Connector/Jumper Locations and Definitions

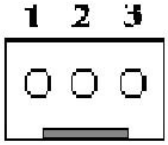


Connector/Jumper Locations & Definitions

Connector	Definitions
FAN 1-2	FAN connector
CN1	++5V/+3.3V power input
CN2--5	SATA connector
CN6	DMI & CPLD BUS
CN7	JTAG
CN8	GPO pin header
CN9	SPI programming
CN10	VGA pin header

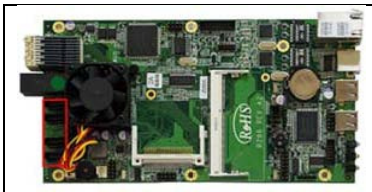
CN11	LPC pin Header
CN12	RESET pin header
CN13	Case open pin header
CN14	GPI pin header
CN15	COM2 box header
CN16	Keypad pin header
CN17	LCM pin header
CN18	PS2 KB/MS pin header
CN19	Giga LAN RJ45 connector *2port
CN20--21	USB1/2 connector
CN22	COM1 RJ455 connector
SW1	Clear CMOS
SW2	Watchdog function
SW3	ATX Switch function
DIMM1	IPMI connector
CF1	CF connector

FAN 1-2: FAN connector

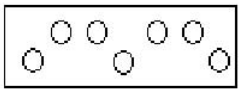


Pin	**Definitions**
1	GND
2	+12V
3	Speed Detect

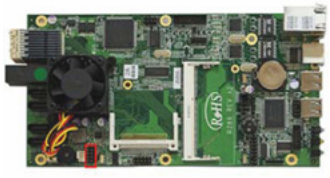
CN2-5：SATA connector

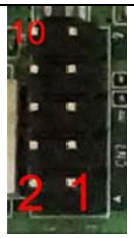


pin	Definitions
1	Ground
2	TXP
3	TXNN
4	Ground
5	RXNN
6	RXP
7	Ground



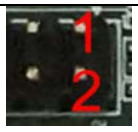
CN7：TAG





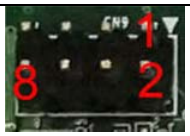
Pin	Definitions	Pin	Definitions
1	TCK	2	GND
3	TDO	4	+3.3V AUX
5	TMS	6	N/A
7	N/A	8	N/A
9	TDI	10	GND

CN8：GPO pin header



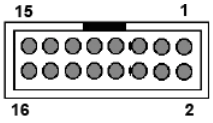
Pin	Define	Pin	Definitions
1	GPIO20#	2	+3.3V_PU
3	GPIO21#	4	+3.3V_PU
5	GPIO22#	6	+3.3V_PU
7	GPIO23#	8	+3.3V_PU
9	GND	10	+3.3V

CN9：SPI programming



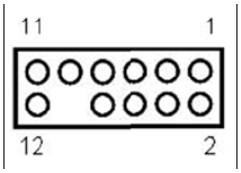
Pin	Definitions	Pin	Definitions
1	+3.3V	2	Ground
3	CS#	4	SCLK
5	MISO	6	MOSI
7	N/A	8	IO

CN10：VGA pin header



Pin	Define	Pin	Define
1	RED	2	GREEN
3	BLUE	4	N/A
5	GND	6	GND
7	GND	8	GND
9	+5V	10	GND
11	N/A	12	SDA
13	HSYNC	14	VSYNC
15	SCL	16	N/A

CN11：LPC pin header CN112：Reset pin header



Pin	Definitions	Pin	Definitions
1	+3.3V	2	AD 0
3	AD 1	4	AD 2
5	AD 3	6	Frame#
7	PCIRST#	8	+5V
9	CLOCK	10	N/A
11	Ground	12	Ground

Pin	Define
1	Ground
2	Reset #

CN13：Case open pin header

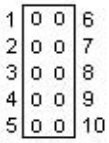
Pin	Definitions
1	Ground

2	Case open#

CN14：GPI pin header CN15：COM2 box header

Pin	Define
1	GPI0
2	GPI1
3	GPI2
4	GPI3
5	GND

CN15: COM2 Box Header

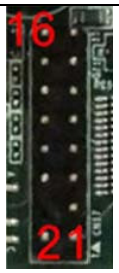


Pin	Definition	Pin	Definition
1	DCD#	6	DSR#
2	RXD#	7	RTS#
3	TXD#	8	CTS#
4	DTR#	9	RRI#2
5	Ground	10	N/A

CN16：Keypad pin header CN17：LCM pin header

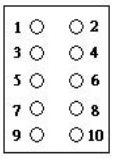
Pin	Definitions

1	ACK##
2 3	BUSY PE
4 5	SLCT Ground



Pin	Definitions	Pin	Definitions
1	+5V	2	Ground
3	AFD#	4	N/A
5	INIT#	6	SLIN#
7	PD1	8	PD0
9	PD3	10	PD2
11	PD5	12	PD4
13	PD7	14	PD6
15	BLN	16	BLP

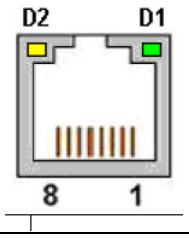
CN18：PS2 KB/MS pin header



Pin	Definitions	Pin	Define
1	KCLK	2	MCLK

3	KDAT	4	MDAT
5	N/A	6	N/A
7	PS2_GND	8	PS2_GND
9	PS2_VCC	10	PS2_VCC

CN19：Giga LAN RJ45 connector *2 port



Pin	Define
	MDI0+
	MDI0
	MDI1+
	MDI2+
	MDI2
	MDI1
	MDI3+
	MDI3

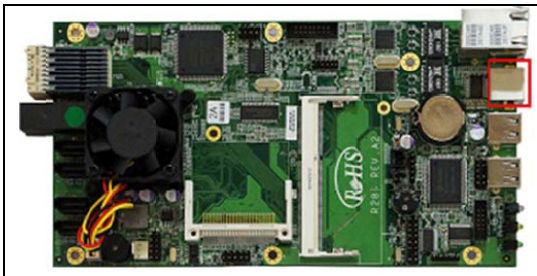
LED:

D2 : Link/Activity LED	
Link	Green
Activity	Blinking
D1 : Bi-Color Speed LED	
10 Mbps	Off
100 Mbps	Yellow
1000Mbps	Green

CN20-21：USB connector

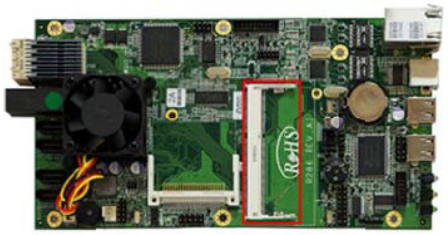
Pin	Definitions
1	+5V_USB
2	USBDT0-
3	USBDT0+
4	Ground

CN22：COM11 RJ45 connector



Pin	Definitions
1	CTS#_RTS#
2	DTR#
3	TXD#
4	GND
5	GND
6	RXD#
7	DSR#
8	CTS#_RTS#

DIMM1：IPMI connector



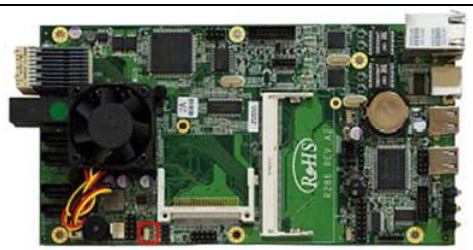
Pin	Definitions	Pin	Define
5	PCIE_SSB_RXN0	4	LAD0
7	PCIE_SSB_RXP0	6	LAD1
15	PCIE_SSB_TXN0	16	LAD2
17	PCIE_SSB_TXP0	18	LAD3
21	CLK_100M_VGA_DPP	22	CLK_33M_IPMI
23	CLK_100 M_VGA_DNN	24	LFRAME#
33	USB__TF_PP2	30	PCIE_RESET#
35	USB__TF_PN2	34	USB_TF_PP33
39	DACBO	36	USB_TF_PN33
45	DDCDAT	40	NCSI_RXD00
47	DDCCLK	42	NNSI_RXD11
51	DACGO	46	NCSI_CRS
57	DACRO	50	NCSI_TXD00
67	VSYNC	52	NCSI_TXD1
69	HSYNC	56	NCSI_TXEN
129	PCIE_SSB_RXN1	164	WAKE#
131	PCIE_SSB_RXP1	166	IRQ_SERIALL
141	PCIE_SSB_TXN1	174	PCH_GP6_PUU
1433	PCIE_SSB_TXP1	176	PCH_GP7_PUU
147	PCIE_SSB_RXN2	180	PANSWIN#
149	PCIE_SSB_RXP2	182	-RST_SW
157	PCIE_SSB_TXN2	192	PCC_GP1_PUU
159	PCIE_SSB_TXP2	194	PCH_PWROKK
163	PCIE_SSB_RXN3		
165	PCIE_SSB_RXP3		
175	PCIE_SSB_TXN3		
177	PCIE_SSB_TXP3		
181	SATAH DR_TXP5		

1833	SATAHDR_TXN5		

1911	SATAHDR_RXN5		
1933	SATAHDR_RXP5		

[V3P3_AUX]：PIN.75,76,81,82,87,88,93,94,99,100
[V5P0_AUX]：PIN.105,106,111,112,117,118,123,124
[GNND]PIN.2,3,,8,9,13,14,,19,20,25,26,31,32,37,38,43,44,48,49,54,55,60,61,65,66,71,72,127,128,133,134,138,139,
144,145,150,151,155,156,161,162,
167,168,172,173,178,179,184,185,189,190,195,196

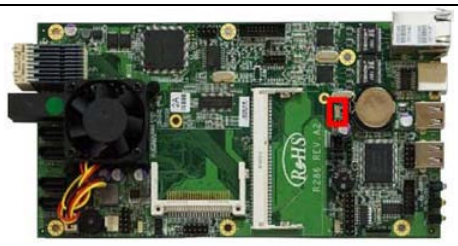
SW1: Clear CMOS



Pin	Setting
B-A	Normal(Default)
B-C	Clear CMOS

SW2: Watchdog function on SW3: ATX switch function

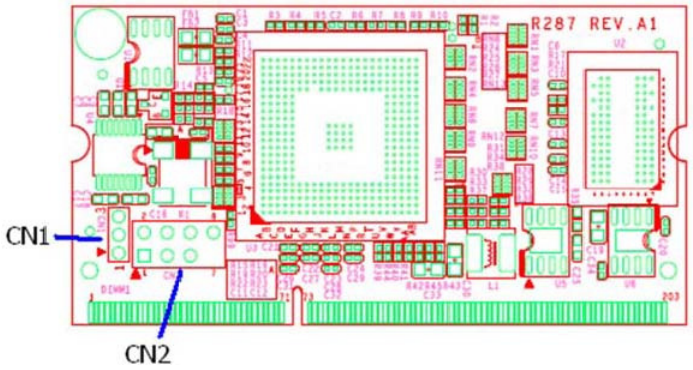
Pin	Setting
B-A	LAN Bypass
B-C	Reset (Default)



Pin	Setting

B-A	Auto power on
B-C	By power button

2.44 R287 Connector/Jumper Locations and Definitions



Connectors/Jumper Locations & Definitions

Connector	Define
CN1	SPI pin header for Debug
CN2	COM3 pin header

CN11：SPI pin header

Connector	Definition
1	GND
2	TXD#
3	RXD#

CN2: COM3 pin header for Debug

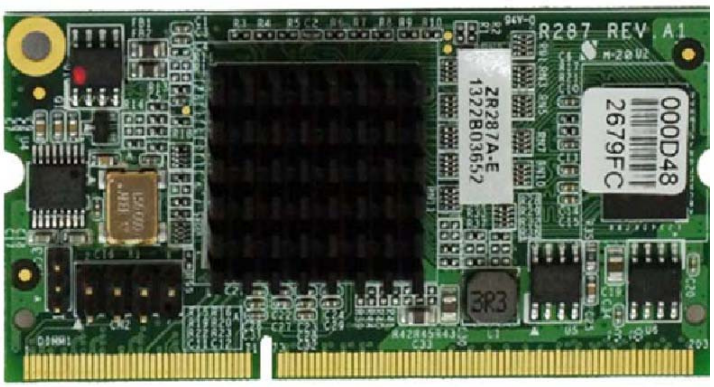
PIN	Define	Pin	Define
1	3.3	2	Ground
3	CS#	4	SCLK
5	MISO	6	MOSI

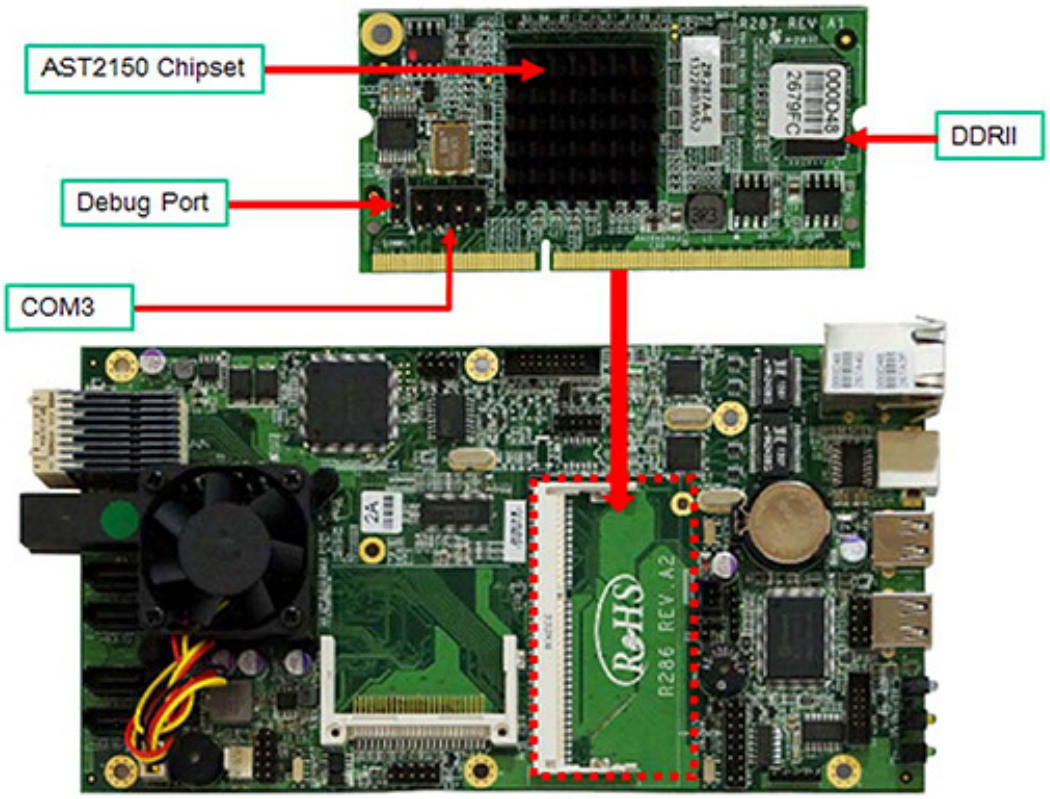
7	N/A	8	IO

Chapter 3. Optional LAN Module & Add-on Card Settings

The PL-80150 can offer various GbE and 10GbE module combinations to match various applications and market demands.

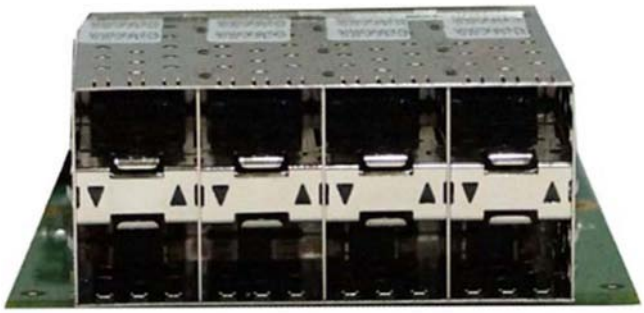
3.1 R287: IPMI card with VGA support

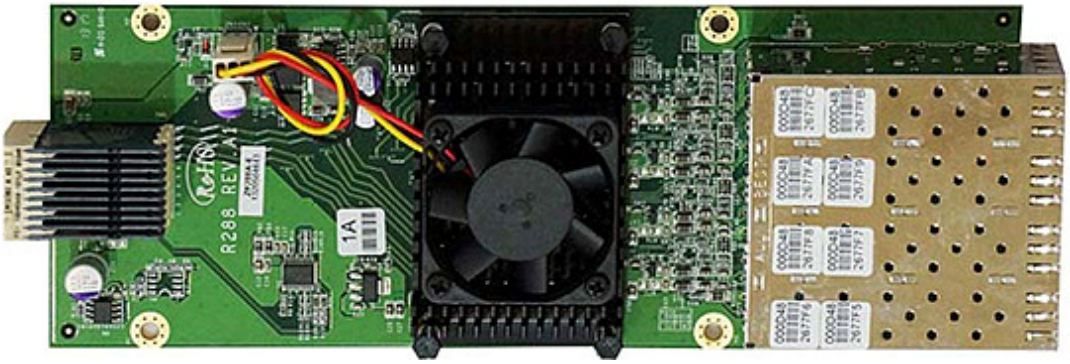




3.22 R288: Ethernet module with eight GbE SFP

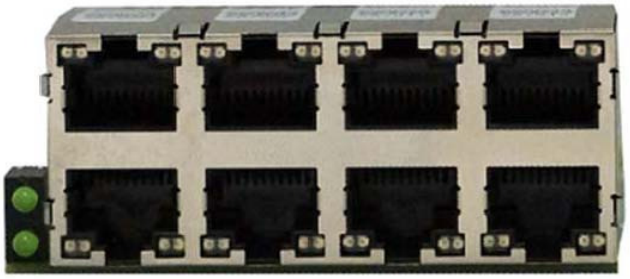
R2888A is an eight GbE fiber module. The FCI Airmax connector must be connected with CN3 (or CN4, CN7, CN8, CN5, CN6, CN9, CN10) proprietary connector of the middle plane（R285A).

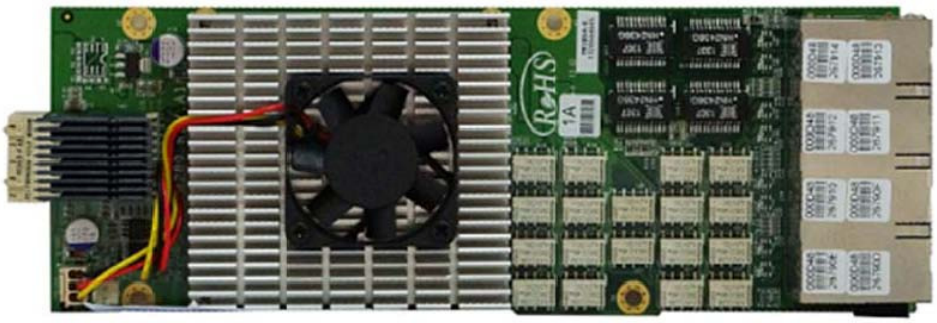




3.3 R289: Ethernet module with eight GbE Copper

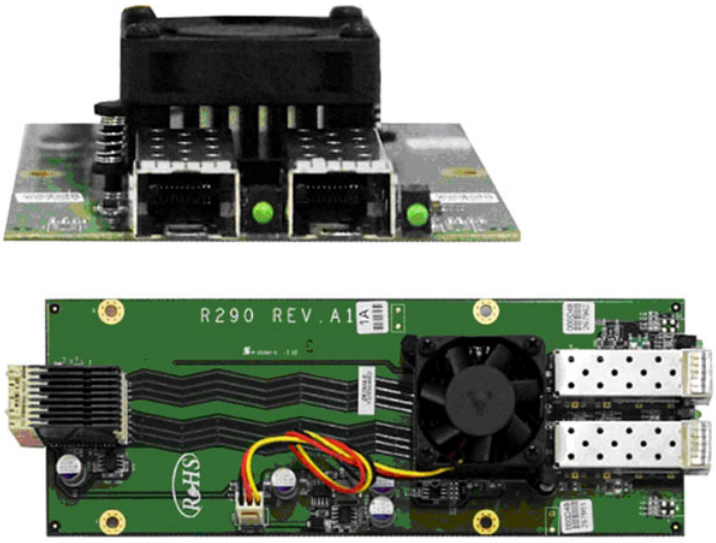
R2889A is an eight GbE Copper module. The FCI Airmax connector must be connected with CN3 (or CN4, CN7, CN8, CN5, CN6, CN9, CN10) proprietary connector of the middle plane（R285A）.





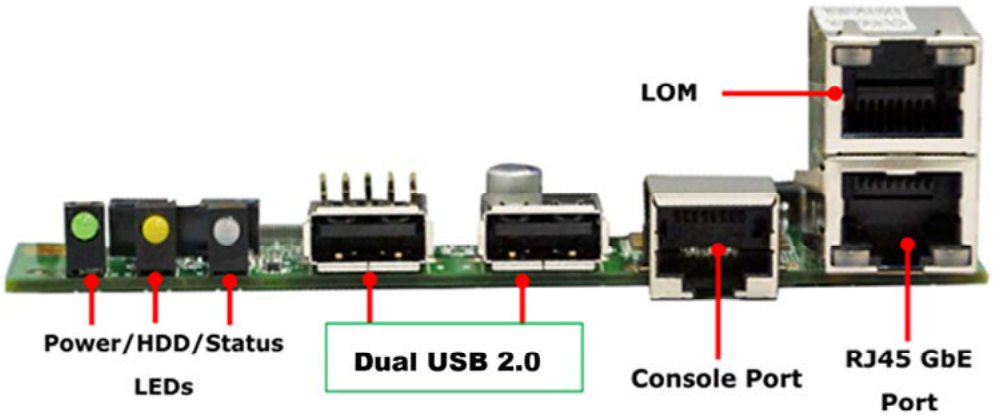
3.4 R290: Ethernet module with two 10GbE SFP+

R290A is a two 10GbE SFFP+ module. The FCI Airmax must be connected with CN3 (or CN4, CN7, CN8, CN5, CN6, CN9, CN10) proprietary connector of the middle plane（R285A.



3.55 R286A: Front I/O module

R286A is a front I/O module with Power/HDD/Status LEDs, Dual USB 2.0 port, one RJ45 console port (COM1, RS-232), two GbE port and designed reserved one VGA pin header for Option. The FCI Airmax must be connected with CN111 proprietary connector of the middle plane（R285A).



Chapter 4. BIOS Setup

The ROM chip of your R286A board is configured with a customized Basic Input/Output System (BIOS) from AMI BIOS. The BIOS is a set of permanently recorded program routines that give the system its fundamental operational characteristics. It also tests the computer and determines how the computer reacts to instructions that are part of programs.

The BIOS is made up of code and programs that provide t he device-level control for the major I/O devices in the system. It contains a set of routines (called POST, for Power-On Self Test) that check out the system when you turn it on. The BIOS also includes BIOS setup program, so no disk-based setup program is required CMOS RAM stores information for:

- ☐ Date and time
- ☐ Memory capacity of the appliance
- ☐ Type of display adapter installed
- ☐ Number and type of disk drives

The CMOS memory is maintained by battery installed on the MB-80150 board. By using the battery, all memory in CMOS can be retained when the system power switch is turned off. The system BIOS also supports easy reload of the CMOS data when you replace the battery or battery loses power.

4.1 Quick Setup

In most cases, you can quickly configure the system by choosing the following main menu options:

1 Choose "Exit" ➔ "Load Optimal Defaults" from the main menu. This loads the setup default values from the BIOS Features Setup and Chipset Features Setup screens.
2 Choose "Main" & "Advanced" from the main menu. This option lets you configure the date and time, hard disk type, floppy disk drive type, primary display and more.
3 In the main menu, press F4 ("Save and Exit") to save your changes and reboot the system.

4.2 Entering the BIOS Setup Utility

Use the BIOS setup program to modify the system parameters to reflect the options installed in your system and to customize your system. For example, you should run the Setup program after you:

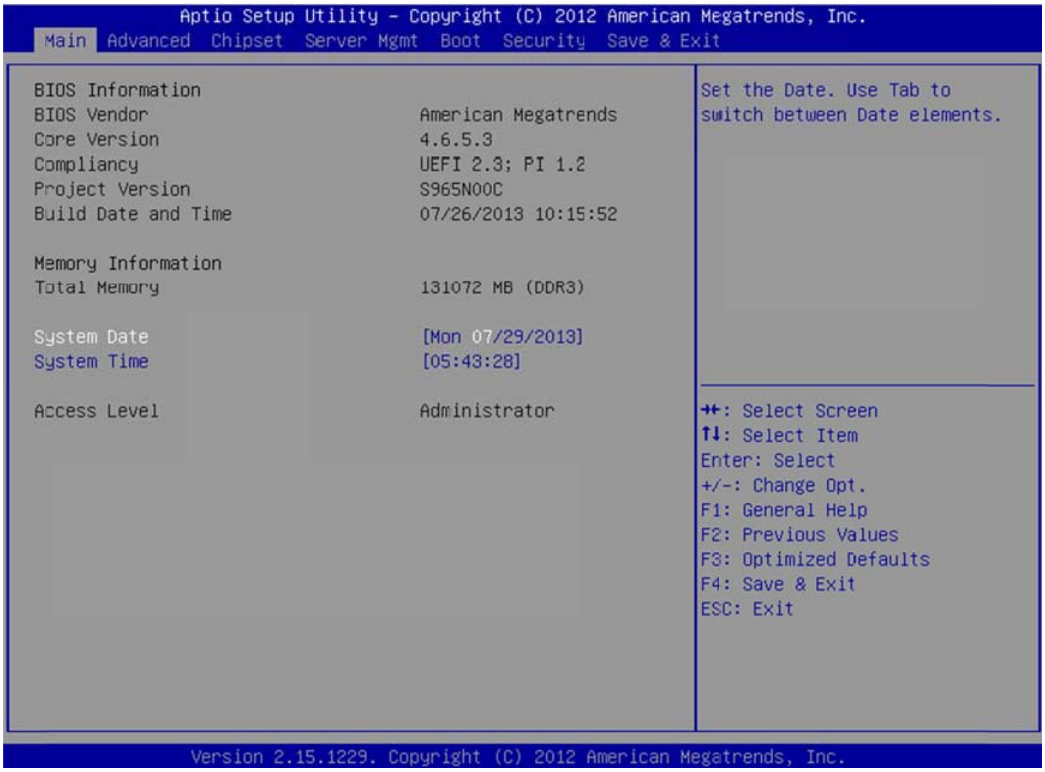
- ☐ Received an error code at startup
- ☐ Install another disk drive
- ☐ Use your system after not having used it for a long time
- ☐ Find the original setup missing
- ☐ Replace the battery
- ☐ Change to a different type of CPU
- ☐ Run the AMI Flash program to update the system BIOS

Run the BIOS setup program after you turn on the system. On-screen instructions explain how to use the program.

Enter the BIOS setup program's main menu as follows:

1. Turn on or reboot the system. After the BIOS performs a series of diagnostic checks, the following message appears: "Press DEL to enter SETUP""

2. Press the <DEL> key to enter BIOS setup utility. The main menu appears:



3. Choose a setup option with the arrow keys and press <Enter>. See the following sections for a brief description off each setup option. **BIOS Information:** Displays the BIOS related information. **Memory Information:** Displays the total memory size.

System Language: Change the language display in BIOS setup utility.

System Date [Day mm/dd/yyyy]: This item allows you to set the system date.

System Time: [hour:min :sec]:

This item allows you to set the system time.

In the main menu, press F4 (“Save and Exit”) to save your changes and reboot the

system. Press F3 (“Optimized Defaults”) to load the Optimal default configuration values of the menu. Pressing <ESCC> anywhere in the program returns you too the main menu.

4.3 Menu Options

The main menu options of the BIOS setup program are described in the following and the following sections of this chapter.

Main: For changing the basic system configurations.

Advanced: For changing the advanced system settings.

Chipset: For customize the Intel chipset function

Server Mgmt: For changing the Server Mgmt settings

Boot: For changing the system boot configurations.

Security: For setting User and Supervisor Passwords.

Save & Exit: For selecting the exit options and loading default settings.

4.4 Advanced Menu

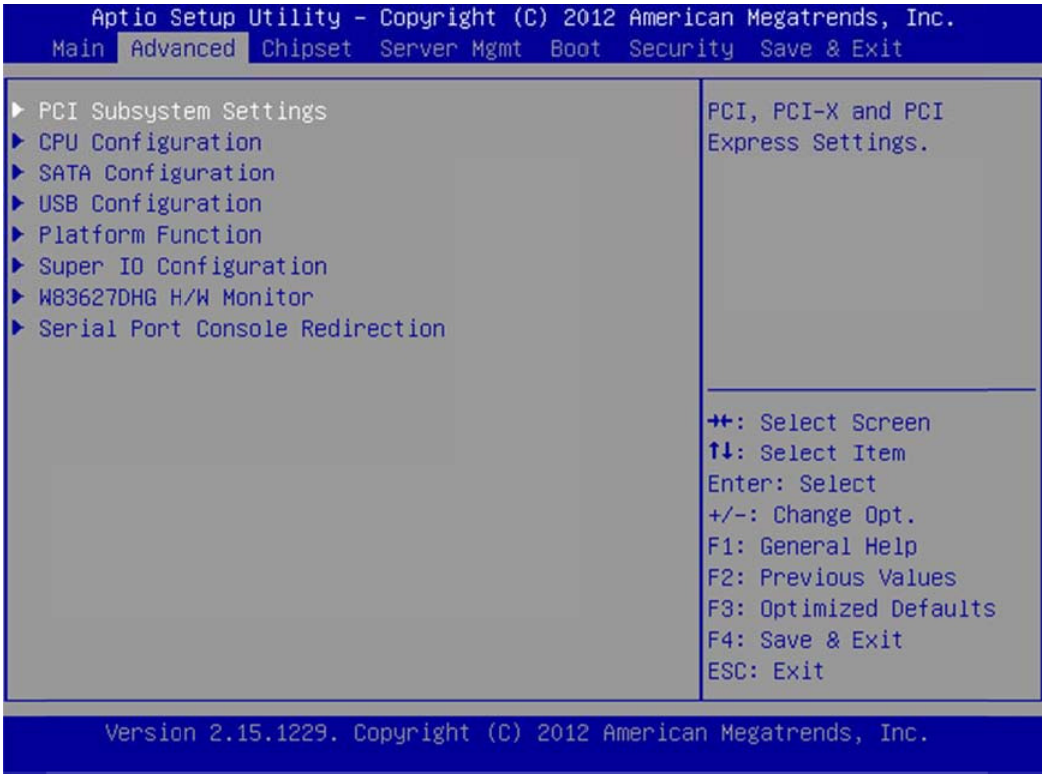
The Advanced menu items allow you to change the settings for the CPU and other system devices.

Use the Advanced Setup option as follows:

Choose "Advanced" from the main menu. The following screen appears:

⇩

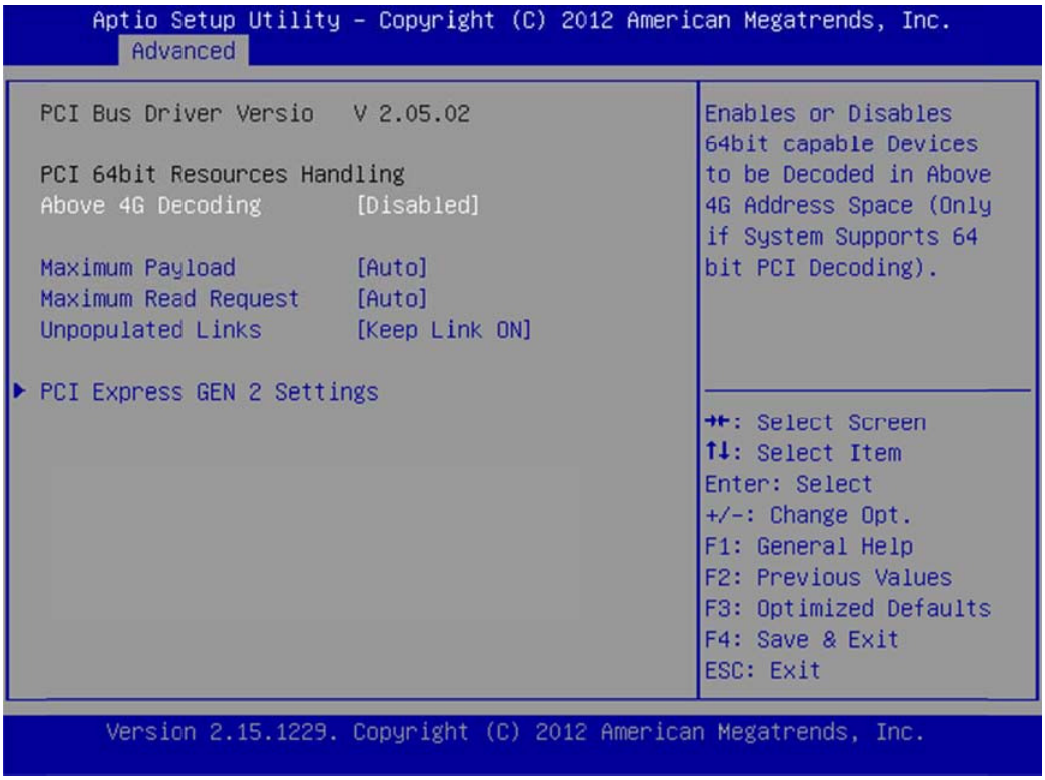
1.



1 Use the arrow keys to move between fields. Modify the selected field using the PgUP/PgDN/+/- keys. Some fields let you enter numeric values directly.

2 After you have finished with the Advanced Setup, press the <←> or <→> key to switch to other setup menu or press <F4> key to save setting.

4. 4.1 PCI Subsystem Settings



Above 4G Decoding

Enables or Disables 64bit capable Devices too be decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).

Maximum Payload

Set Maximum Payload off PCI Express Device or allow S system BIOS to select the value.

Maximum Read Request

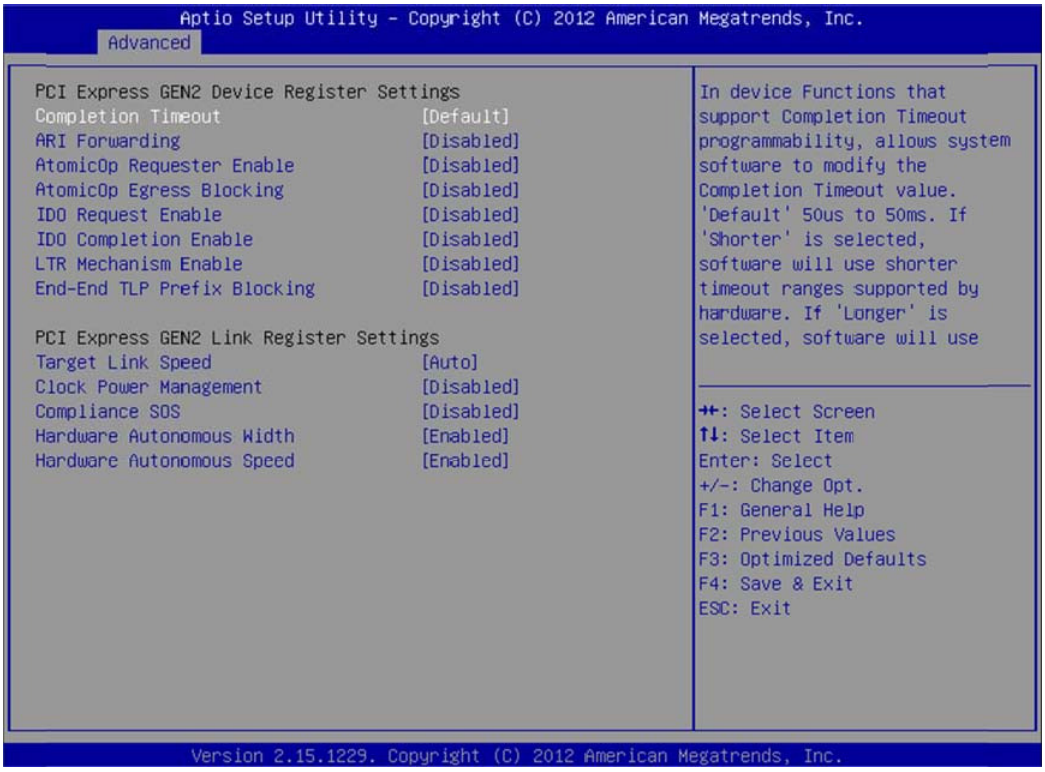
Set Maximum Read Request Size o f PCI Express Device or allow System BIOOS to select the value.

Unpopulated Links

In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Lin k'.

4.4.2 PCI Express GEN 2 Settings

PCI, PCI-X and PCI Express Settings.



4.4.2.1 PCI Express GEN2 Device Register Settings

Completion Timeout

In device Functions that support Completion Timeout programmability, allows system software to modify the Completion Timeout value. 'Default' 50us to 50mms. If 'Shorter' is selected, software will use shorter timeout ranges supported by hardware. If 'Longer' is selected, software will use longer timeout ranges.

ARI Forwarding

If supported by hardware and set to 'Enabled', the Downstream Port disable its traditional Device Number field being 0 enforcement when turning a Type1 Configuration Request into a Type0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. Default value: Disabled

AtomicOp Requester Enable

If supported by hardware and set to 'Enabled', this function initiates AtomicOp Requests only if Bus Master Enable bit is in the Command Register Set.

AtomicOp Egress Blocking

If supported by hardware and set to 'Enabled', outbound AtomicOp Requests via Egress Ports will be blocked.

IDO Request Enable

If supported by hardware and set too 'Enabled', this permits setting the number of ID-Based Ordering (IDO)) bit (Attribute[2]) requests to be initiated.

IDO Completion Enable

If supported by hardware and set too 'Enabled', this permits setting the number of ID-Based Ordering (IDO)) bit (Attribute[2]) requests to be initiated.

LTRR Mechanism Enable

If supported by hardware and set too 'Enabled', this enables the Latency Tolerance Reporting (LTRR) Mechanism.

End-End TLP Prefix Blocking

If supported by hardware and set too 'Enabled', this function will block forwarding of TLPs containing End-End TLP Prefixes.

4.4.2.2 PCI Express GEN2 Link Register Settings

Target Link Speed

If supported by hardware and set too 'Force to 22.5 GT/s' for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used.

Clock Power Management

If supported by hardware and sett to 'Enabled', the device is permitted to use CLKKREQ# signal for power management of Link clock in accordance to protocol defined in appropriate form factor specification.

Compliance SOS

If supported by hardware and set to 'Enabled', this will force LTSS SM to send SKP Ordered Sets between sequences when sending Compliance Pattern or Modified

Compliance Pattern.

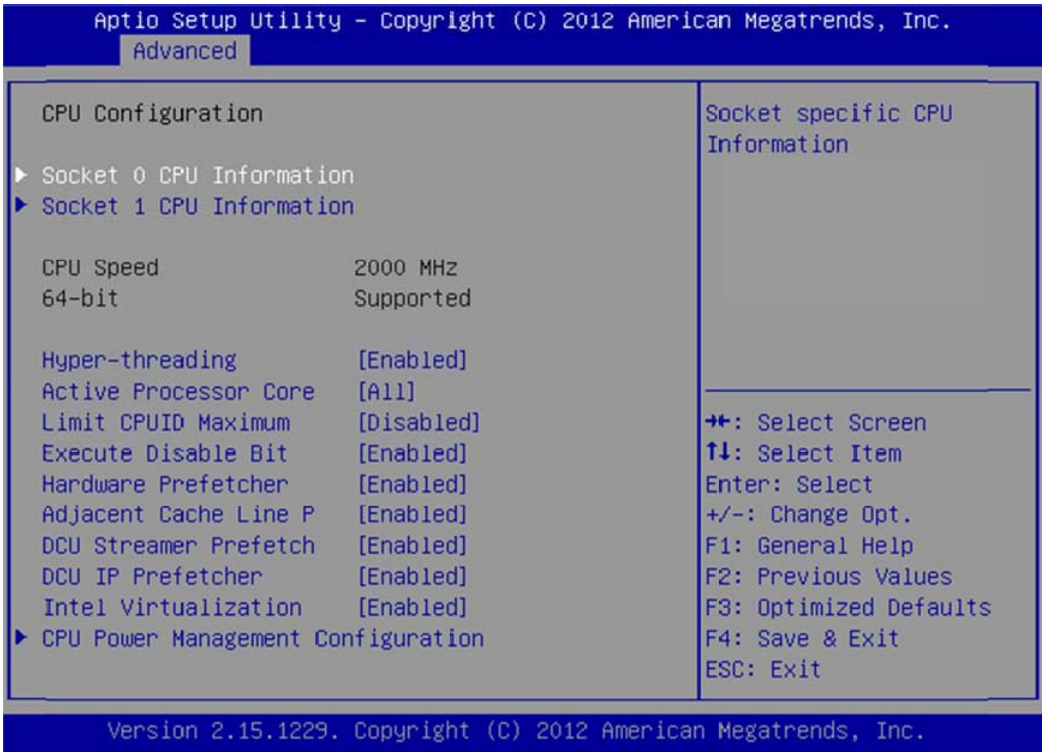
Hardware Autonomous Width

If supported by hardware and set to 'Disabled', this will disable the hardware's ability to change link width except width size reduction for the purposes of correcting unstable link operation.

Hardware Autonomous Speed

If supported by hardware and set to 'Disabled', this will disable the hardware's ability to change link speed except speed rate reduction for the purpose of correcting unstable link operation.

4.4.3.1 CPU Configuration



HyperThreading

Enabled for Windows XP and Linux (OS optimized for HyperThreading Technology) and Disabled for other OS (OS not optimized for HyperThreading Technology). When Disabled only, one thread per enabled core is enabled.

Active Processor Cores

Number of cores to enable in each processor package.

Limit CPUID Maximum

Disabled for Windows XP...

Execute Disable Bit

XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SPP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3.)

Hardware Prefacer

Enable the Mid Level Cache (L2) streamer prefacer.

Adjacent Cache Line Prefect

Enable the Mid Level Cache (L2) prefetching of adjacent cache lines.

DCU Streamer Prefetcher

Enable prefetch of next LL1 Data line based upon multiple loads in same cache line.

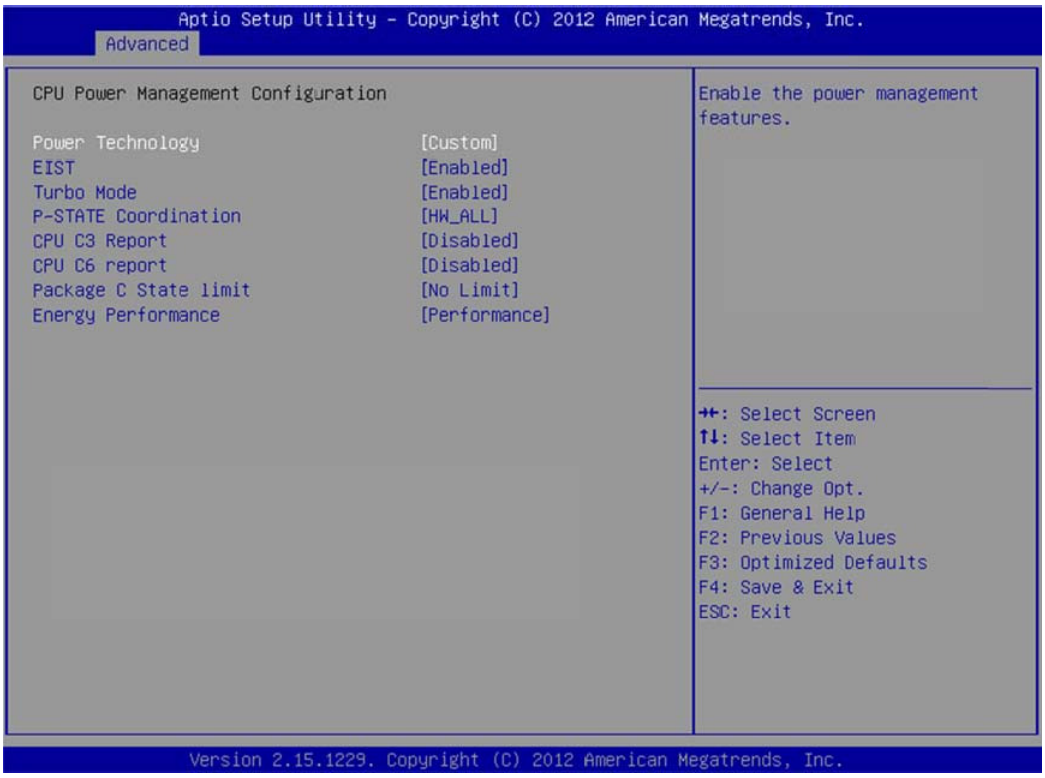
DCU IP Prefetcher

Enable prefetch of next LL1 line based upon sequential load history.

Intel® Virtualization Technology

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology**.**

4.4.3.2 CPU Power Management Configuration



Power Technology

Enable the power management features.

EISST Enable/Disable Intel SpeedStep**.**

Turbo Mode

Enable/Disable Intel Turbo Mode.

P-STATE Coordination

Change P-STATE Coordination type.

CPU C3 Report

Enable/Disable CPU C3 (AACPI C2) report to OS.

CPU C6 report

Enable/Disable CPU C6 (AACPI C3) report to OS.

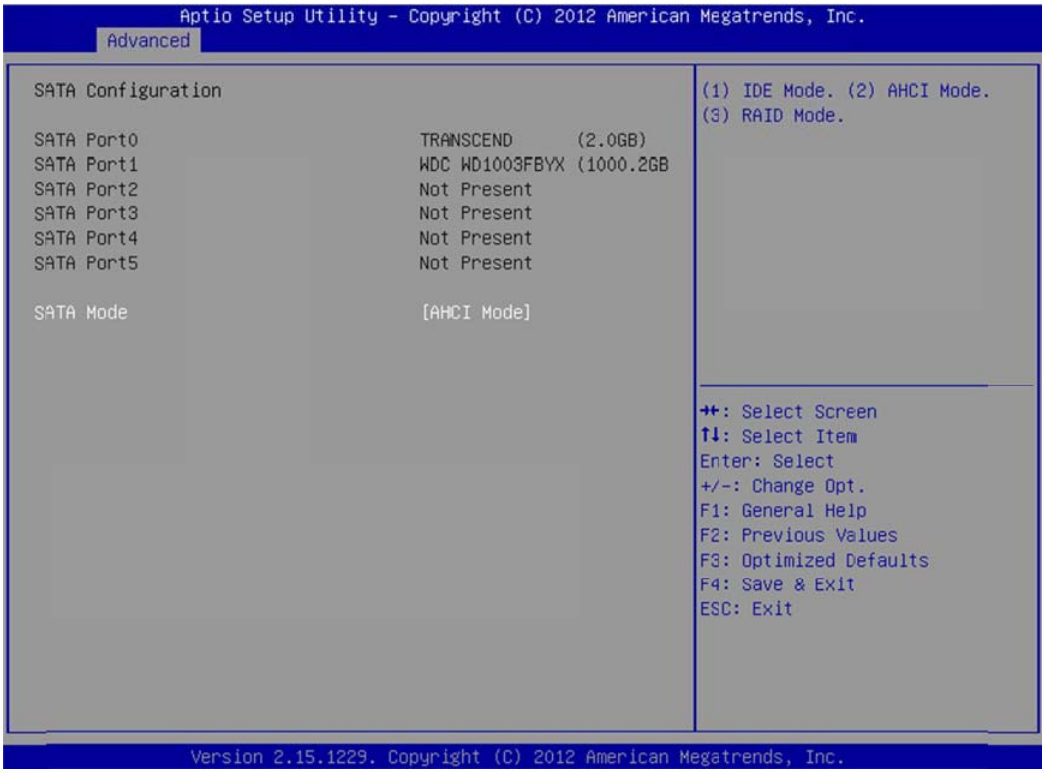
Package C State limit

Package C State limit

Energy Performance

Optimize between performance and power saving. Windows 2008 and later OSes overrides this value according to its power plan.

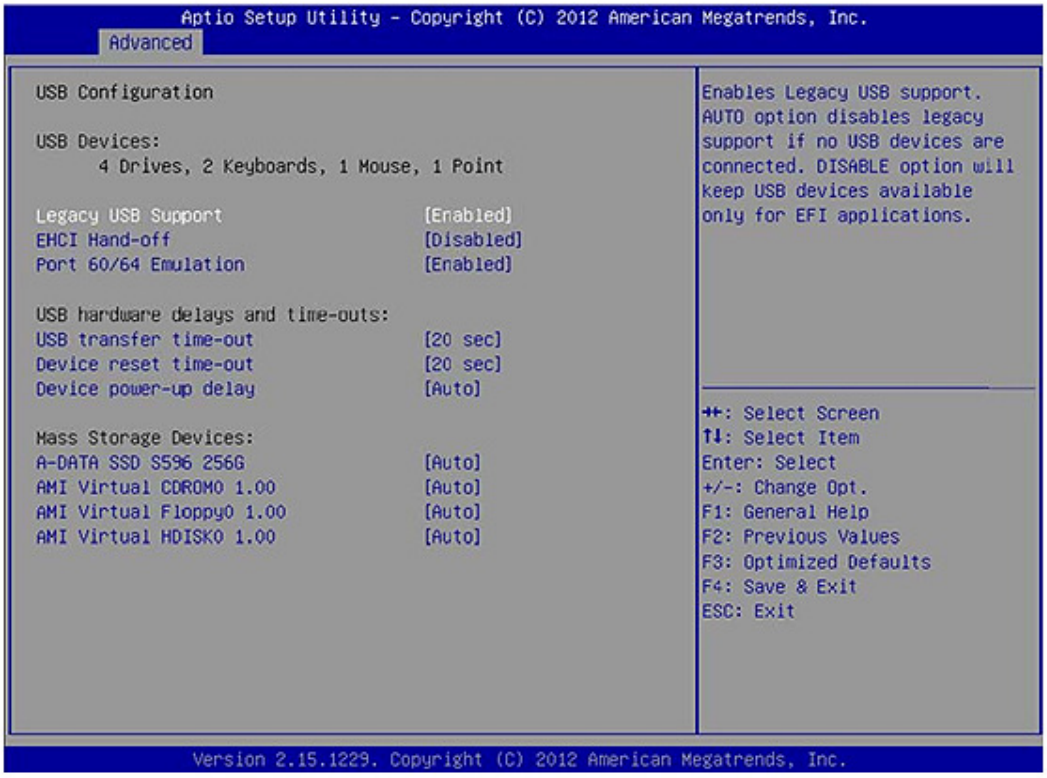
4.4.4 SATA Configuration



SATA Mode

(1) IDE Mode. (2) AHCI Mode. (3) RAID Mode.

SATA Port0 ~ 5 This information is auto-detected by BIOS and is not user configurable. It will show "Not Present" if no IDE device is installed in the system.



Legacy USB Support

Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

XHCCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XXHCI ownership change should be claimed by XHCI driver.

Port 60/64 Emulation

Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.

USB transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

Device reset time-out

USB mass storage device Start Unit command time-out.

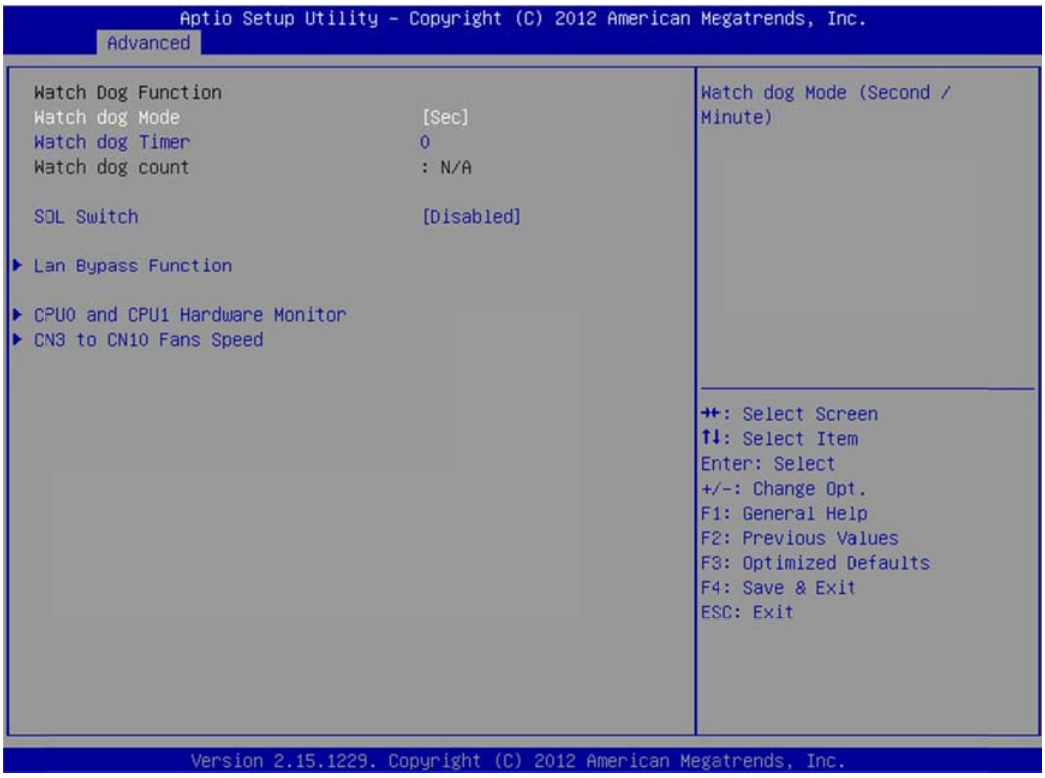
Device power-up delay

Maximum time the device will take before it properly reports itself to the Host

Controller. 'Auto' uses default value: for a Root port it is 1100 ms, for a Hub port the delay is taken from Hub descriptor.

4.4.5 Platform Function

4.4.5.1 Watch dog function



Watchdog Mode

Watchdog Mode（Sec/Min）.

Watchdog Timer

Watchdog Mode（Sec/Min）.

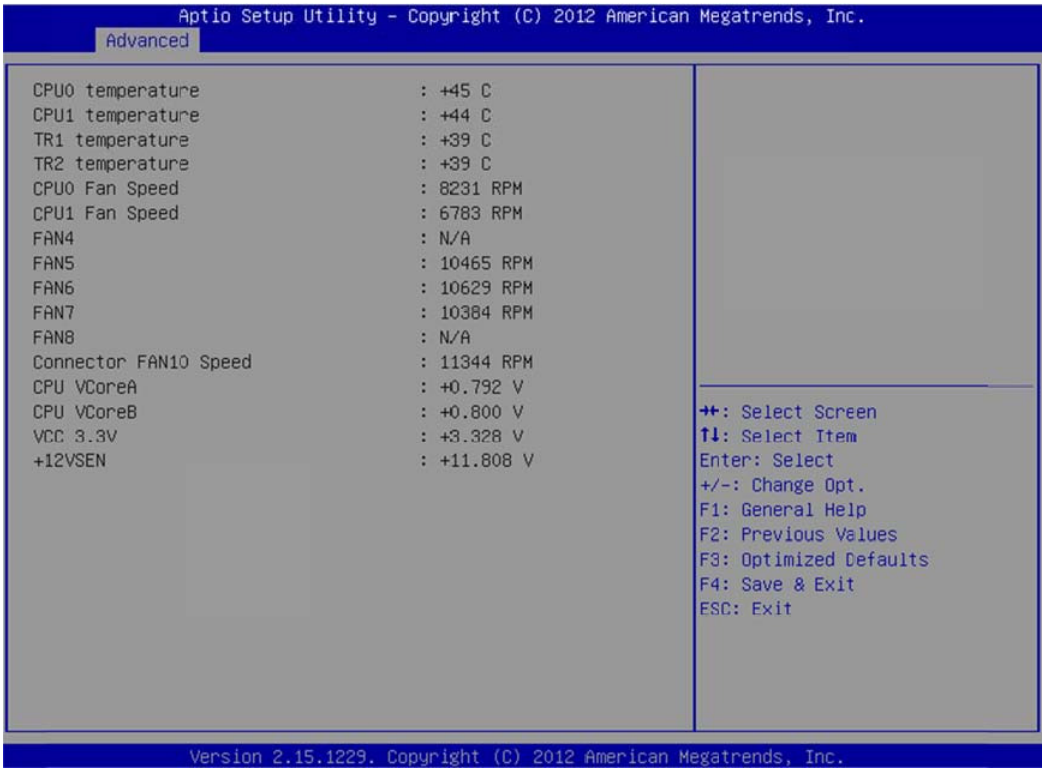
SOL Switch

Switch console for COM2 or SOL.

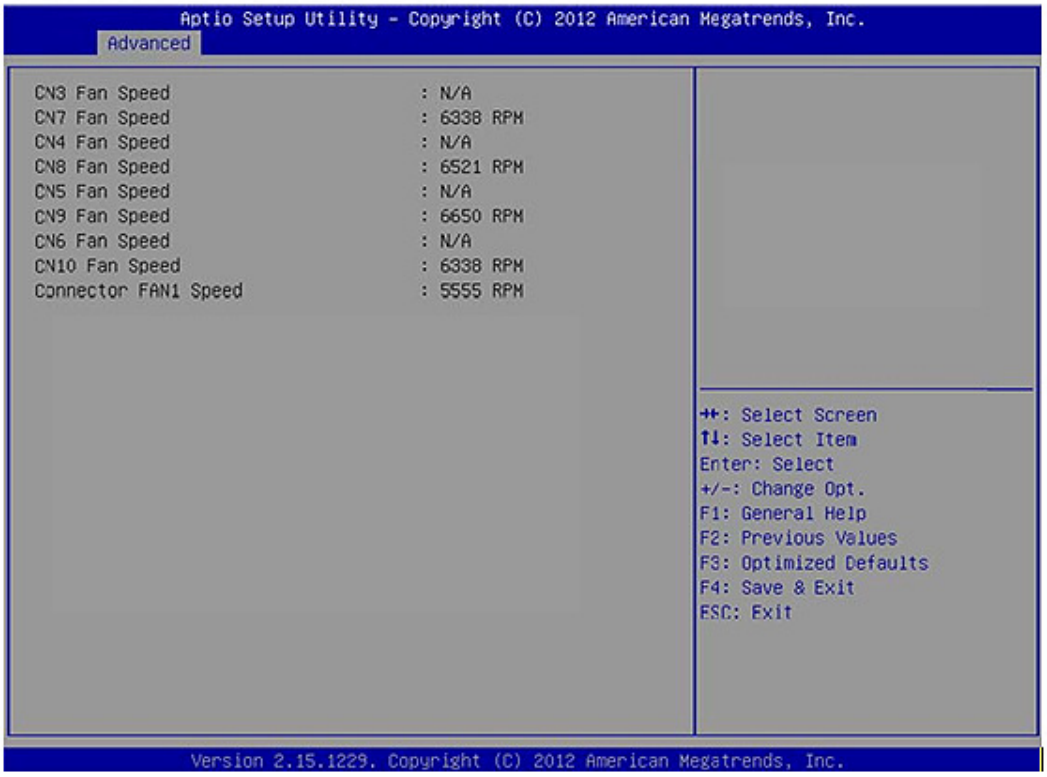
W83793 Mode

If Switch this function, need save and reboot.

CPU0 and CPU1 Hardware Monitor

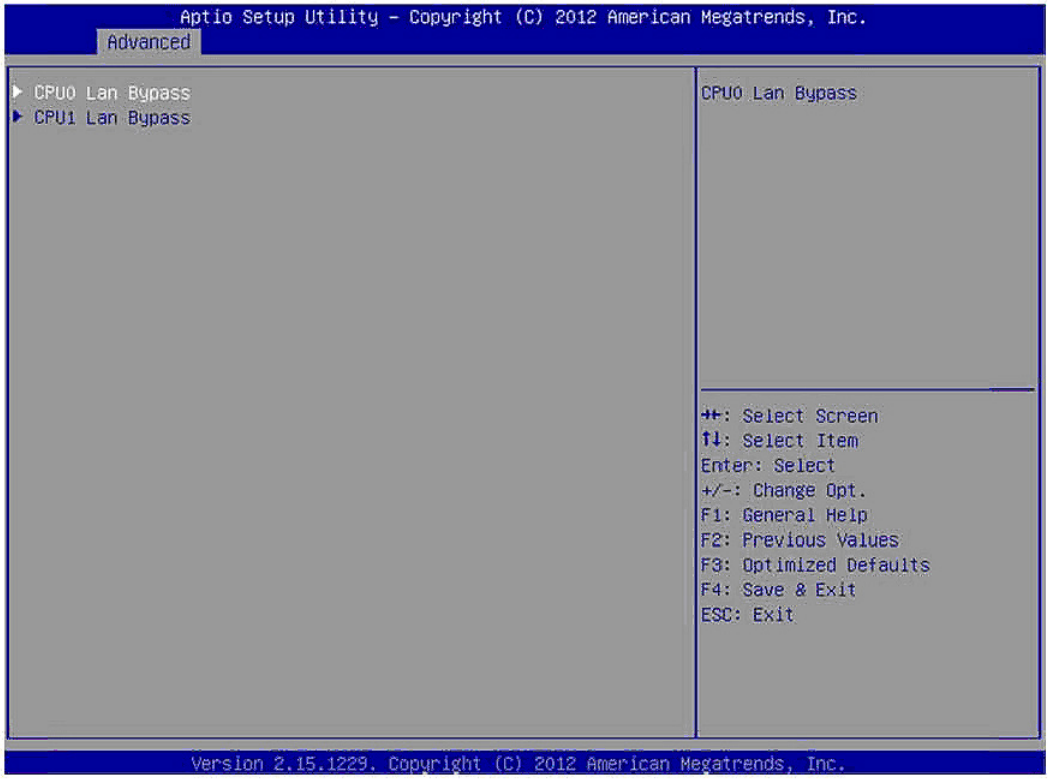


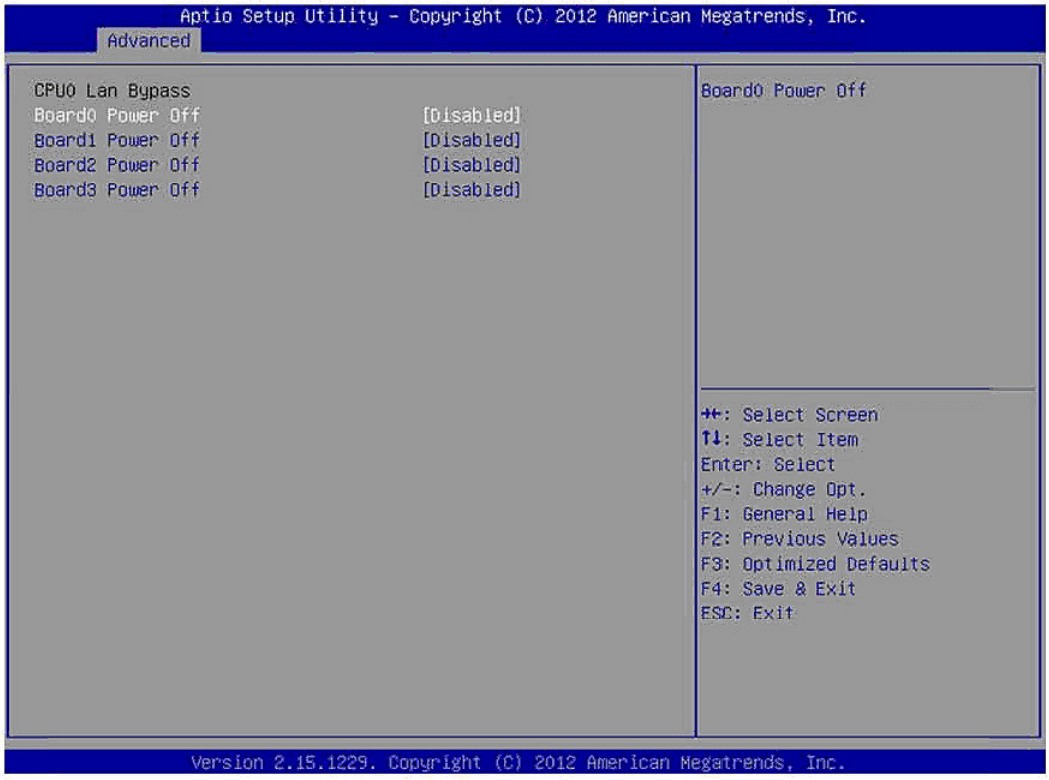
CN33 to CN10 Fans Speed



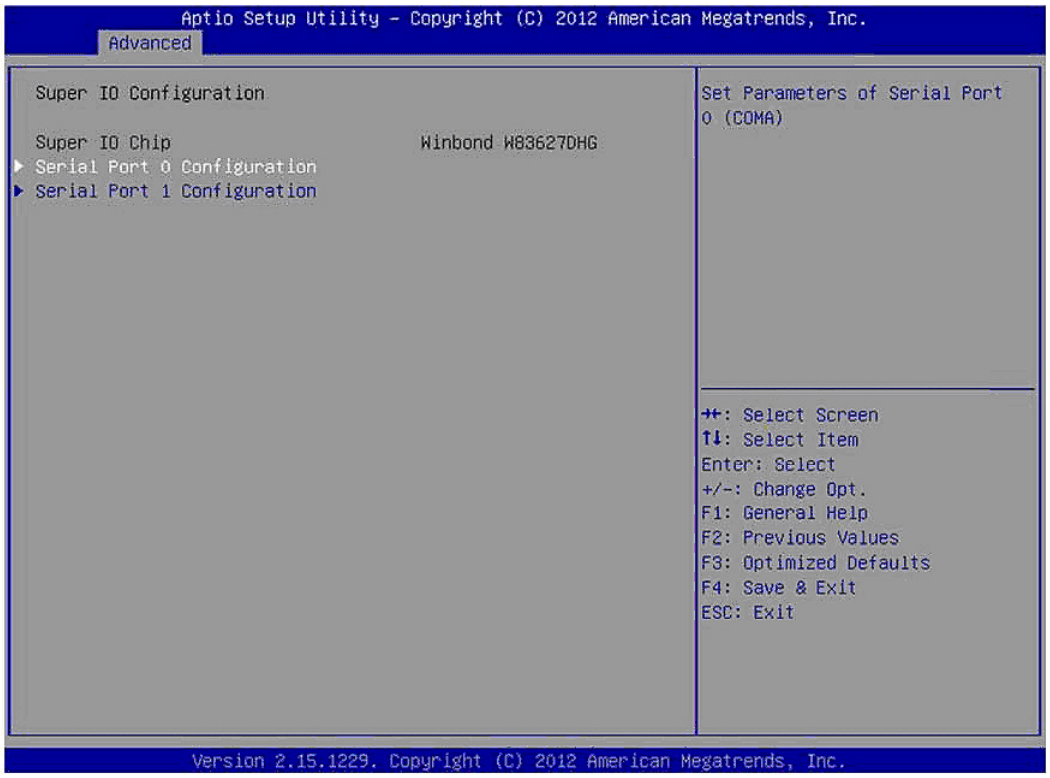
4.4.5.2 LAN Bypass function

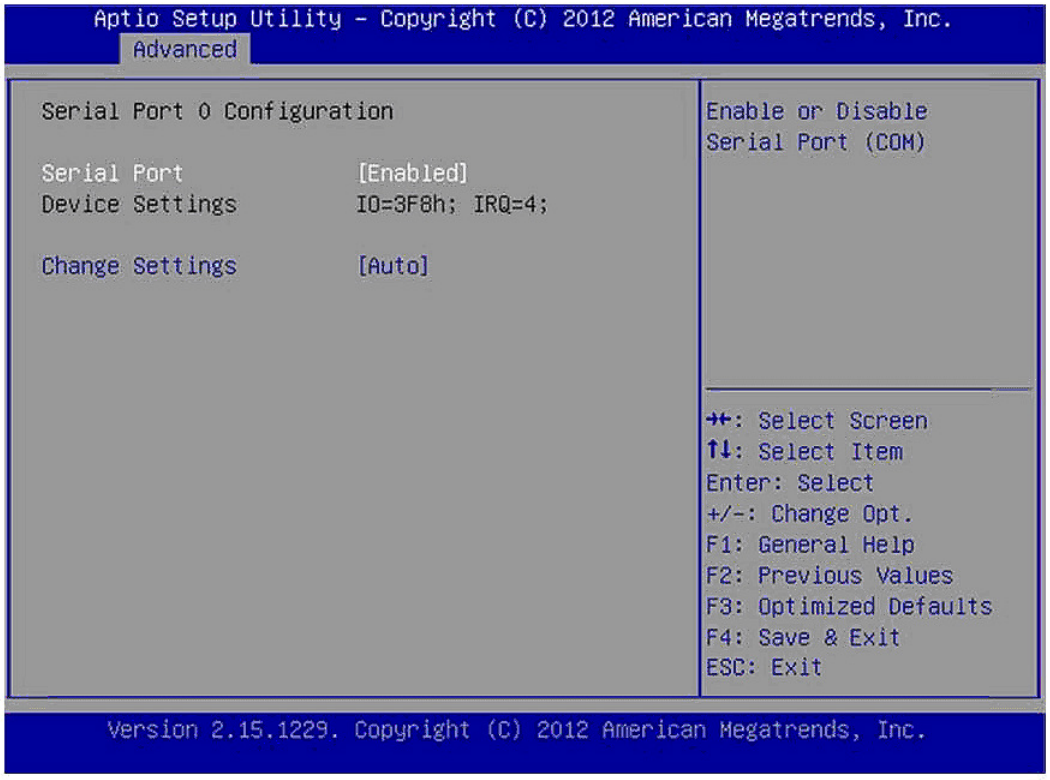
This item allows you to enable/disable the LAN Bypass 1 or 2 when system power off on CPU0 or CPU1

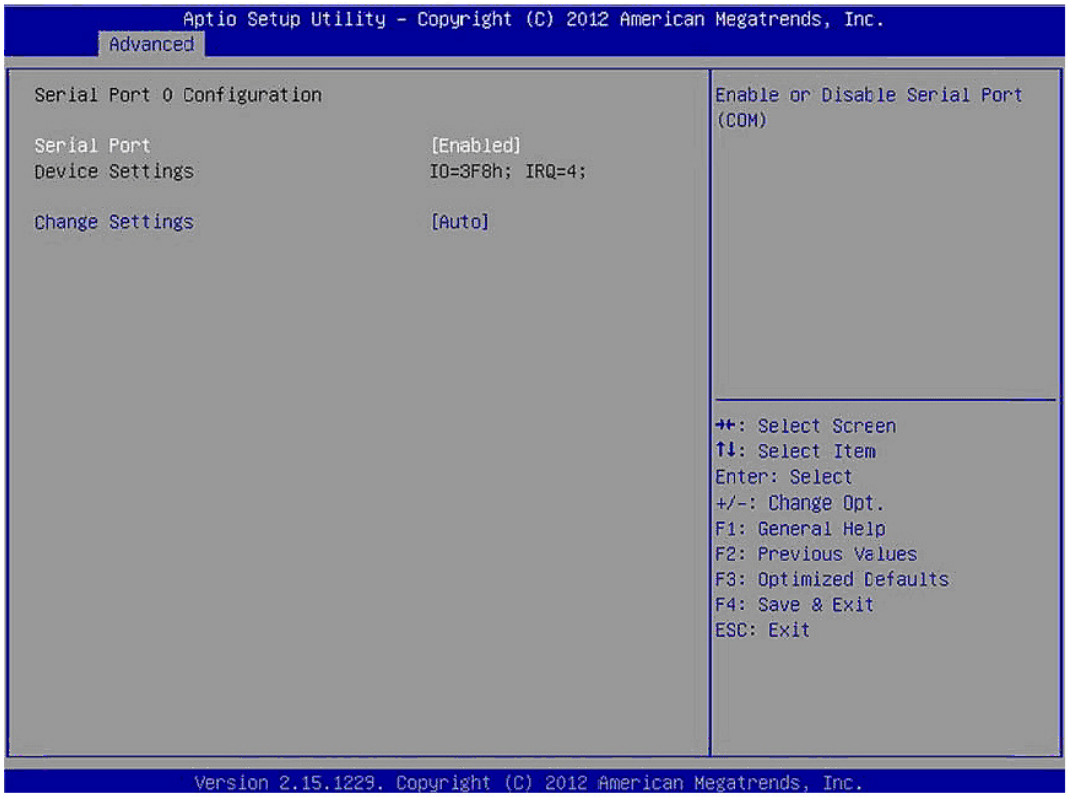

Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Advanced
CPU0 Lan Bypass
CPU1 Lan Bypass
CPU0 Lan Bypass
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1229. Copyright (C) 2012 American Megatrends, Inc.


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Advanced
CPU0 Lan Bypass
Board0 Power Off [Disabled]
Board1 Power Off [Disabled]
Board2 Power Off [Disabled]
Board3 Power Off [Disabled]
Board0 Power Off
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1229. Copyright (C) 2012 American Megatrends, Inc.

4.4.6 Super IO Configuration







4.4.6.1 Serial Port 0/1 Configuration

Serial Port

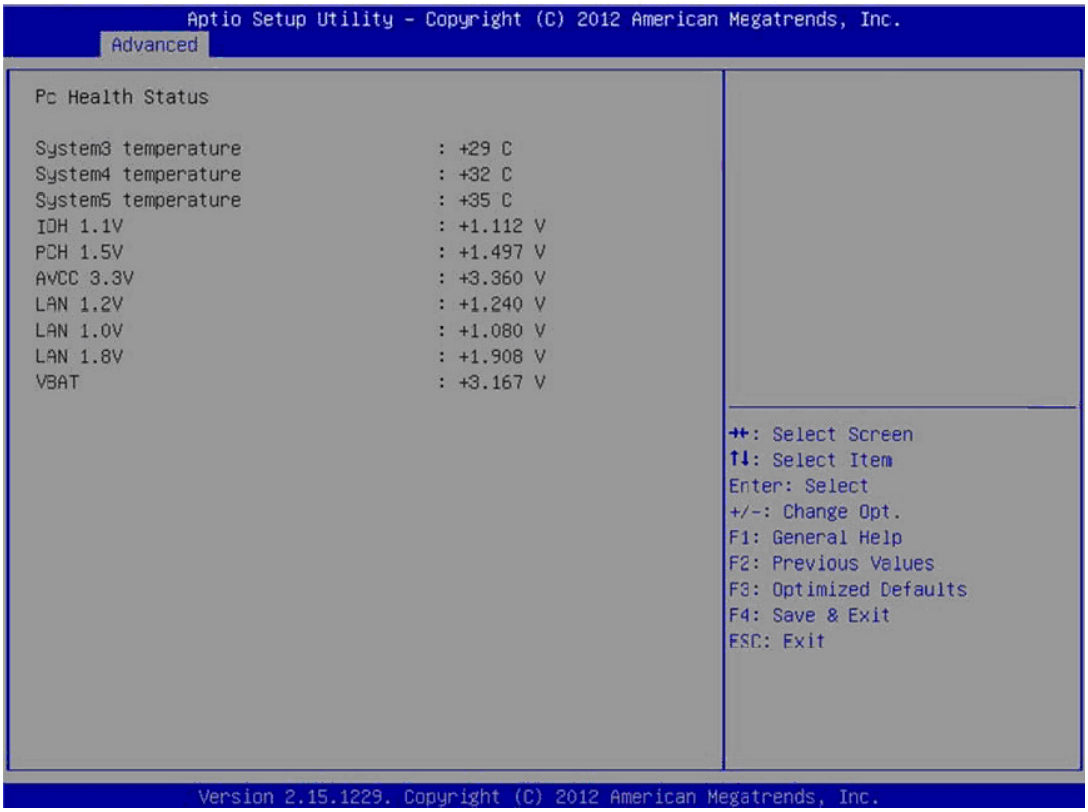
Enable or Disable Serial Port (COM)

Change Settings

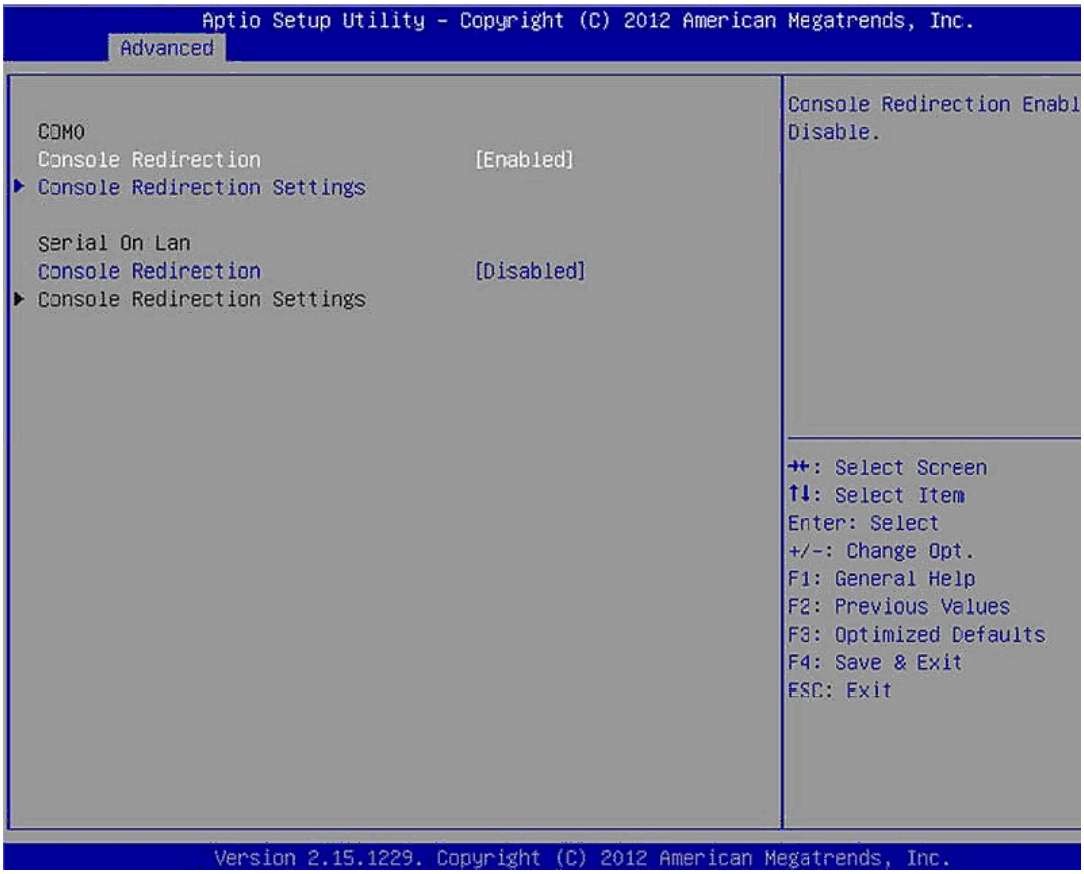
Select an optimal setting for Super IO device.

PC Health Status

This screen shows the mother board voltage and system temperature.

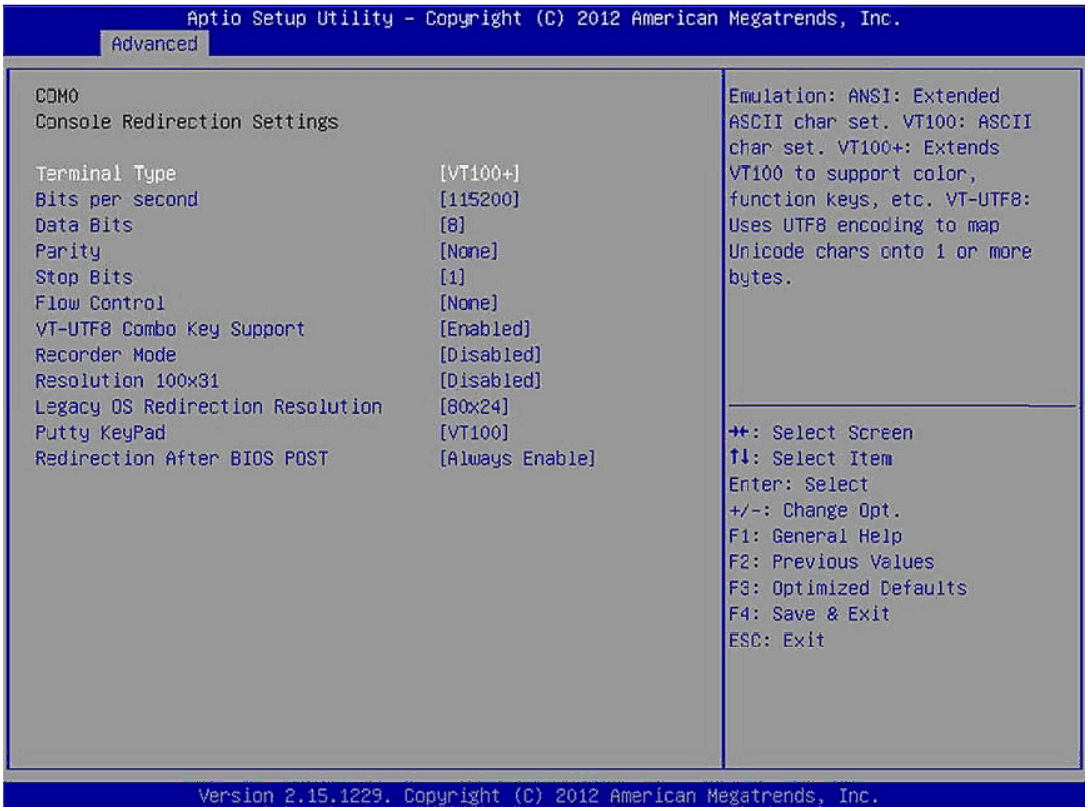


4.4.6.2 Console Redirection Settings (COM0)



Console Redirection

Console Redirection Enable or Disable.



Terminal Type

Emulation: ANSI: Extended ASCII I char set. VT100: ASCII char set. VT1000+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.

Bits per second

Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

Data Bits

Data Bits.

Parity

A parity bit can be sent with the data bits to detect some transmission on errors. Even: parity bit is 0 if the number of 1's in the data bits are even. Odd: parity bit is 0 if number of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always

0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.

Stop Bits

Stop bits indicate the end of a serial data packet. (AA start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 11 stop bit.

Flow Control

Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can bee sent to stoop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-star t the flow. Hardware flow control uses two wires too send start/stop signals.

VT--UTF8 Combo Key Support

Enable VT-UTFF8 Combination Key Support for ANSI/VT1000 terminals.

Recorder Mode

With this mode enabled only text w ill be sent. This is to capture Terminal data.

Resolution 100x31

Enables or disables extended terminal resolution.

Legacy OS Redirection Resolution

On Legacy OS, the Number of Rows and Columns supported redirection.

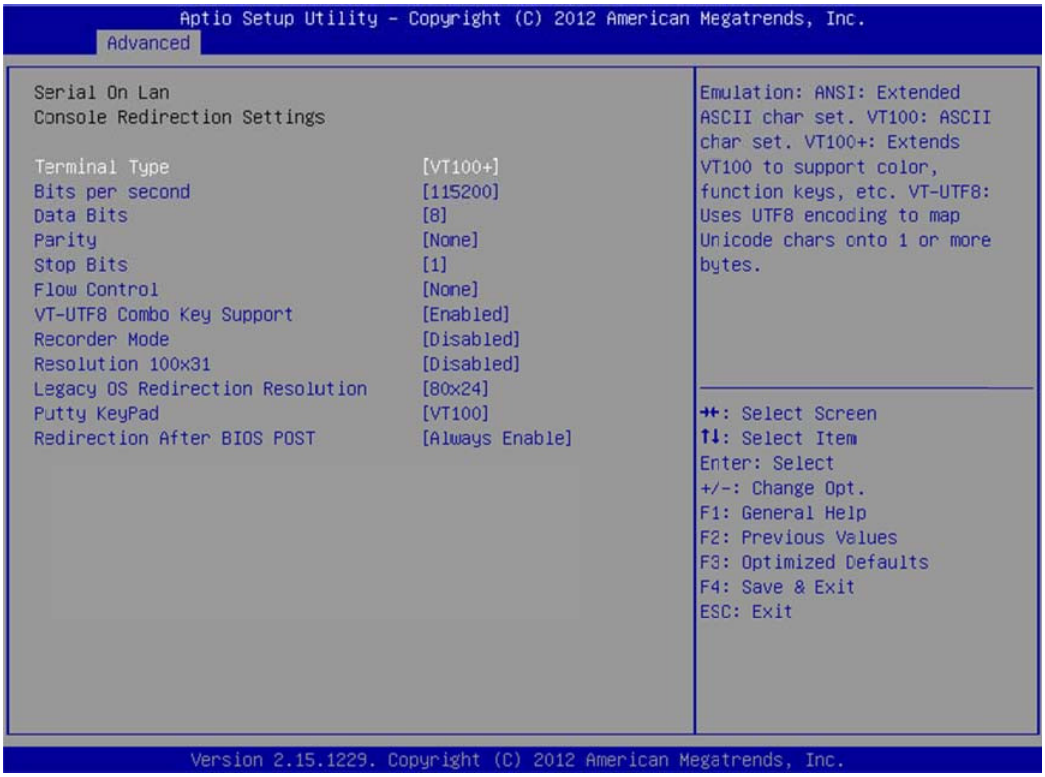
Putty Keypad

Select Function key and Keypad on Putty.

Redirection after BIOS POST

The Settings specify if BootLoader is selected than Legacy console redirection is disabled before booting t o Legacy OOS. Default value is Always Enable le which means Legacy console Redirection is enabled for Legacy OS.

4.4.6.3 Serial on LAN



Terminal Type

Emulation: ANNSI: Extended ASCII I char set. VT100: AASCII char set. VT1000+: Extends VT1000 to Support color, function keys, etc. VT-UTFF8: Uses UTTF8 encoding to map Unicode chars onto 1 or more bytes.

Bits per second

Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

Data Bits

Data Bits

Parity

A parity bit can be sent with the data bits to detect some transmission on errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity b bit is 0 if nu m of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.

Stop Bits

Stop bits indicate the end of a serial data packet. (AA start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Flow Control

Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-star t the flow. Hardware flow control uses two wires too send start/stop signals.

VT--UTF8 Combo Key Support

Enable VT-UTFF8 Combination Key Support for ANSI/VT1000 terminals.

Recorder Mode

With this mode enabled only text will be sent. This is to capture Terminal data.

Resolution 100x31

Enables or disables extended terminal resolution.

Legacy OS Redirection Resolution

On Legacy OS, the Number of Rows and Columns supported redirection.

Putty Keypad

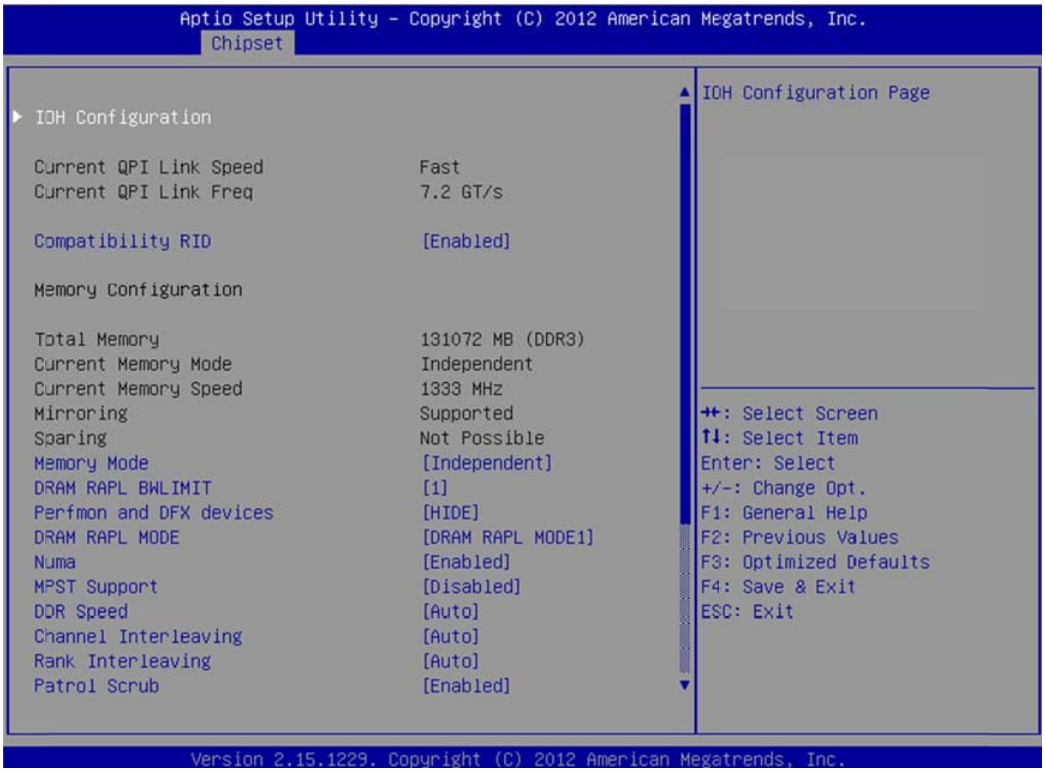
Select Function Key and Key Pad on Putty.

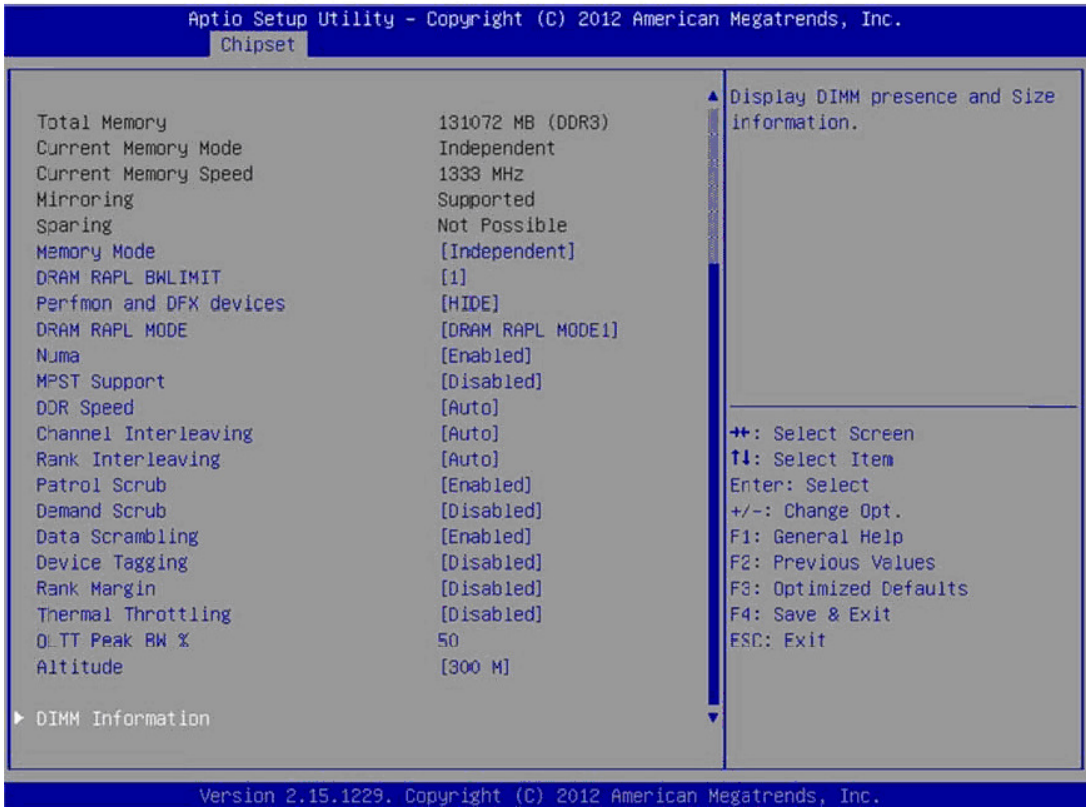
Redirection After BIOS POST

The Settings specify if BootLoader is selected than Legacy console redirection is disabled before booting t o Legacy OOS. Default value is Always Enable which means Legacy console Redirection is enabled for Legacy OS.

4.5 Chipset

4.5.1 North Bridge / IOOH Configuration


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Chipset
IOH Configuration
Current QPI Link Speed Fast
Current QPI Link Freq 7.2 GT/s
Compatibility RID [Enabled]
Memory Configuration
Total Memory 131072 MB (DDR3)
Current Memory Mode Independent
Current Memory Speed 1333 MHz
Mirroring Supported
Sparing Not Possible
Memory Mode [Independent]
DRAM RAPL BWLIMIT [1]
Perfmon and DFX devices [HIDE]
DRAM RAPL MODE [DRAM RAPL MODE1]
Numa [Enabled]
MPST Support [Disabled]
DDR Speed [Auto]
Channel Interleaving [Auto]
Rank Interleaving [Auto]
Patrol Scrub [Enabled]
IOH Configuration Page
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1229. Copyright (C) 2012 American Megatrends, Inc.



Compatibility RID

Support for Compatibility Revision IID (CRID) Functionality mentioned in Sandy Bridge BIOS spec.

Memory Mod e

Select the mode for memory initialization.

DRAAM RAPL BBWLIMIT

DRAAM RAPL BWWLIMIT: Intel Recommended values.

Perfmon and DFX devices

Perfmon and DDFX devices can be hidden or unhidden.

DRAM RAPL MMODE

DRAAM RAPL MODES: Disable/MODE0/MODE1

Memory Mode

Select the mode for memory initialization.

DRAAM RAPL BBWLIMIT

DRAAM RAPL BWWLIMIT: Intel Recommended values.

DRAAM RAPL MMODE

DRAAM RAPL MODES: Disable/MODE0/MODE1

Numa

Enable or Disable Non uniform Memory Access (NUMA).

MPST Support

Enable or Disable MPST Support. Along with enabling MPST Support, it also requires NUMMA to be enabled and Channel Interleaving to be set too 1-way for MPST tables to be published.

DDRR Speed

Force DDR Speed.

Channel Interleaving

Select different Channel Interleaving setting.

Rank Interleaving

Select different rank Interleaving setting.

Patrol Scrub

Enable/Disable Patrol Scrub.

Demand Scrub

Enable/Disable Demand Scrubbing Feature.

Data Scrambling

Enable/Disable Data Scrambling.

Device Tagging

Enable/Disable Device Tagging.

Rank Margin

Enable/Disable Rank Margin.

Thermal Throttling

CLTTTT - Closed Loop Thermal Throttling, OLTT - Open Loop Thermal Throttling

OLTT Peak BW %

Valid Offset 25 - 100. This is a percentage of the peak bandwidth allowed for OOLTT

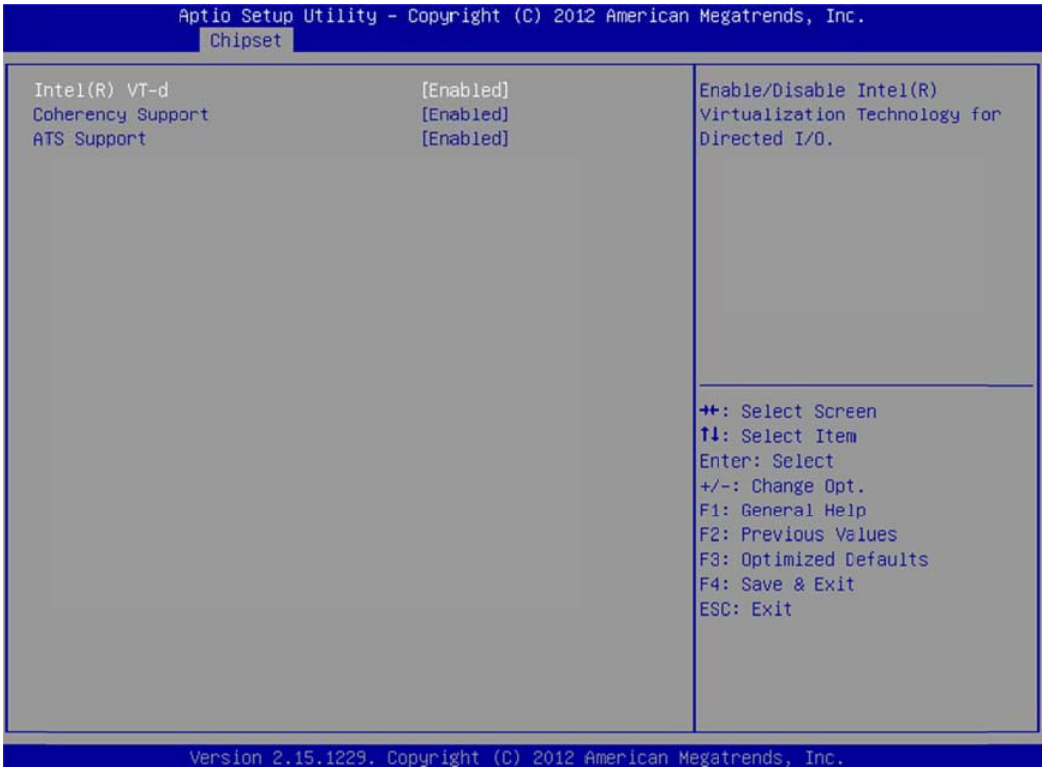
Altitude

The system altitude above the sea level in meters.

DIMM Information

This screen shows the memory information.

4.5.2 North Bridge / Intel® VT for Directed I/O Configuration



Intel(R) VT-d

Enable/Disable Intel(R) Virtualization Technology for Directed I/O.

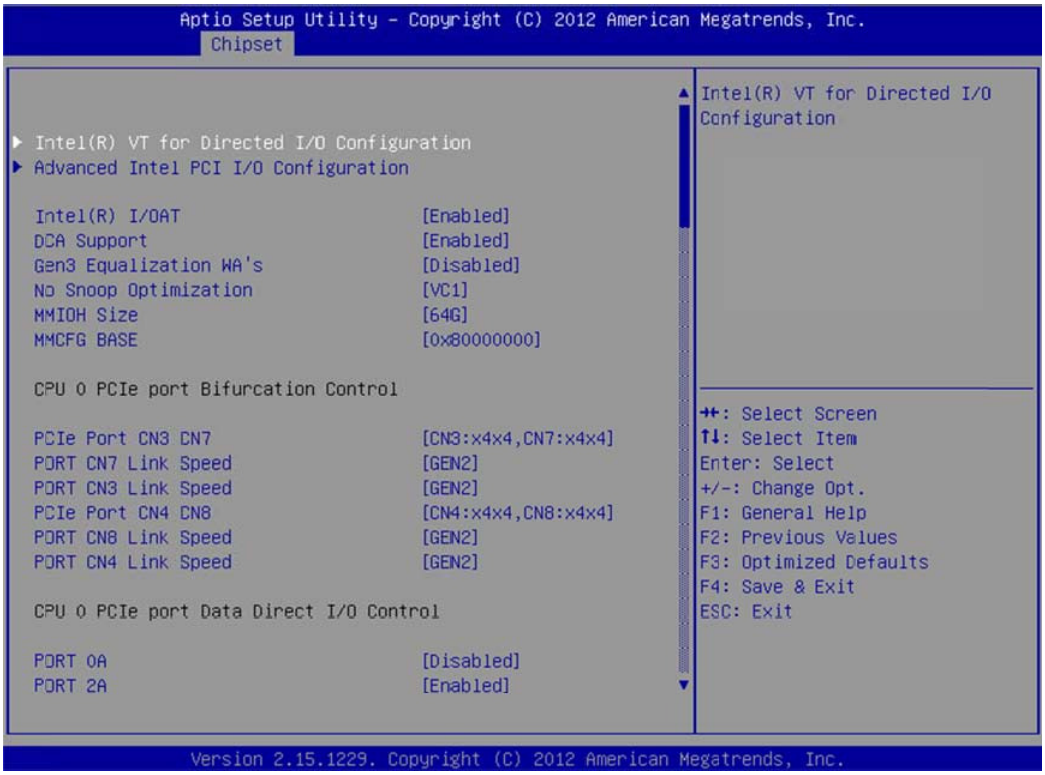
Coherency Support

Enable/Disable VT-d Engine Coherency support.

ATSS Support

Enable/Disable VT-d Engine Address Translation Services (ATS) support.

4.55.3 North Bridge / Advanced Intel PPCI I/O Configuration



Intel® I/OAAT

Enables/Disables Intel(R)) I/O Acceleration Technology (I//OAT).

DCAA Support

Enables/Disables Direct Cache Access Support.

Gen3 Equalization WA's

Support for Gen3 Equalization Workarounds mentioned inn SNB_BSUU Version 0 .83

No Snoop Optimization

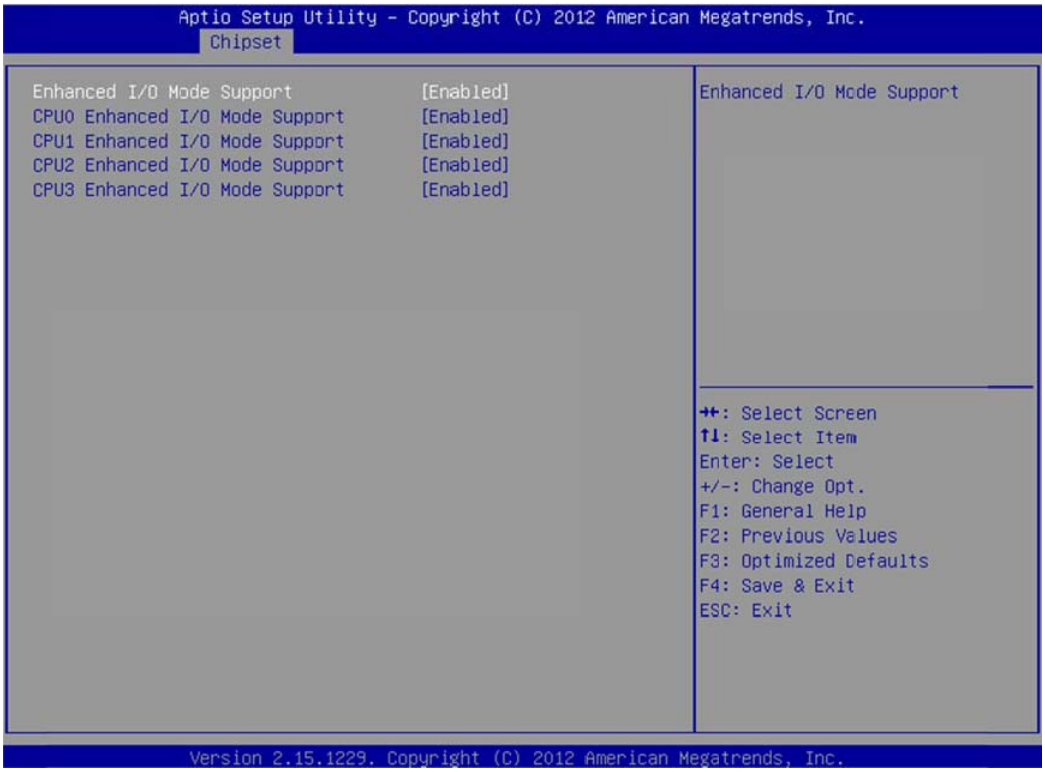
This configuration requires that No Snoop in PCI Express Settings is enabled. It is recommended that this option is left at default (VC1)

MIOH Size

Select number of 1GB contiguous regions to bee assigned for MMIOH space per CPU.

MCFG BASE

MCFG BASE Values.



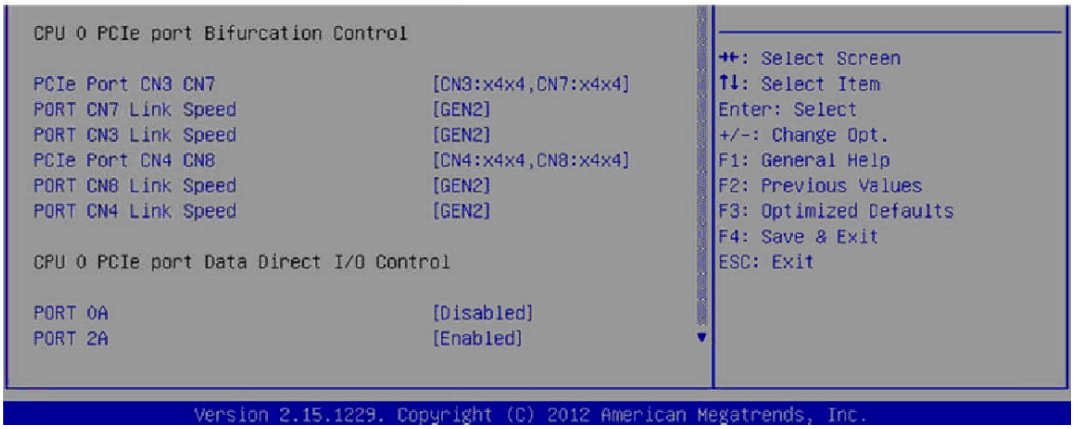
Enhance IO Mode Suppport

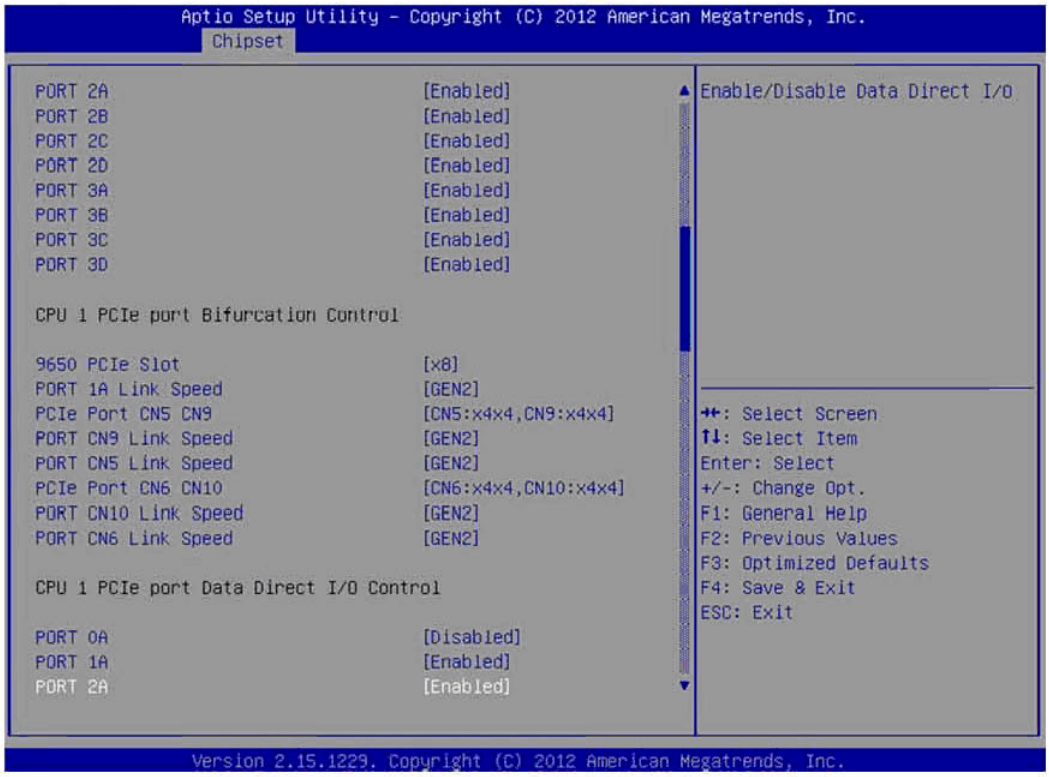
Enhance IO Moode Supporrt for PCIe

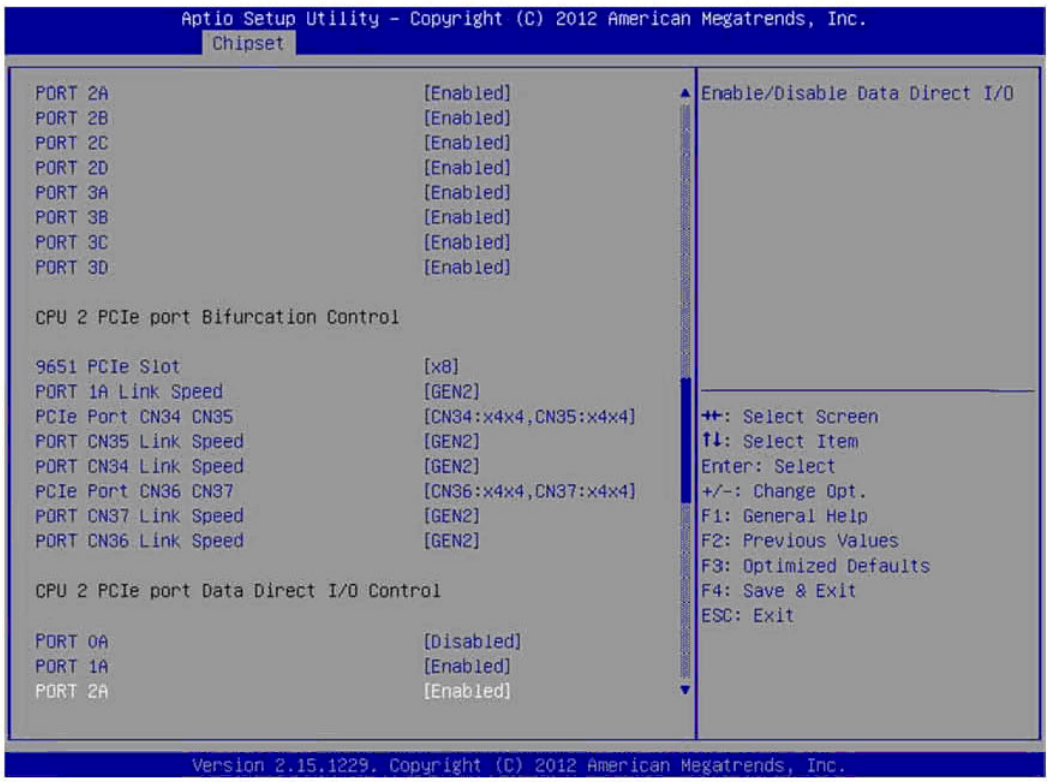
***The SPL-80150 can auto set & config PCIe lanes for LAN module, if**

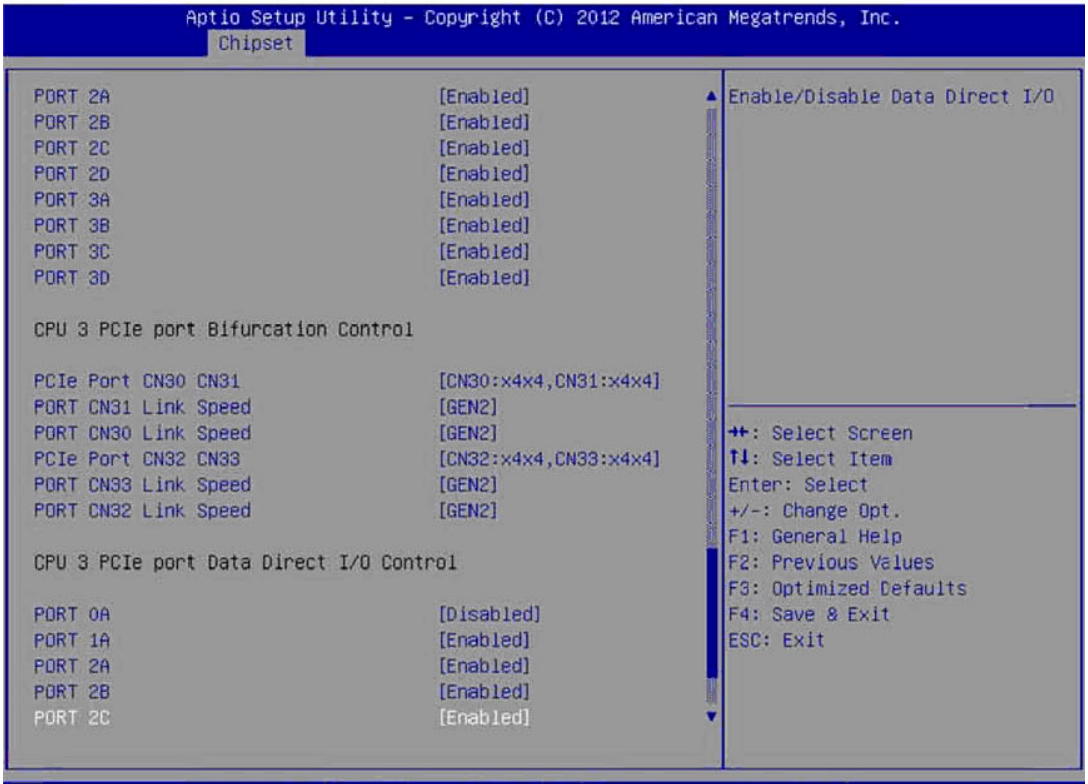
there are no problem, please keep the original settings. However, if any setting is incorrect that will cause unpredictable errors.

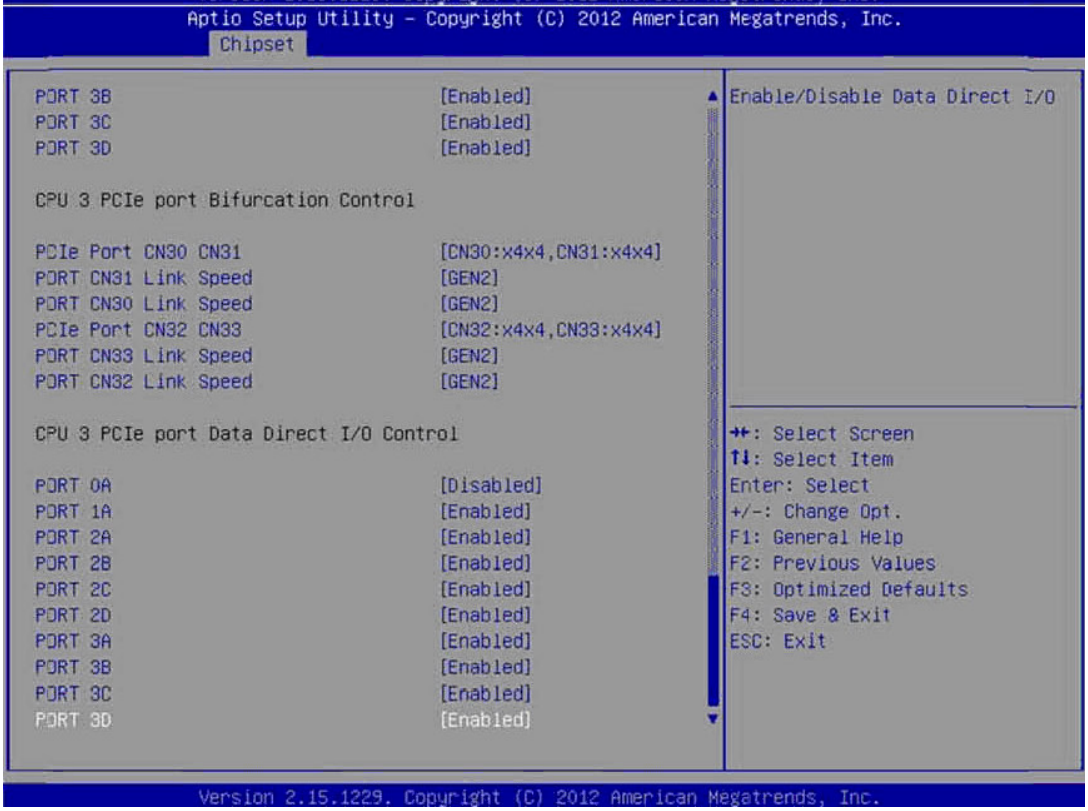
PCIe Configuration drawing for PL-80150

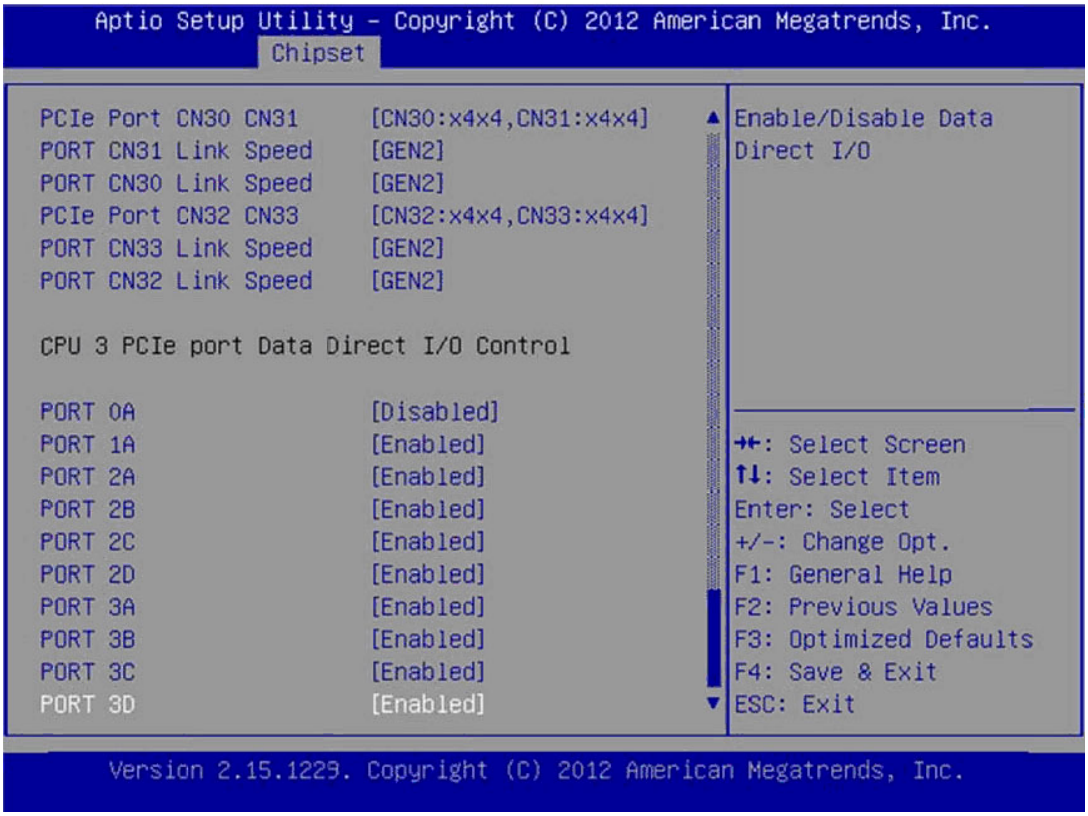



Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Chipset
PORT 2A [Enabled]
PORT 2B [Enabled]
PORT 2C [Enabled]
PORT 2D [Enabled]
PORT 3A [Enabled]
PORT 3B [Enabled]
PORT 3C [Enabled]
PORT 3D [Enabled]
CPU 1 PCIe port Bifurcation Control
9650 PCIe Slot [x8]
PORT 1A Link Speed [GEN2]
PCIe Port CN5 CN9 [CN5:x4x4,CN9:x4x4]
PORT CN9 Link Speed [GEN2]
PORT CN5 Link Speed [GEN2]
PCIe Port CN6 CN10 [CN6:x4x4,CN10:x4x4]
PORT CN10 Link Speed [GEN2]
PORT CN6 Link Speed [GEN2]
CPU 1 PCIe port Data Direct I/O Control
PORT 0A [Disabled]
PORT 1A [Enabled]
PORT 2A [Enabled]
Enable/Disable Data Direct I/O
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1229. Copyright (C) 2012 American Megatrends, Inc.

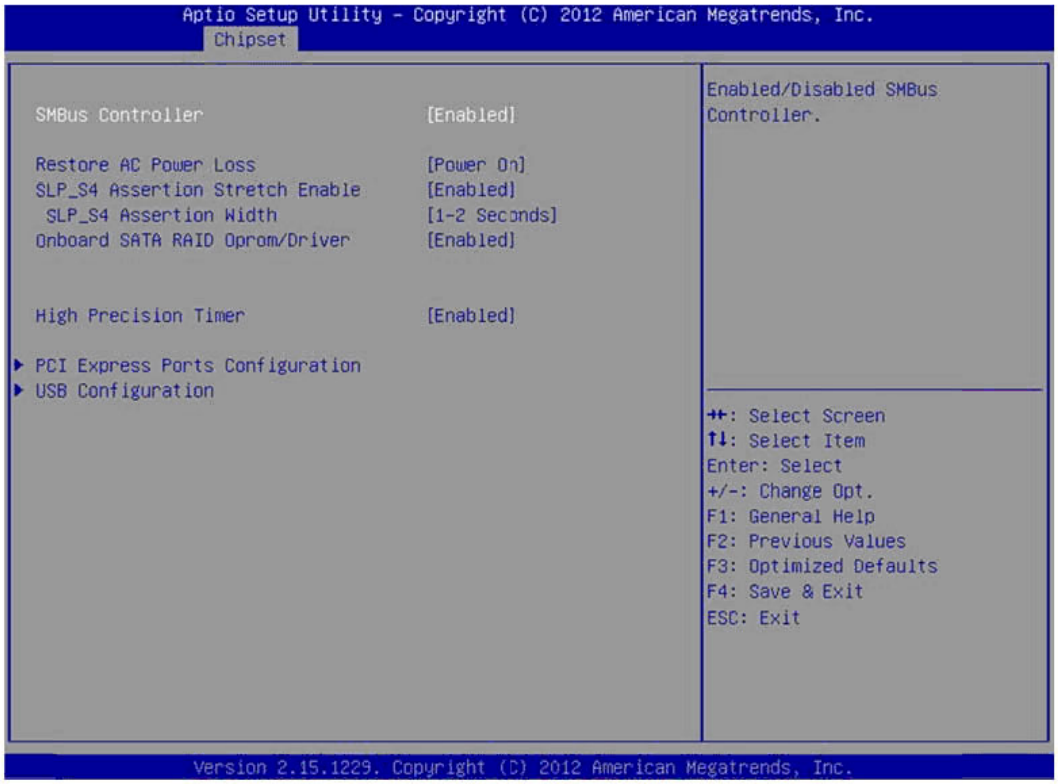

Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Chipset
PORT 2A [Enabled]
PORT 2B [Enabled]
PORT 2C [Enabled]
PORT 2D [Enabled]
PORT 3A [Enabled]
PORT 3B [Enabled]
PORT 3C [Enabled]
PORT 3D [Enabled]
CPU 2 PCIe port Bifurcation Control
9651 PCIe Slot [x8]
PORT 1A Link Speed [GEN2]
PCIe Port CN34 CN35 [CN34:x4x4,CN35:x4x4]
PORT CN35 Link Speed [GEN2]
PORT CN34 Link Speed [GEN2]
PCIe Port CN36 CN37 [CN36:x4x4,CN37:x4x4]
PORT CN37 Link Speed [GEN2]
PORT CN36 Link Speed [GEN2]
CPU 2 PCIe port Data Direct I/O Control
PORT 0A [Disabled]
PORT 1A [Enabled]
PORT 2A [Enabled]
Enable/Disable Data Direct I/O
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1229. Copyright (C) 2012 American Megatrends, Inc.


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Chipset
PORT 2A [Enabled]
PORT 2B [Enabled]
PORT 2C [Enabled]
PORT 2D [Enabled]
PORT 3A [Enabled]
PORT 3B [Enabled]
PORT 3C [Enabled]
PORT 3D [Enabled]
CPU 3 PCIe port Bifurcation Control
PCIe Port CN30 CN31 [CN30:x4x4,CN31:x4x4]
PORT CN31 Link Speed [GEN2]
PORT CN30 Link Speed [GEN2]
PCIe Port CN32 CN33 [CN32:x4x4,CN33:x4x4]
PORT CN33 Link Speed [GEN2]
PORT CN32 Link Speed [GEN2]
CPU 3 PCIe port Data Direct I/O Control
PORT 0A [Disabled]
PORT 1A [Enabled]
PORT 2A [Enabled]
PORT 2B [Enabled]
PORT 2C [Enabled]
Enable/Disable Data Direct I/O
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1229. Copyright (C) 2012 American Megatrends, Inc.


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Chipset
PORT 3B [Enabled]
PORT 3C [Enabled]
PORT 3D [Enabled]
CPU 3 PCIe port Bifurcation Control
PCIe Port CN30 CN31 [CN30:x4x4,CN31:x4x4]
PORT CN31 Link Speed [GEN2]
PORT CN30 Link Speed [GEN2]
PCIe Port CN32 CN33 [CN32:x4x4,CN33:x4x4]
PORT CN33 Link Speed [GEN2]
PORT CN32 Link Speed [GEN2]
CPU 3 PCIe port Data Direct I/O Control
PORT 0A [Disabled]
PORT 1A [Enabled]
PORT 2A [Enabled]
PORT 2B [Enabled]
PORT 2C [Enabled]
PORT 2D [Enabled]
PORT 3A [Enabled]
PORT 3B [Enabled]
PORT 3C [Enabled]
PORT 3D [Enabled]
Enable/Disable Data Direct I/O
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1229. Copyright (C) 2012 American Megatrends, Inc.



4.5.4 Chipset/South Bridge



SMBus Controller

Enabled/Disabled SMBus Controller.

Restore AC Power Loss

Specify what state to go to when power is re-applied after a power failure (G3 state).

SLPP_S4 Assertion Stretch Enable

Enabled/Disabled SLP_S44# Assertion Stretch.

SLPP_S4 Assertion Width

Select a minimum assertion width of the SLP_S4# signal.

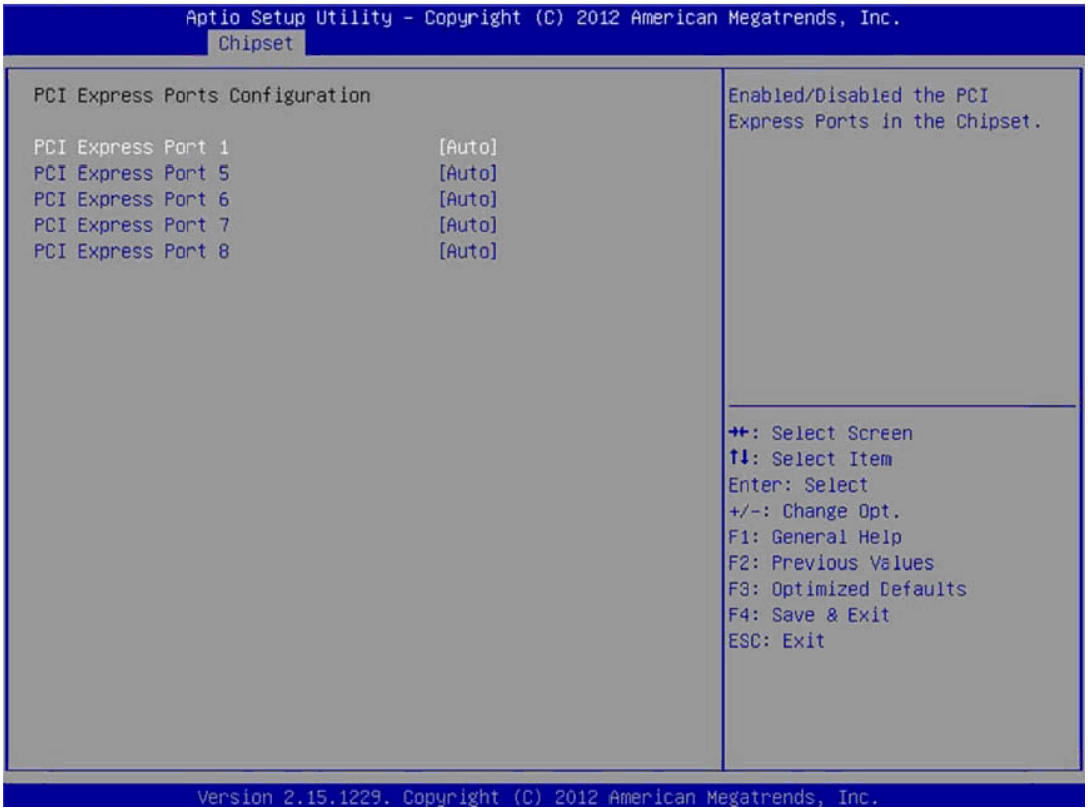
Onboard SATA RAID Oprom/Driver

Controls whether to enable the onboard SATA Option ROM or EFI Driver.

High Precision Timer

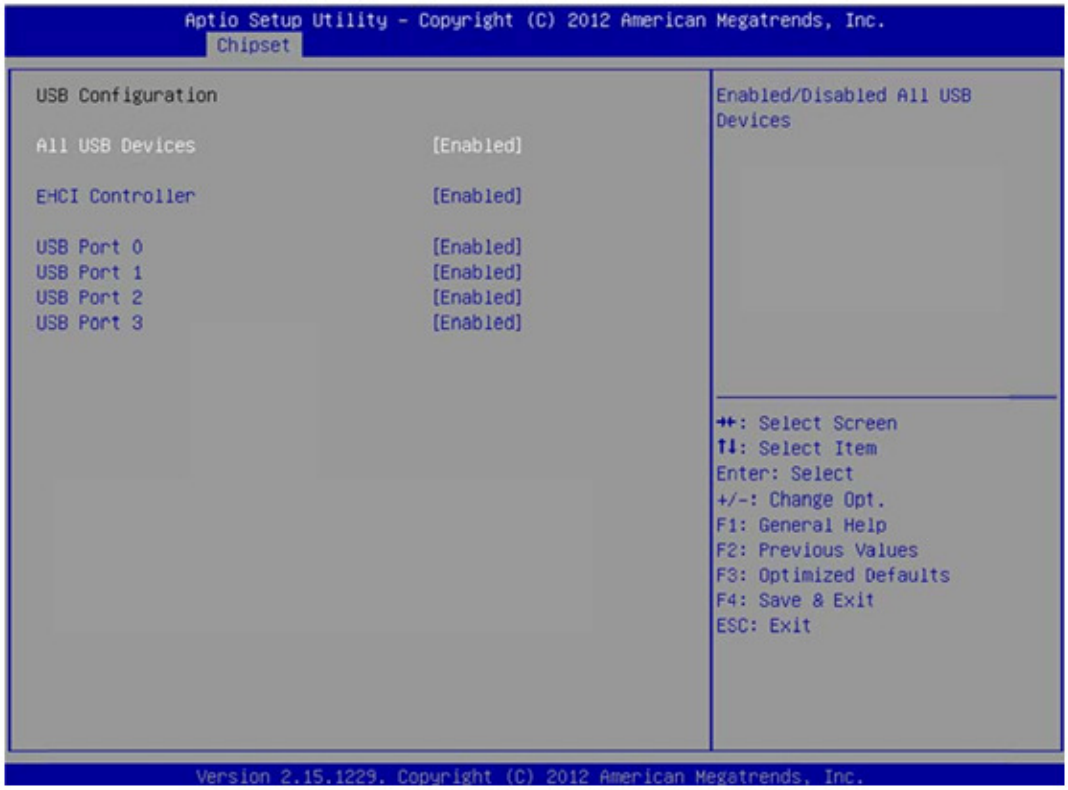
Enabled/Disabled the High Precision Event Timer.

4.4.7.5 Chipset/South Bridge / PCI Express Ports Configuration



PCI Express Port 1,5,6,7,8

Enabled/Disabled the PCI Express Ports in the Chipset.



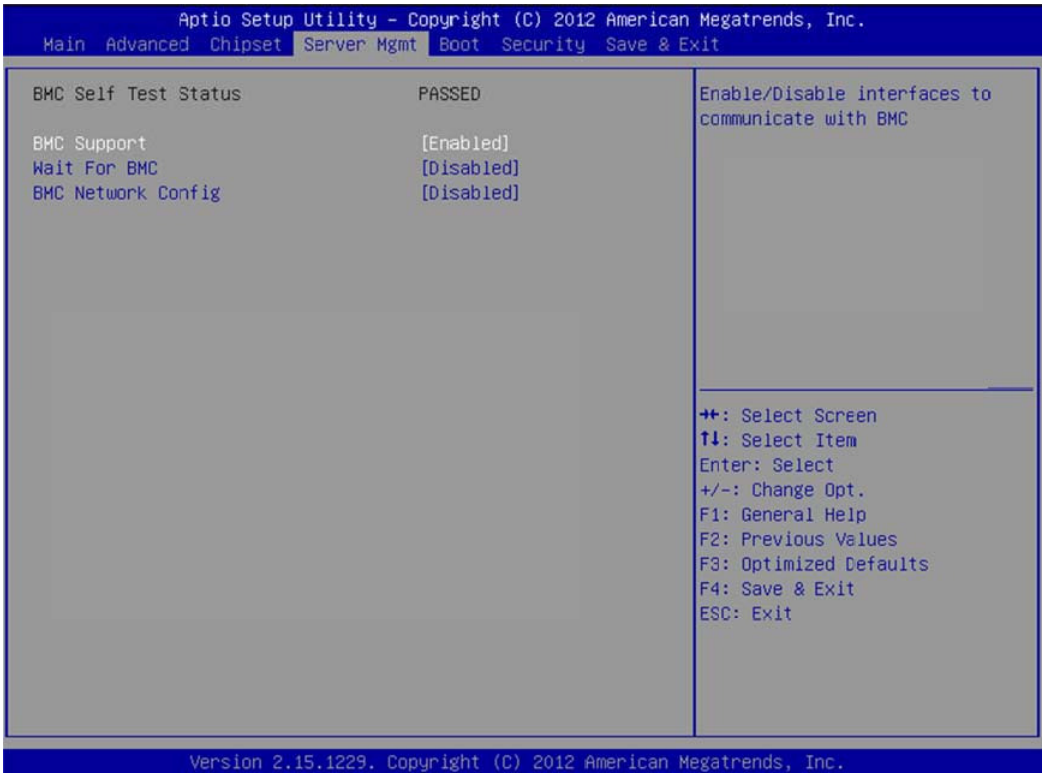
EHCCI Controller

Enabled/Disabled USB 2.0 (EHCI) S Support

USB Port 0, 1, 2, 3

Enabled/Disabled All USBB Devices

4.6 Server Mgmt



BMC Support

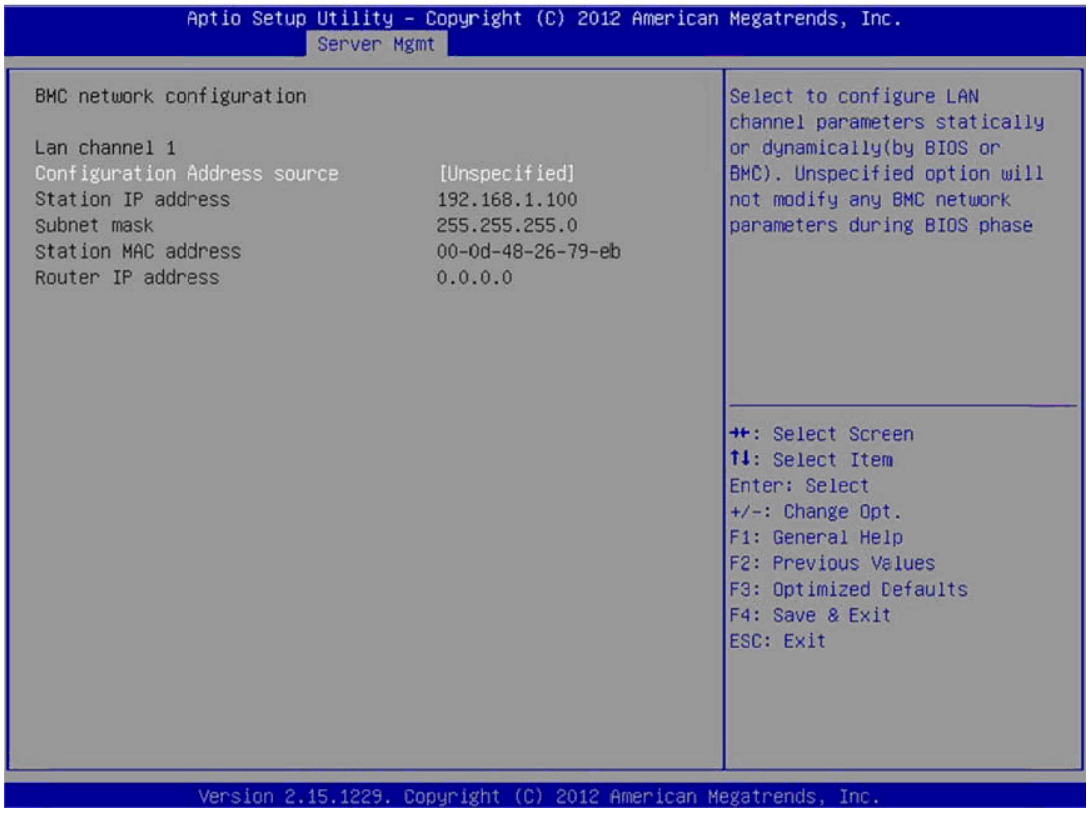
Enable/Disable interfaces to communicate with BMC

Wait For BMC

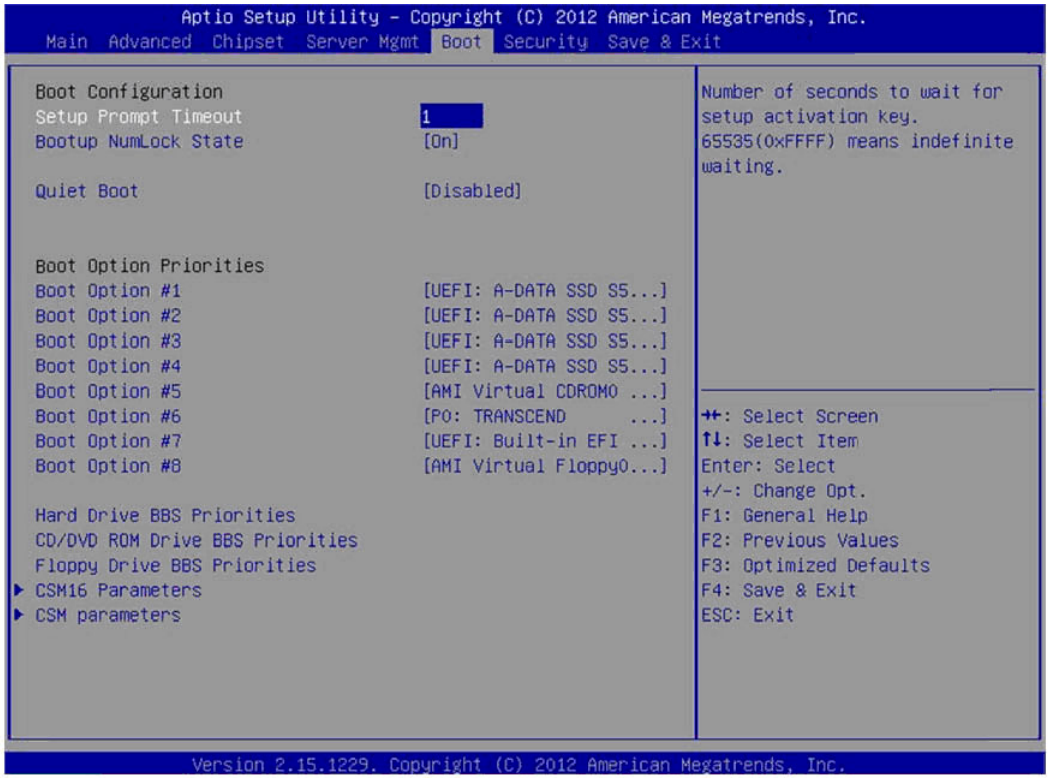
Wait for BMC response for specified time out. In PILOTIII, BMC starts at the same time when BIOOS starts during AC power ON. It takes around 30 seconds to initialize Host to BMC interfaces.

BMC Network Config

BMC Network Config


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Server Mgmt
BMC network configuration
Lan channel 1
Configuration Address source [Unspecified]
Station IP address 192.168.1.100
Subnet mask 255.255.255.0
Station MAC address 00-0d-48-26-79-eb
Router IP address 0.0.0.0
Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1229. Copyright (C) 2012 American Megatrends, Inc.

4.7 Boot


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Main Advanced Chipset Server Mgmt Boot Security Save & Exit
Boot Configuration
Setup Prompt Timeout 1
Bootup NumLock State [On]
Quiet Boot [Disabled]
Boot Option Priorities
Boot Option #1 [UEFI: A-DATA SSD S5...]
Boot Option #2 [UEFI: A-DATA SSD S5...]
Boot Option #3 [UEFI: A-DATA SSD S5...]
Boot Option #4 [UEFI: A-DATA SSD S5...]
Boot Option #5 [AMI Virtual CDROM0 ...]
Boot Option #6 [P0: TRANSCEND ...]
Boot Option #7 [UEFI: Built-in EFI ...]
Boot Option #8 [AMI Virtual Floppy0...]
Hard Drive BBS Priorities
CD/DVD ROM Drive BBS Priorities
Floppy Drive BBS Priorities
▶ CSM16 Parameters
▶ CSM parameters
Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1229. Copyright (C) 2012 American Megatrends, Inc.

Setup Prompt Timeout

Use the <+> and <-> keys to adjust the number of seconds to wait for setup activation key.

Bootup NumLock State

This item allows you to select "On" or "Off" power-on state for the NumLock.

Quiet Boot

If this option is set to Disabled, the BIOS displays normal POST messages. If enabled, an O EM Logo is shown instead of POSST messages.

Boot Option Priorities

Choose boot priority from boot device.

Hard Disk Drive BS Priorities

Specifies the Boot Device Priority sequence from available Hard Drives.

CD/DVD ROM Drive BBS Priorities

Specifies the Boot Device Priority sequence from available e CD/DVD Drives.

NETWORK Device BBS Priorities

Specifies the Boot Device Priority sequence from available NETWORK Drives.

CSMM16 Parameters

Enable/Disable, Option ROM execution settings, etc.

GateA20 Active

UPON REQUEST - GA20 can be disabled using BIOS services. ALWAYS - do not allow disabling GA200; this option is useful when any RT code is executed above 1MB.

Option ROM Messages

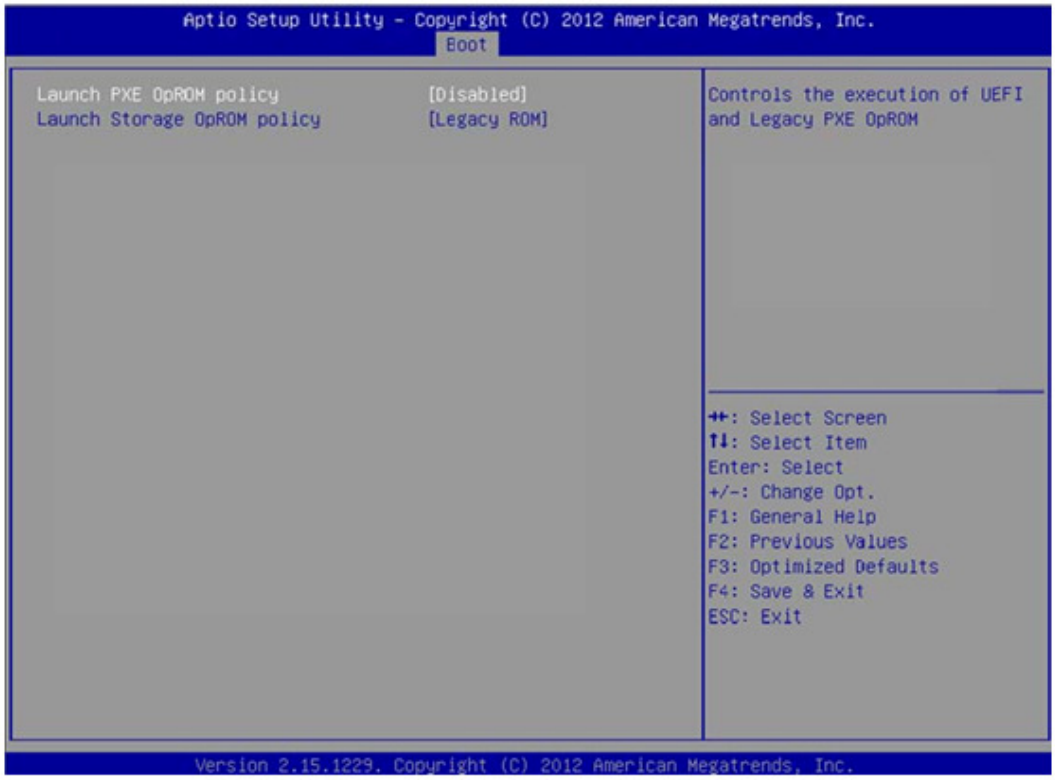
Set display mode for Option ROM.

INT19 Trap Response

BIOS reaction on INT19 trapping b by Option ROM: IMMEDIATE - execute the trap right away; POSTPONED - execute the trap during legacy boot.

CSM parameters

OpROM execution, boot Option filter, etc.



Launch PXE OpROM policy

Controls the execution off UEFI and Legacy PXEE OpROM

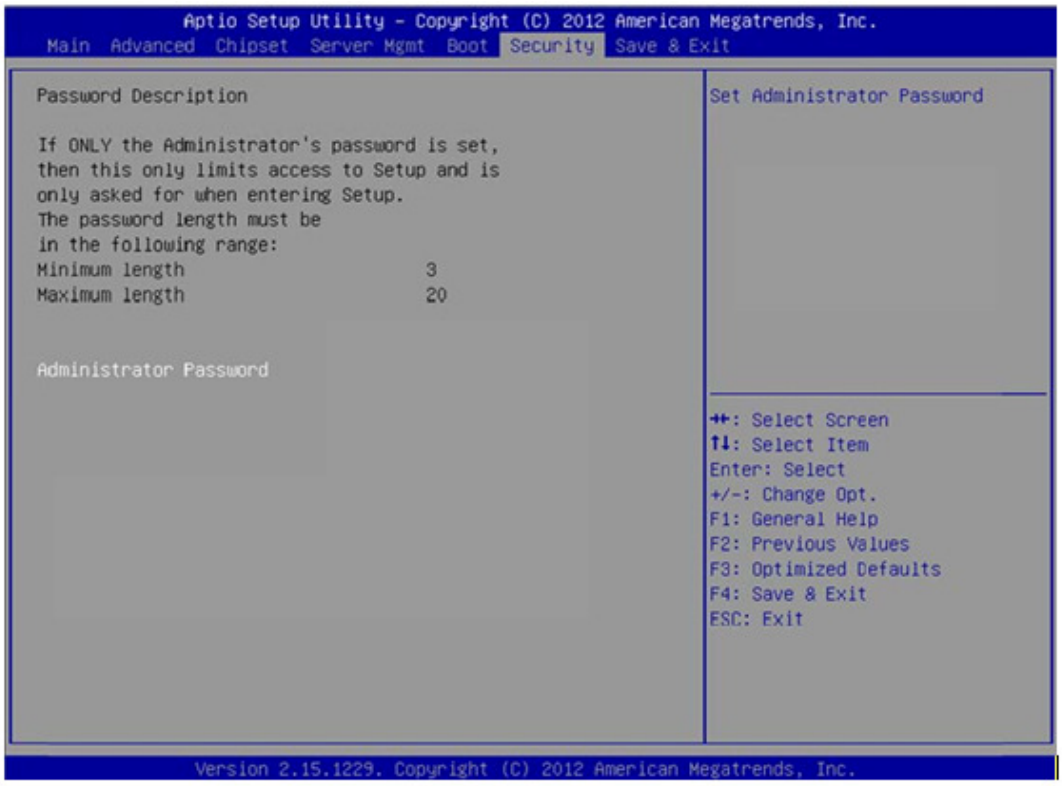
Launch Storage OpROM policy

Controls the execution off UEFI and Legacy Storage OpROM

4.4.10 Security Menu

⇩Use the Security Setup option as follows:

1 Choose "Security" from the main menu. The following screen appears:
2 Move between items and select values by using the arrow keys. Modify the selected fields using the PgUP/PgDN key s. Please press the <F1> key for information on the various options.
3 After you have finished with the Security setup, press the < · > or < · > key to switch to other setup menu or press <F4> key to save setting.



Administrator Password:

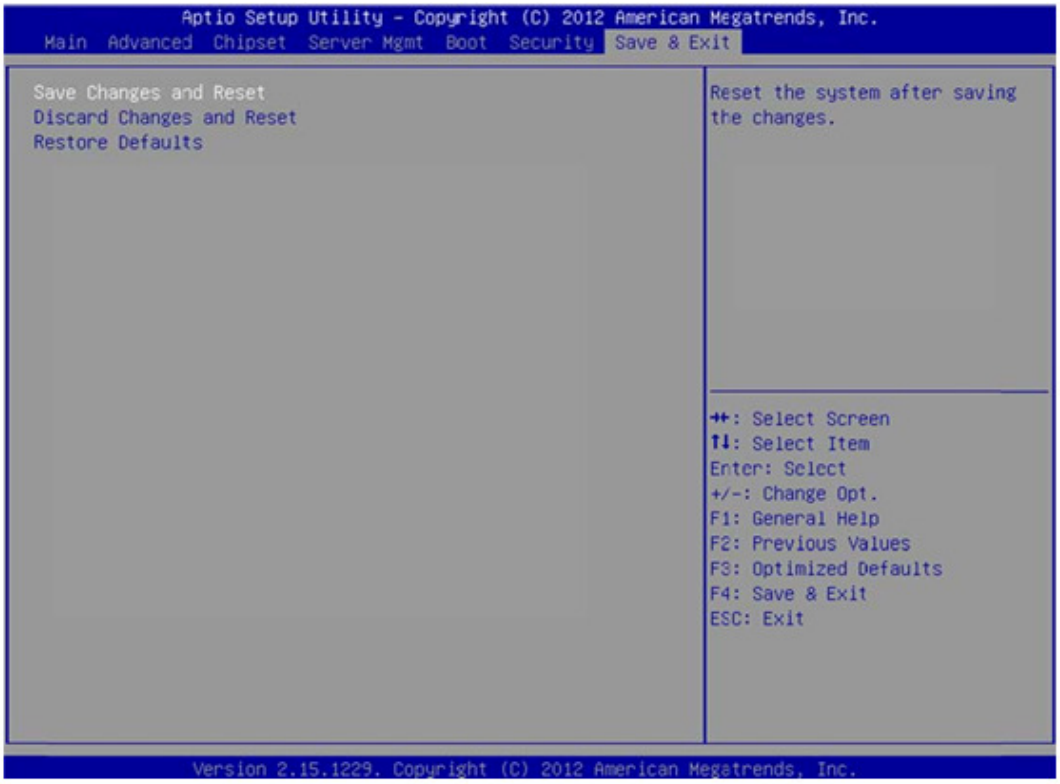
This item allows you to set or change the administrator password. The Administrator Password item on top of the screen shows the default Nott Installed. After you have set a password, this item shows Installed.

4.8 Save & Exit

The item allows you to save or discard your changes to the BIOS items, and load the optimal defaults or user defaults for the BIOS items.

⇩Use the Exit option as follows:

1 Choose "Exit" from the main menu, the following screen appears.
2 Move between items and select values by using the arrow keys. Modify the selected fields using the PgUP/PgDN keys. For information on the various options, please press <F1>> key.
3 Press the < · > or< · > key to switch to other setup menu or press <F4> key to save setting.



Save Changes and Reset:

Store all changes you made into CMOS and reboot system. F4 key can be used for this operation.

Discard Changes and Reset:

Discard all changes you made and reboot system. ESC key can bee used for this operation.

Restore Defaults:

This item allows you to load optimal defaults for each setting on the Setup Utility menus, which will provide the best performance settings for system. F3 key can be used for this operation.

Chapter 5. Utility & Driver Installation

Please install the GbE module properly before you install the OS, driver or other software.

5.1 Operation System Supporting

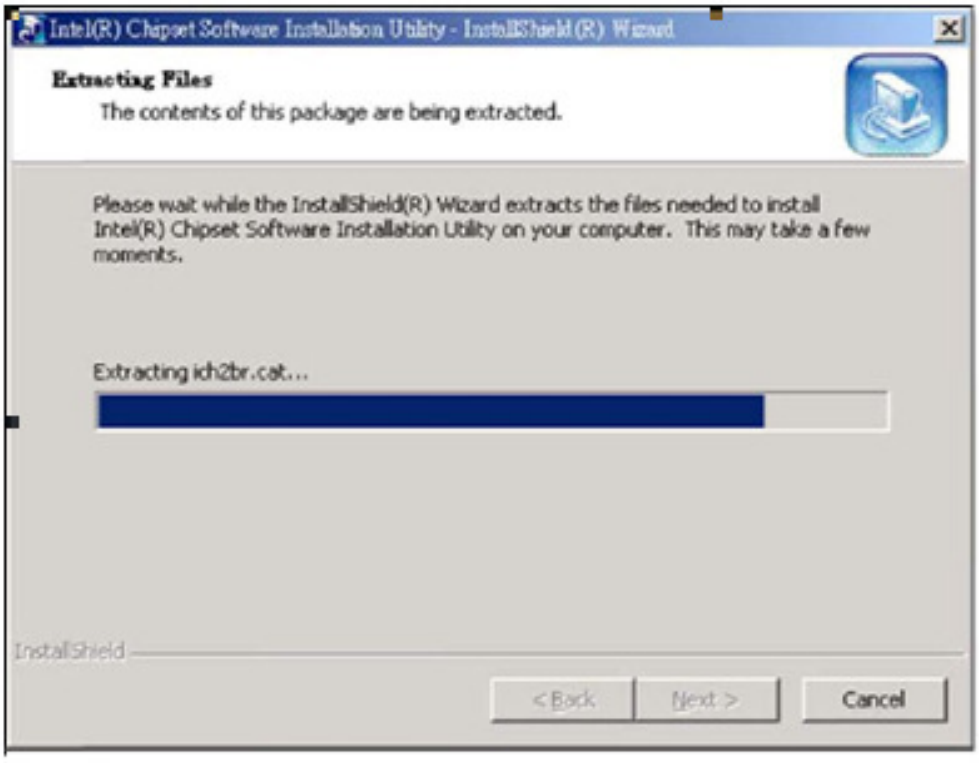
PL-80150 can support Windows® and Linux® operation system as follows. Before installation, please check your OS version. If your OS is

not in the following list, please upgrade your OS version.

OS	Version
DOOS	DOS 6.222
Windows®	Microsoft Windows Server 2008R2 Enterprise (x64) Microsoft Server 2008 Enterprise (x32 and x64) Microsoft Windows Server 2012 (x64)
Linux®	Red Hat SUSE Li t Enterprise Linux Server* (x32 and 64) SUSE Linux Enterprise Server (x32 and x64)

5.2 System Driver Installation

PL-80150 offers the system driver in the setup CCD. Please install the driver following the procedures.



5.3 LAN Driver Installation

PL-80150 offers the LAN driver in the setup CDD. Please click the Autorun file and install the driver following the procedures.

1 Insert the setup CCD of SCBB-9650 into your CCD-ROM drive.
2 Choose the Drivers file to click the Autorun icon.
3 Follow the procedures to finish the installation.

Appendix A: DOS / Linux Sample Code

We offer some sample code for PL-80150 appliance for customer needs. Sample code is placed into the Driver CD for software development use.

Appendix B: Cable Development Kit

The PL-80150 offers some cables for development use.

DK002

Item & Description	Part No.	Qty
Ethernet Cat.5 Cable 2M/ RoHS	CB-EC5200-00	1
Cross Over 2M Color/ RoHS	CB-CO5202/4-00	1
RJ45 to DB9 2M Cable/ RoHS	CB-RJDB91-00	1
2m null modem cable/ RoHS	CB-DB9200-01	1
VVGA CABLE (2mmm) 15CM/ RoHS	CB-IVGA01-00	1
KB/MS CABLE 15CCM/ RoHS	CB-IPS 200-00	1
USB CABLE/ RoHS	CB-IUSB01-00	1

CB-EC5200-00

CB-CO5202/4-00

CB-RJDB91-00

CB-DB9200-00

CB-IVGA01-00

CB-IPS200-00

CB-IUSB01-00