PL-80310

Networking Appliance

1U Rackmount Intel® Sandy Bridge Xeon E3/Core i7/i5/i3 Network System, 7 GbE Copper, SATA, CF, LCM, Cavium, PCI-E x8, Bypass

User's Manual

Version 1.1a, 4/10

Manual Edition 1.1a, Jul, 2013

For more information on PL-80310 or other WIN ENTERPRISES products, please visit our website http://www.win-ent.com.

For technical support send your inquiries to sales@win-ent.com.

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Chapter 1. General Information

1.1 Introducing

The PL-80310 is a 1U rackmounted hardware platform designed for high performance network service applications. Built with Intel® new generation microprocessor architecture on 32nm process technology, the PL-80310 supports Intel® Sandy Bridge Xeon E3 and Core i7/i5/i3 processors with Intel® Advanced Vector Extensions and Turbo Boost Technology.

The platform supports four unbuffered ECC or non-ECC DDR3 1066/1333MHz DIMM sockets with memory up to 32GB. In order to provide the best network performance and best utilization, the powerful storage interfaces include one 3.5" SATA 3.0 6Gbps and CompactFlash™. In order to enhance network security performance, PL-80310 affords optional onboard Cavium Nitrox PX CN16xx to give hardware level cryptographic acceleration which can leave more CPU computing power for higher layer packet processing. The optional IPMI module support web-based UI for remote management that affords powerful function with KVM over IP, SoL, Virtual Storage Redirection, remote power control and hardware monitor.

This platform 7 GbE and max to 15 GbE Ethernet ports via PCI-E by 8 on the front-panel. To prevent network problems when the platform shuts down, PL-80310 supports two segments of LAN bypass function through WDT and GPIO pin definitions. The front panel also has dual USB 2.0 ports, one RJ-45 console port and LED indicators that monitor power and storage device activities for local system management, maintenance and diagnostics. In addition, the PL-80310 supports one PCI-E by 8 slot, one PCI-E by 8 Golden Finger and one PCI slot.

1.2 Specifications

Processor System	CPU	Support Single Intel® Sandy Bridge Xeon E3/Core i7/i5/i3 processors, LGA1155
	Chipset	Intel® C206 PCH

	DMI BIOS	Up to 5GT/s AMI® Aptio BIOS
Memory	Technology	Dual-channel, ECC/Non-ECC, un-buffered, DDR3 1066/1333MHz memory
	Capacity	Up to 32GB with 4 DIMM sockets
Expansion	Expansion Slots	One PCI-E x8 slot for expansion module One PCI-E x8 golden finger for expansion module (optional Riser card) One PCI-E connector for R199A IPMI module only One PCI slot
Ethernet	GbE Ethernet	Seven RJ45 GbE ports, Intel 82574L PCI-E x1, with two pairs bypass function (optional) 2~8 GbE ports (optional expansion module)
H/W Acceleration	Security Processor	One Cavium NITROX PX CN16xx (option, only available for Xeon E3-1200 series processor)
Remote Management	IPMI	One Aspeed AST2150 Remote Management Module (optional)
Storage	SATA	Internal HDD bay support one 3.5" or two 2.5" SATA HDD
	Compact Flash Socket	One CompactFlash™ Type I/II
I/O	USB	One External Dual USB2.0 One internal USB 2.0 (5x2 pin header)
	Serial	One RJ45 Console port (COM1) One internal header for second console (COM2)
Power Supply	Watt	ATX power supply
Mechanical and Environment	Form Factor	1U rackmount
	LCD Module	one 16x2 LCM
	Keypad	Four buttons keypad
	LED	One Power LED (Green)

		One HDD LED (Yellow) Two Bypass LED (Green)
	Dimension（W x D x H）	435mm (W) x 400mm (D) x 44mm (H) (17.1" W x 15.8" D x 1.7" H)
	Operating Temperature	Operating: 0 ~ 40°C (32 ~ 104°F)
	Humidity	10 ~ 85% relative humidity, non-operating, non-condensing
Weight	1pc/CTN, 10kgs, 55.5cm(W) x 54cm(D) x 22.5cm(H)	
Certification	CE/FCC	

1.3 Ordering Information

We offer some accessories for PL-80310 appliance for various customer needs.

PL-8031A	1U Rackmount Intel® Sandy Bridge Xeon E3/Core i7/i5/i3 Network System, 11 RJ45 GbE, LCM, PCI, PCI-E x8, bypass (CB-8970A + R168A)
PL-8031B	1U Rackmount Intel® Sandy Bridge Xeon E3/Core i7/i5/i3 Network System, 7 RJ45 GbE, 4 SFP, LCM, PCI, PCI-E x8, bypass (CB-8970A + R169A)
PL-8031C	1U Rackmount Intel® Sandy Bridge Xeon E3/Core i7/i5/i3 Network System, 7 RJ45 GbE, LCM, PCI, PCI-E x8, bypass
DK001	Cable development kit

1.4 Packaging

Please make sure that the following items have been included in the package before installation.

1. PL-80310 Appliance
2. Quick Installation Guide (Optional)
3. Cables (Optional)
4. CD-ROM that contains the following folders:

(1) Manual
(2) System Driver
(3) Ethernet Driver
(4) Utility Tools

If any of the above items are missing or damaged, please contact sales@win-ent.com. Retain the box and carton for safe shipping and storage. After you unpack the goods, inspect contents to make sure everything is intact. Do not plug in the power adapter if you find the unit appears damaged.

Note: Keep the PL-80310 in the original packaging until you start installation.

1.5 Precautions

Please make sure you properly ground yourself before handling the PL-80310 appliance or any system components. Electrostatic discharge can be easily damage the PL-80310 appliance.

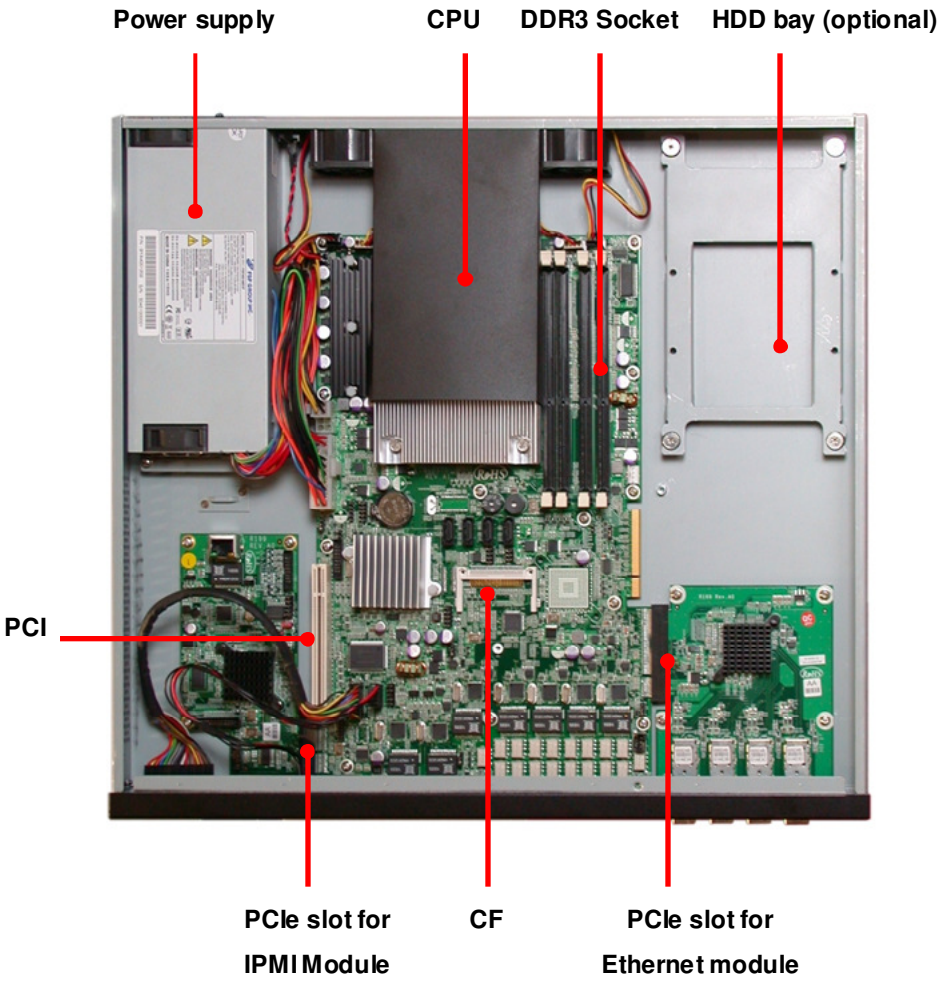
Do not remove the anti-static packing until you are ready to install the PL-80310 appliance.

Ground yourself before removing any system component from its protective anti-static packaging. To ground yourself, grasp the expansion slot covers or other unpainted parts of the computer chassis.

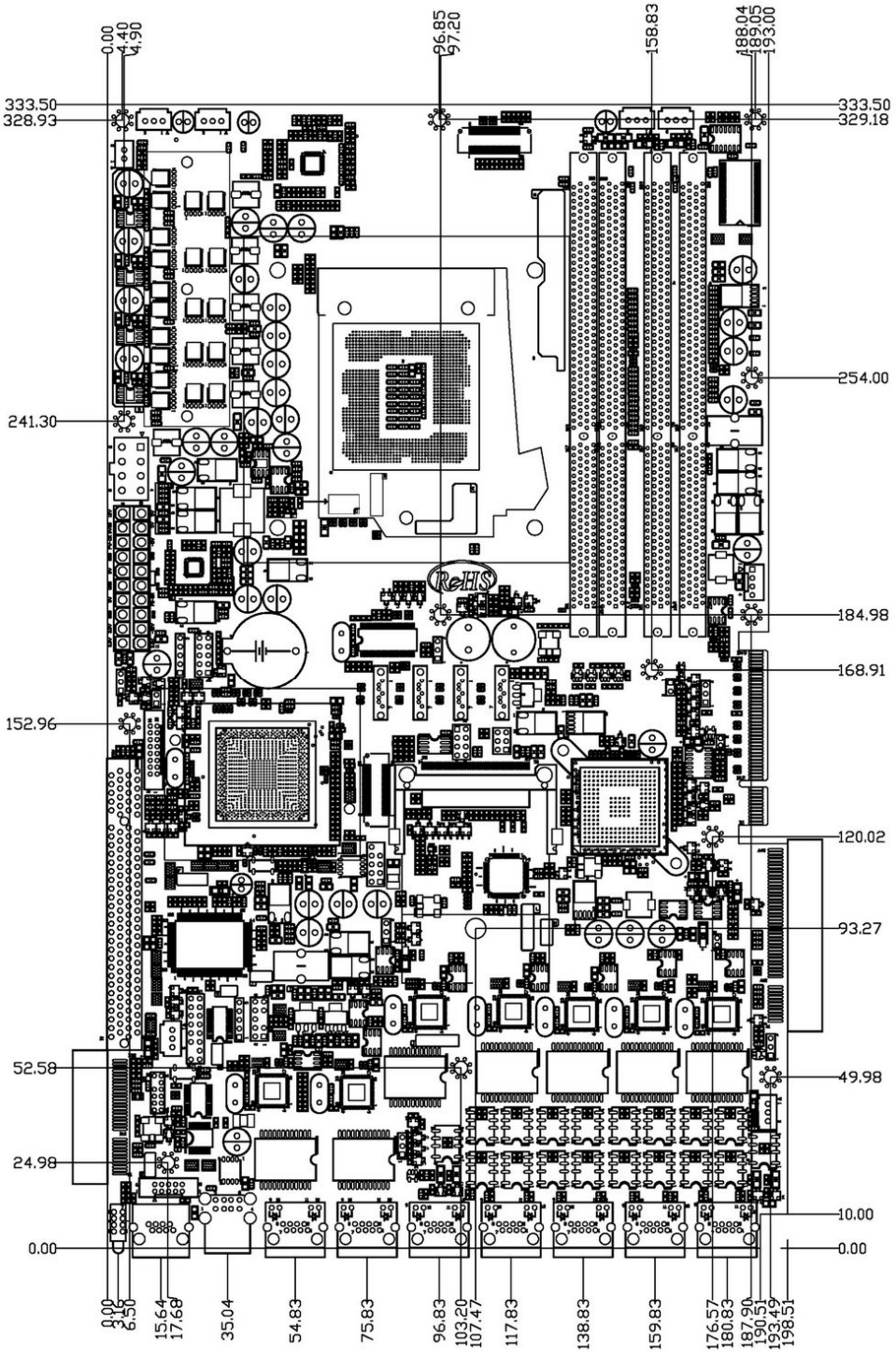
Handle the PL-80310 appliance by its edges and avoid touching its components.

1.6 System Layout

PL-80310 Front Side

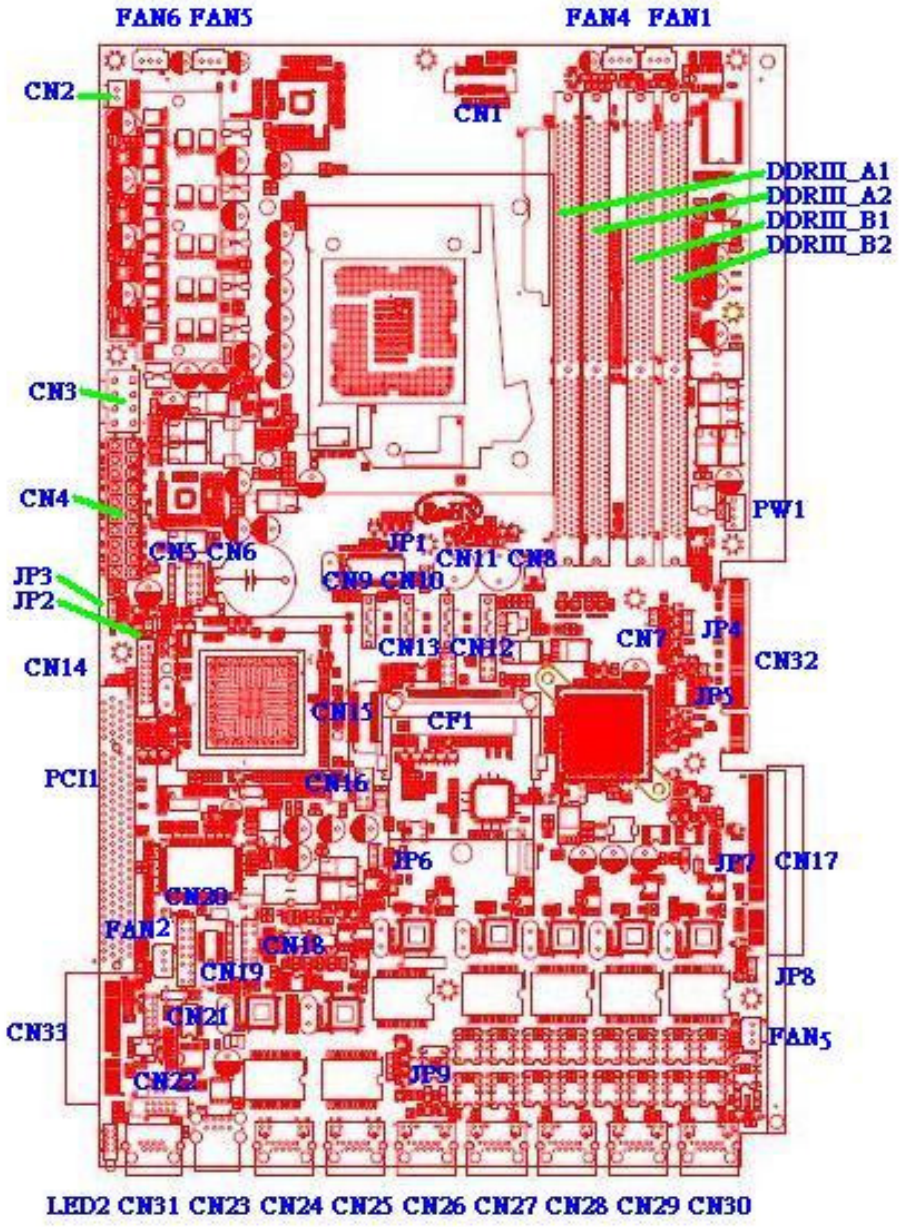


1.7 Board Dimensions



Chapter 2. Connector/Jumper Configuration

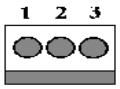
2.1 Connector/Jumper Locations and Definitions



Connector	Define	Connector	Define
FAN 1	FAN Connector	CN19	LCM KEYPAD Pin Header
FAN 2	FAN Connector	CN20	LCM Pin Header
FAN 3	FAN Connector	CN21	LPC Pin Header
FAN 4	SMART FAN Connector	CN22	COM2 Box Header
FAN 5	SMART FAN Connector	CN23	USB0/1 Connector
FAN 6	SMART FAN Connector	CN24	Giga LAN RJ45 Connector
CN2	ATX SWITCH Pin Header	CN25	Giga LAN RJ45 Connector
CN3	+12V Power Connector(8Pin)	CN26	Giga LAN RJ45 Connector
CN4	ATX Power Connector(20Pin)	CN27	Giga LAN RJ45 Connector
CN5	GPI Pin Header	CN28	Giga LAN RJ45 Connector
CN6	GPO Pin Header	CN29	Giga LAN RJ45 Connector
CN7	Reset Pin Header	CN30	Giga LAN RJ45 Connector
CN8	SATA Connector	CN31	COM1 RJ45 Connector
CN9	SATA Connector	CN32	PCI-E x8 Golden Finger
CN10	SATA Connector	CN33	PCI-E x4 SLOT(IPMI)
CN11	SATA Connector	JP3	Power on type
CN13	SPI Pin Header	JP4	Watchdog function
CN14	VGA Pin Header	JP5	PCI-E Golden Finger +5V
CN15	PCH XDP Connector(N/A)	JP6	CLEAR CMOS
CN16	USB2/3 Connector	JP7	PCI-E SLOT +5V
CN17	PCI-E x8 Slot	JP8	LAN1-2 Bypass
CN18	PS2 KB/MS	JP9	LAN3-4 Bypass

2.2 Connector and Jumper Setting

FAN1/FAN2/FAN3/FAN4/FAN5/FAN6: FAN Connector

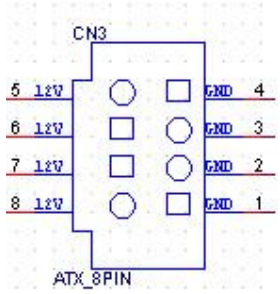


Pin	Define
1	Ground
2	+12V
3	Speed Detect

CN2：ATX SWITCH Pin Header

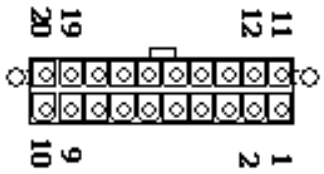
Pin	Define
1	5VSB
2	**SIGNAL**

CN3：+12V Power Connector(8Pin)



Pin	Define	Pin	Define
1	Ground	5	+12V
2	Ground	6	+12V
3	Ground	7	+12V
4	Ground	8	+12V

CN4: ATX Power Connector

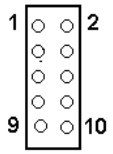


Pin	Define	Pin	Define
11	+3.3V	1	+3.3V
12	-12V	2	+3.3V
13	Ground	3	Ground
14	PS_ON*	4	+5V
15	Ground	5	Ground
16	Ground	6	+5V
17	Ground	7	Ground
18	RSVD	8	POWER GOOD
19	+5V	9	5VSB
20	+5V	10	+12V

CN5: GPI Pin Header

Pin	Define
1	GPI0
2	GPI1
3	GPI2
4	GPI3
5	Ground

CN6 : GPO Pin Header

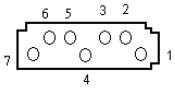


Pin	Define	Pin	Define
1	GPO4-	2	GPO4+
3	GPO5-	4	GPO5+
5	GPO6-	6	GPO6+
7	GPO7-	8	GPO7+
9	NC	10	NC

CN7 : Reset Pin Header

Pin	Define
1	Ground
2	Reset #

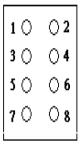
CN8/CN9/CN10/CN11: SATA Connector



Pin	Define
1	GND
2	TXP
3	TXN
4	GND

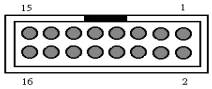
5	RXN
6	RXP
7	GND

CN13: SPI (reserved for manufactory test)



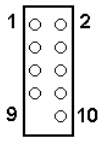
Pin	Define	Pin	Define
1	VCC3	2	GND
3	SPI_CS0	4	SPI_CLK
5	SPI_MISO	6	SPI_MOSI
7	NC	8	FLASH_IO

CN14: VGA Pin Header (No function for some Xeon E3-1200 series CPUs)



Pin	Define	Pin	Define
1	RED	2	GREEN
3	BLUE	4	+5V
5	Ground	6	Ground
7	Ground	8	Ground
9	+5V	10	Ground
11	+5V	12	SDA
13	HSYNC	14	VSYNC
15	SCL	16	NC

CN16: USB2/3 Pin Header



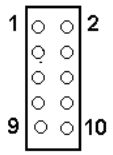
Pin	Define	Pin	Define
1	+5V	2	+5V
3	DATA 0-	4	DATA 1-
5	DATA 0+	6	DATA 1+
7	GND	8	GND
9	KEY PIN	10	GND

CN17: PCIE x8 Slot (proprietary)

Pin	Define	Pin	Define
A1	GND	B1	+12V
A2	+12V	B2	+12V
A3	+12V	B3	+12V
A4	GND	B4	GND
A5	VCC3	B5	SMB_CLK_ RESUME
A6	VCC3	B6	SMB_DATA_ RESUME
A7	GND	B7	GND
A8	VCC3	B8	VCC3
A9	VCC3	B9	NC
A10	VCC3	B10	VCC3_STBY
A11	RESET	B11	PE_WAKE
A12	GND	B12	LAN_PWRO K
A13	PCI_E3_P2	B13	GND
A14	PCI_E3_N2	B14	TX_0_DP

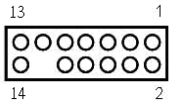
A15	GND	B15	TX_0_DN
A16	RX_0_DP	B16	GND
A17	RX_0_DN	B17	VCC5
A18	GND	B18	GND
A19	VCC5	B19	TX_1_DP
A20	GND	B20	TX_1_DN
A21	RX_1_DP	B21	GND
A22	RX_1_DN	B22	GND
A23	GND	B23	TX_2_DP
A24	GND	B24	TX_2_DN
A25	RX_2_DP	B25	GND
A26	RX_2_DN	B26	GND
A27	GND	B27	TX_3_DP
A28	GND	B28	TX_3_DN
A29	RX_3_DP	B29	GND
A30	RX_3_DN	B30	BYPASS
A31	GND	B31	GPIO35
A32	GPIO33	B32	GND
A33	GND	B33	TX_4_DP
A34	GND	B34	TX_4_DN
A35	RX_4_DP	B35	GND
A36	RX_4_DN	B36	GND
A37	GND	B37	TX_5_DP
A38	GND	B38	TX_5_DN
A39	RX_5_DP	B39	GND
A40	RX_5_DN	B40	GND
A41	GND	B41	TX_6_DP
A42	GND	B42	TX_6_DN
A43	RX_6_DP	B43	GND
A44	RX_6_DN	B44	GND
A45	GND	B45	TX_7_DP
A46	GND	B46	TX_7_DN
A47	RX_7_DP	B47	GND
A48	RX_7_DN	B48	NC
A49	GND	B49	GND

CN18: KB/MS Pin Header



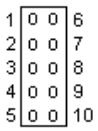
Pin	Define	Pin	Define
1	KCLK	2	MCLK
3	KDAT	4	MDAT
5	NC	6	NC
7	PS2_GND	8	PS2_GND
9	PS2_VCC	10	PS2_VCC

CN21: LPC Connector



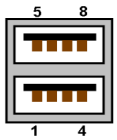
Pin	Define	Pin	Define
1	+3.3V	2	AD 0
3	AD 1	4	AD 2
5	AD 3	6	Frame#
7	PCIERST#	8	+5V
9	CLOCK	10	PME#
11	GND	12	
13	SERIRQ	14	LDRQ

CN22 :COM2 Box Header



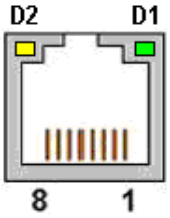
Pin	Define	Pin	Define
1	DCD#	6	DSR#
2	RXD#	7	RTS#
3	TXD#	8	CTS#
4	DTR#	9	RI#
5	Ground	10	NC

CN23: USB0/1 Connector



Pin	Define
1	5VUSB0
2	USBDT0-
3	USBDT0+
4	Ground
5	5VUSB0
6	USBDT1-
7	USBDT1+
8	Ground

CN24/CN25/CN26/CN27/CN28/CN29/CN30: Giga LAN RJ45 connector



Pin	Define
1	MDI0+
2	MDI0-
3	MDI1+
4	MDI2+
5	MDI2-
6	MDI1-
7	MDI3+
8	MDI3-

LED:

D2 : Link/Activity LED	
Link	Green
Activity	Blinking
D1 : Bi-Color Speed LED	
10 Mbps	Off
100 Mbps	Green
1000Mbps	Yellow

CN31: COM1 RJ45 Connector

Pin	Define(STD)
1	CTS#
2	DTR#
3	TXD#
4	GND
5	Ground
6	RXD#
7	DSR#
8	RTS#

CN33: PCI-E x8 Golden Finger

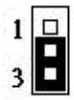
Pin	Define	Pin	Define
A1	GND	B1	+12V
A2	+12V	B2	+12V
A3	+12V	B3	+12V
A4	GND	B4	GND
A5	VCC3	B5	SMB_CLK_RESUME
A6	VCC3	B6	SMB_DATA_RESUME
A7	VCC3	B7	GND
A8	VCC3	B8	VCC3
A9	VCC3	B9	NC
A10	VCC3	B10	VCC3_STBY
A11	RESET	B11	PE_WAKE
A12	GND	B12	LAN_PWROK
A13	PCI_E4_P1	B13	GND
A14	PCI_E4_N1	B14	TX_0_DP
A15	GND	B15	TX_0_DN
A16	RX_0_DP	B16	GND
A17	RX_0_DN	B17	VCC5
A18	GND	B18	GND
A19	VCC5	B19	TX_1_DP
A20	GND	B20	TX_1_DN
A21	RX_1_DP	B21	GND
A22	RX_1_DN	B22	GND
A23	GND	B23	TX_2_DP
A24	GND	B24	TX_2_DN
A25	RX_2_DP	B25	GND
A26	RX_2_DN	B26	GND
A27	GND	B27	TX_3_DP
A28	GND	B28	TX_3_DN

A29	RX_3_DP	B29	GND
A30	RX_3_DN	B30	BYPASS
A31	GND	B31	GPIO27
A32	GPIO34	B32	GND
A33	GND	B33	TX_4_DP
A34	GND	B34	TX_4_DN
A35	RX_4_DP	B35	GND
A36	RX_4_DN	B36	GND
A37	GND	B37	TX_5_DP
A38	GND	B38	TX_5_DN
A39	RX_5_DP	B39	GND
A40	RX_5_DN	B40	GND
A41	GND	B41	TX_6_DP
A42	GND	B42	TX_6_DN
A43	RX_6_DP	B43	GND
A44	RX_6_DN	B44	GND
A45	GND	B45	TX_7_DP
A46	GND	B46	TX_7_DN
A47	RX_7_DP	B47	GND
A48	RX_7_DN	B48	GPIO28
A49	PCIE_SLOT0_1_SEL	B49	GND

JP3: Power On Type Control

Pin		Setting
	1-2	Control by POSN# (Default)
	2-3	Force On

JP4: Watchdog or Bypass Select

Pin		Setting
	1-2	Reset (Default)
	2-3	LAN Bypass

JP5,JP7 : PCI-E Golden Finger +5V / PCI-E SLOT +5V

	
1-2	+5V IN

JP6: Clear CMOS

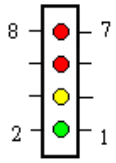
Pin		Setting
	1-2	Normal(Default)
	2-3	Clear CMOS

JP8/JP9: LAN5 & LAN6 Bypass

Pin		Setting
	1-2	Normal (Default)

	2-3	Bypass Always Disable

LED2: Front LEDs

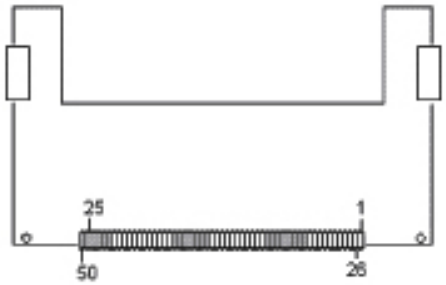


Pin	Define	Pin	Define
1	GND	2	Power_LED+
3	HDD LED-	4	HDD LED+
5	BYPASS LED-	6	BYPASS_LED+
7	BYPASS LED-	8	BYPASS_LED+

2.3 CompactFlashTM Card Socket Pin Definitions

CompactFlash™ card is a small removable mass storage device. It can provide complete PCMCIA-ATA functionality and compatibility plus True IDE functionality compatible with ATA/ATAPI-4.
CompactFlash™ storage products are solid state form factor, it means they contain no moving parts. Thus, it provides users with much greater protection of the data than conventional magnetic disk device.

Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment
1	Ground	11	Ground	21	D00	31	D15	41	RESET
2	D03	12	Ground	22	D01	32	CS	42	ORDY
3	D04	13	VCC	23	D02	33	NC	43	DREG
4	D05	14	Ground	24	WP	34	IOR	44	DACK
5	D06	15	Ground	25	NC	35	IOW	45	LED
6	D07	16	Ground	26	NC	36	WE	46	BVD
7	CS	17	Ground	27	D11	37	RDY/BSY	47	D08
8	Ground	18	A02	28	D12	38	VCC	48	D09
9	Ground	19	A01	29	D13	39	SCSE	49	D10
10	Ground	20	A00	30	D14	40	NC	50	Ground



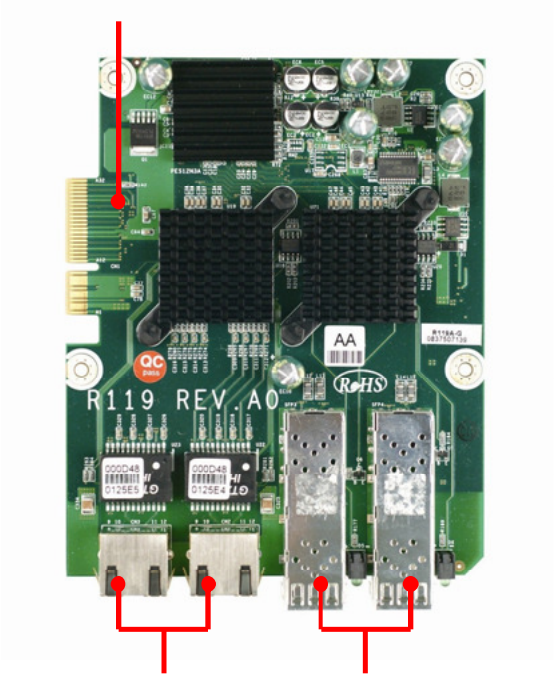
Chapter 3. Optional GbE Module & Riser Card Setting

The PL-80310 can offer various GbE module combinations to match various applications and market demand.

3.1 R119: Ethernet module with two GbE Copper and two GbE SFP

R119A is a two GbE Copper and two GbE SFP Ethernet module. The golden edge fingers to be connected with CN17 proprietary connector of PL-80310 board.

Golden Edge Fingers to be connected with CN17
of MB-80310. (or PCI-E x8 slot of R117A)

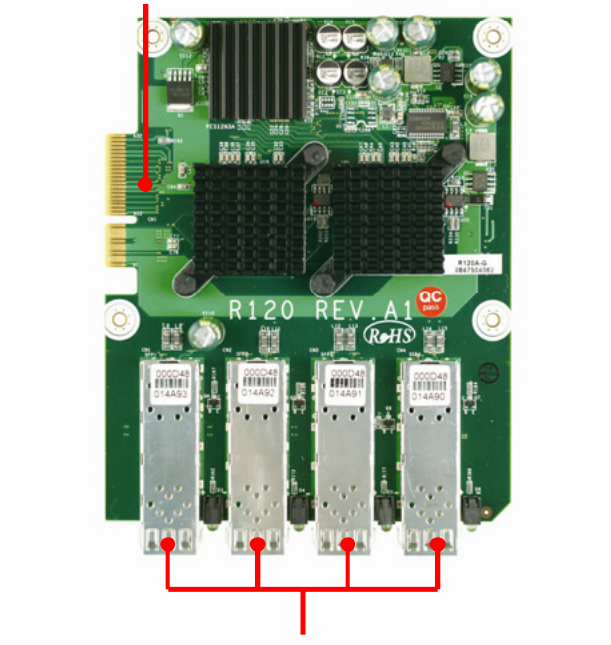


2 x GbE Copper ports 2 x GbE SFP ports

3.2 R120: Ethernet module with four GbE SFP

R120A is a four GbE SFP Ethernet module. The golden edge fingers to be connected with CN17 proprietary connector of PL-80310 board.

Golden Edge Fingers to be connected with CN17
of MB-80310. (or PCI-E x8 slot of R117A)

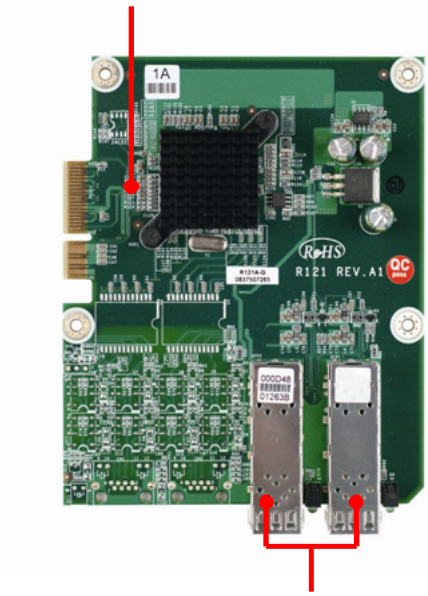


4 x GbE SFP ports

3.3 R121: Ethernet module with two GbE Copper or SFP

R121B is a two GbE Copper Ethernet module and designed reserved one pair bypass function for optional (ODM project). The golden edge fingers must be connected with CN17 proprietary connector of CB-8970 board. The alternative R121A is a two GbE SFP Ethernet module.

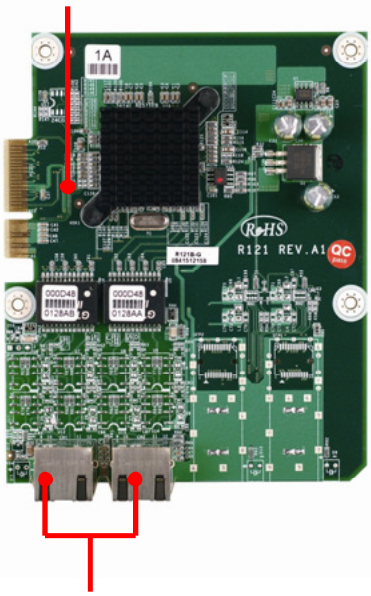
Golden Edge Fingers to be connected with CN17 of MB-80310. (or PCI-E x8 slot of R117A)



2 x GbE SFP ports

Picture-1: R121A

Golden Edge Fingers to be connected with CN17 of MB-80310. (or PCI-E x8 slot of R117A)



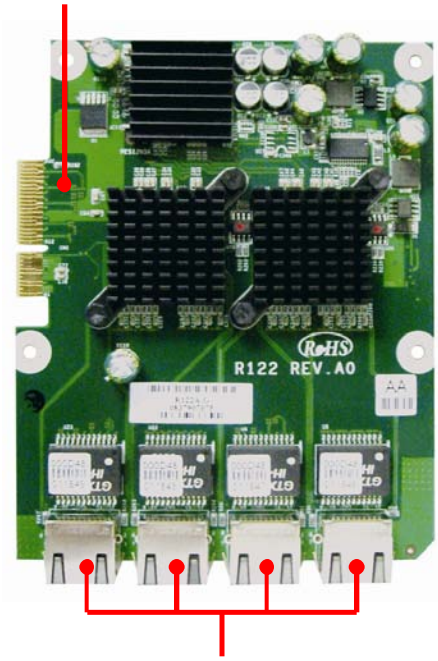
2 x GbE Copper ports

Picture-2: R121B

3.4 R122: Ethernet module with four GbE Copper

R122A is a four GbE Copper Ethernet module. The golden edge fingers to be connected with CN17 proprietary connector of PL-80310 board.

Golden Edge Fingers to be connected with CN17 of MB-80310. (or PCI-E x8 slot of R117A)



4 x GbE Copper ports

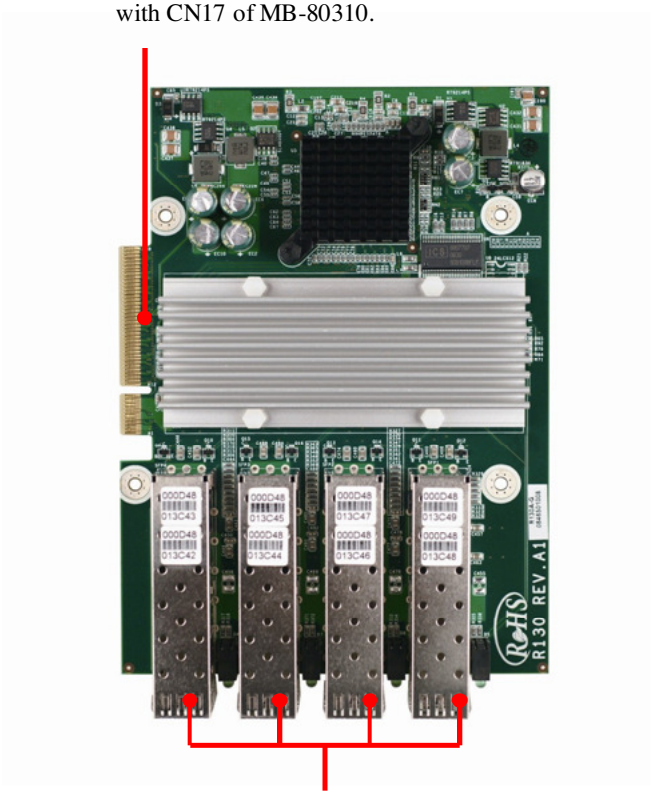
3.5 R127: Ethernet module with eight GbE Copper

R127A is a four GbE Copper Ethernet module. The golden edge fingers to be connected with CN17 proprietary connector of PL-80310 board.

3.6 R130: Ethernet module with eight GbE SFP

R130A is a four GbE Copper Ethernet module. The golden edge fingers to be connected with CN17 proprietary connector of PL-80310 board.

Golden Edge Fingers to be connected with CN17 of MB-80310.

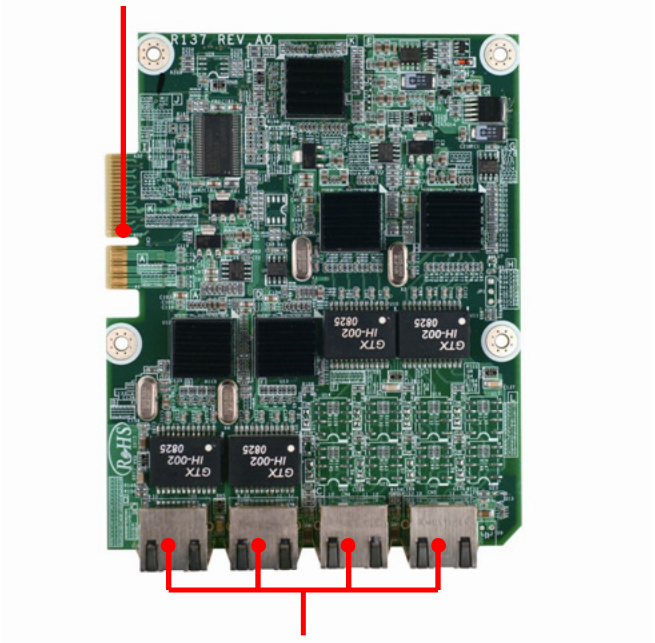


8 x GbE SFP ports

3.7 R137: Ethernet module with four GbE Copper

R137A is a four GbE Copper module and designed reserved one pair bypass function for optional (ODM project). The golden edge fingers must be connected with CN17 proprietary connector of PL-80310 board.

Golden Edge Fingers to be connected with CN17
of MB-80310. (or PCI-E x8 slot of R117A)

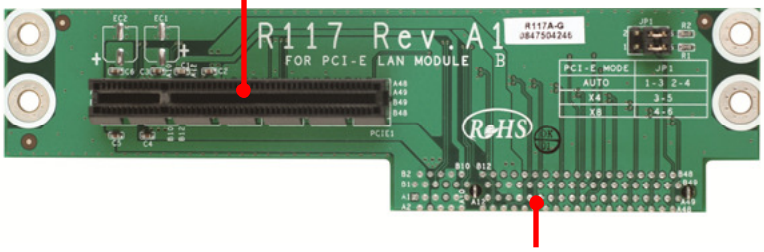


4 x GbE Copper ports

3.8 R117: Riser card for expansion module PCI-E x8

R117A is one PCI-E x8 to PCI-E x8(proprietary) riser card for expansion Ethernet module. It must be connected to CN32(PCI-E x8 Golden Finger) of PL-80310 appliance.

PCI-E x8 slot to proprietary Ethernet module

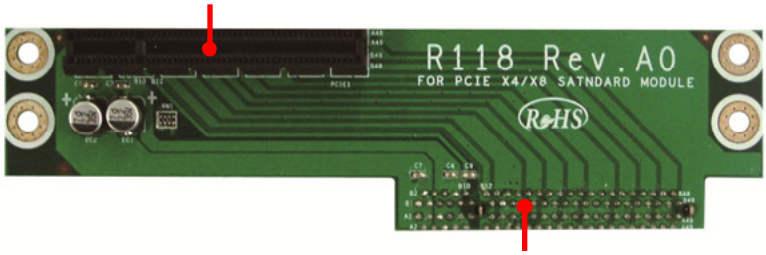


PCI-E x8 slot to be Golden Edge Fingers of MB-80310

3.9 R118: Riser card for PCI-E x8 add-on card

R118A is one PCI-E x8 to PCI-E x8 riser card for standard PCI-E x8/x4/x1 add-on card. It must be connected to CN32(PCI-E x8 Golden Finger) of PL-80310 appliance.

PCI-E x8 slot to standard Add-on card

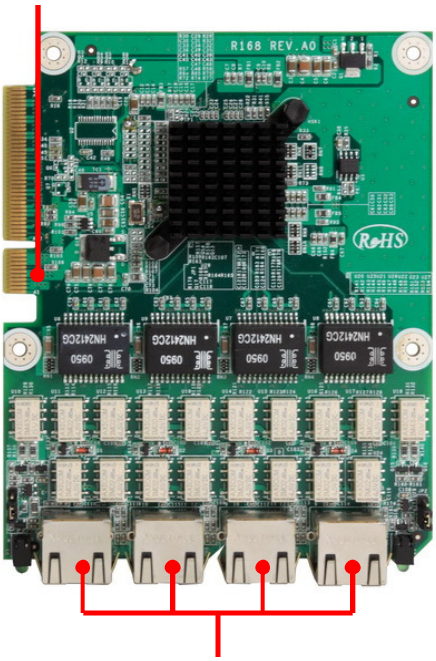


PCI-E x8 slot to be Golden Edge Fingers of MB-80310

3.10 R168: Ethernet module with four GbE Copper and bypass

R168 is a four GbE Copper Ethernet module with bypass. The golden edge fingers must be connected with CN17 proprietary connector of PL-80310 board.

Golden Edge Fingers must be connected with CN17 of MB-80310.

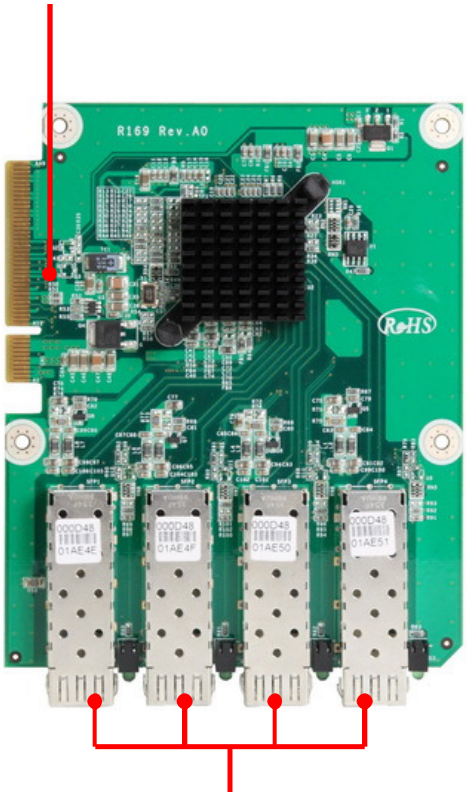


4 x GbE Copper ports

3.11 R169: Ethernet module with four GbE SFP

R168 is a four GbE SFP Ethernet module. The golden edge fingers must be connected with CN17 proprietary connector of PL-80310 board.

Golden Edge Fingers must be connected with CN17 of MB-80310.

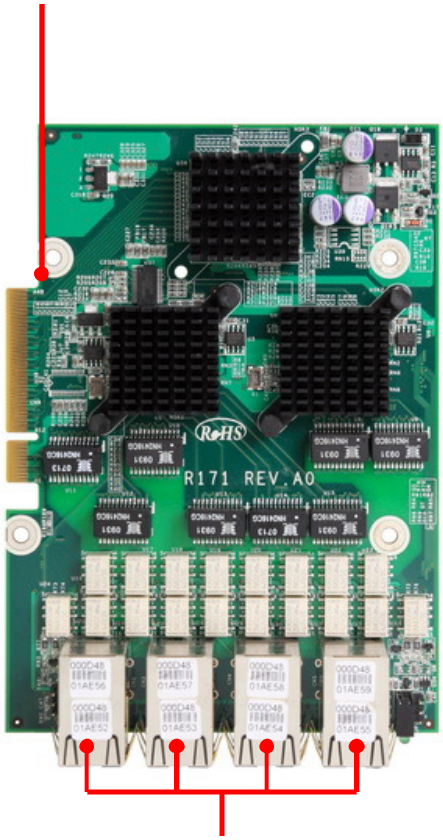


4 x GbE SFP ports

3.12 R171: Ethernet module with eight GbE Copper

R168 is an eight GbE Copper Ethernet module. The golden edge fingers must be connected with CN17 proprietary connector of PL-80310 board.

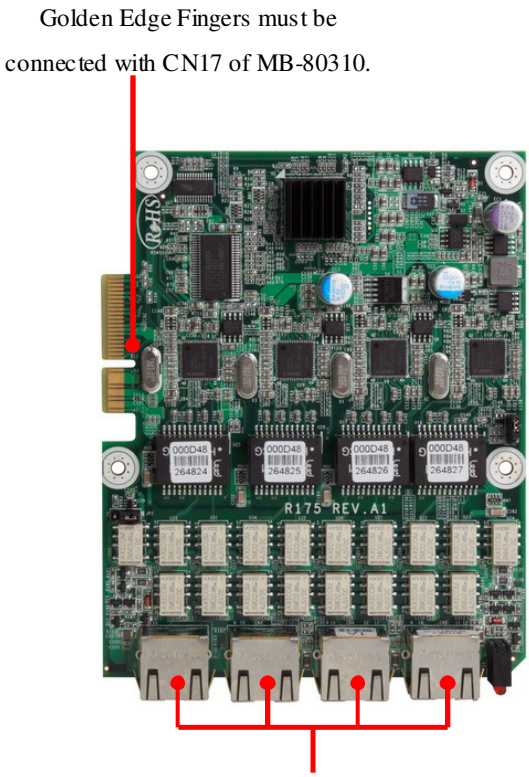
Golden Edge Fingers must be connected with CN17 of MB-80310.



8 x GbE Copper ports

3.13 R175: Ethernet module with four GbE Copper and bypass

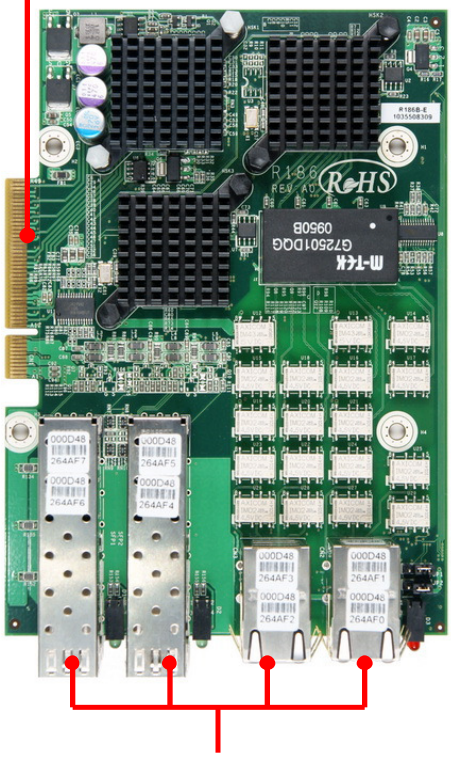
R175 is a four GbE Copper Ethernet module with bypass. The golden edge fingers must be connected with CN17 proprietary connector of PL-80310 board.



3.14 R186: Ethernet module with four GbE Copper & four GbE SFP

R186 is a four GbE Copper and four GbE SFP Ethernet module with bypass. The golden edge fingers must be connected with CN17 proprietary connector of PL-80310 board.

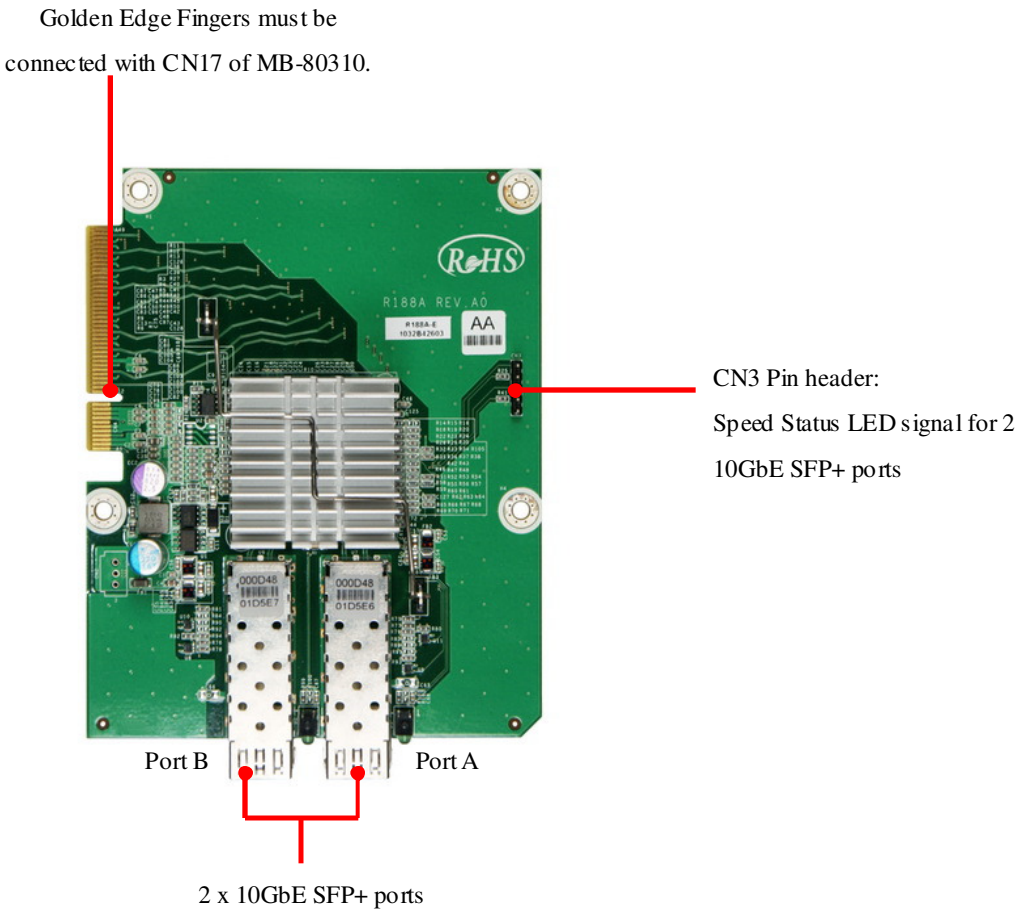
Golden Edge Fingers must be connected with CN17 of MB-80310.



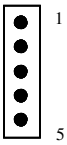
4 x GbE Copper &
4 x GbE SFP ports

3.15 R188: Ethernet module with two 10GbE SFP+

R188 is a two 10GbE SFP+ Ethernet module. The golden edge fingers must be connected with CN17 proprietary connector of PL-80310 board.



CN3 Pin header:



Pin	Define
1	10G Speed Status (+) for Port A
2	1G Speed Status (+) for Port A
3	10G Speed Status (+) for Port B
4	1G Speed Status (+) for Port B
5	Ground

Chapter 4. BIOS Setup

The ROM chip of your PL-80310 board is configured with a customized Basic Input/Output System (BIOS) from AMI BIOS. The BIOS is a set of permanently recorded program routines that give the system its fundamental operational characteristics. It also tests the computer and determines how the computer reacts to instructions that are part of programs.

The BIOS is made up of code and programs that provide the device-level control for the major I/O devices in the system. It contains a set of routines (called POST, for Power-On Self Test) that check out the system when you turn it on. The BIOS also includes BIOS setup program, so no disk-based setup program is required CMOS RAM stores information for:

- Date and time
- Memory capacity of the appliance
- Type of display adapter installed
- Number and type of disk drives

The CMOS memory is maintained by battery installed on the PL-80310 board. By using the battery, all memory in CMOS can be retained when the system power switch is turned off. The system BIOS also supports easy way to reload the CMOS data when you replace the battery of the battery power lose.

4.1 Quick Setup

In most cases, you can quickly configure the system by choosing the following main menu options:

1. Choose "Exit" ➔ "Load Optimal Defaults" from the main menu. This loads the setup default values from the BIOS Features Setup and Chipset Features Setup screens.
2. Choose "Main" & "Advanced" from the main menu. This option lets you configure the date and time, hard disk type, floppy disk drive type, primary display and more.
3. In the main menu, press F4 ("Save and Exit") to save your changes and reboot the system.

4.2 Entering the BIOS Setup Utility

Use the BIOS setup program to modify the system parameters to reflect the options installed in your system and to customize your system. For example, you should run the Setup program after you:

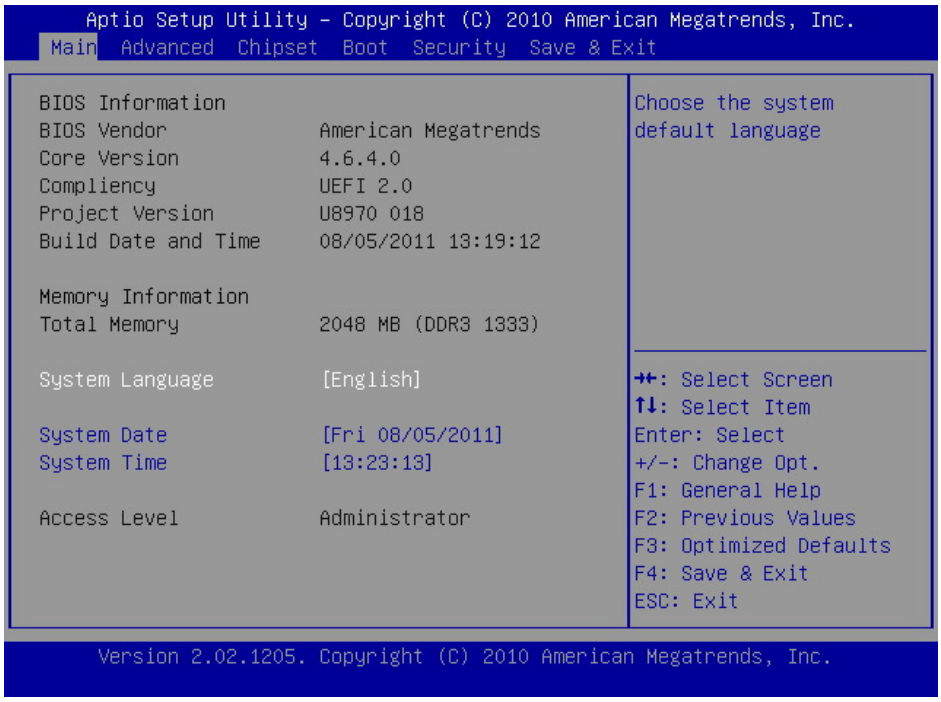
- Received an error code at startup
- Install another disk drive
- Use your system after not having used it for a long time
- Find the original setup missing
- Replace the battery
- Change to a different type of CPU
- Run the AMI Flash program to update the system BIOS

Run the BIOS setup program after you turn on the system. On-screen instructions explain how to use the program.

⇩ **Enter the BIOS setup program's main menu as follows:**

1. Turn on or reboot the system. After the BIOS performs a series of diagnostic checks, the following message appears:
   "Press DEL to enter SETUP"

2. Press the <DEL> key to enter BIOS setup utility. The main menu appears:



3. Choose a setup option with the arrow keys and press <Enter>. See the following sections for a brief description of each setup option.

BIOS Information: Displays the BIOS related information.

Memory Information: Displays the total memory size.

System Language: Change the language display in BIOS setup utility.

System Date [Day mm/dd/yyyy]:
This item allows you to set the system date.

SystemTime: [hour:min:sec]:
This item allows you to set the system time.

In the main menu, press F4 ("Save and Exit") to save your changes and reboot the system. Press F3("Optimized Defaults") to load the Optimal

default configuration values of the menu. Pressing <ESC> anywhere in the program returns you to the main menu.

4.3 Menu Options

The main menu options of the BIOS setup program are described in the following and the following sections of this chapter.

Main: For changing the basic system configurations.

Advanced: For changing the advanced system settings.

Chipset: For customize the Intel chipset function

Boot: For changing the system boot configurations.

Security: For setting User and Supervisor Passwords.

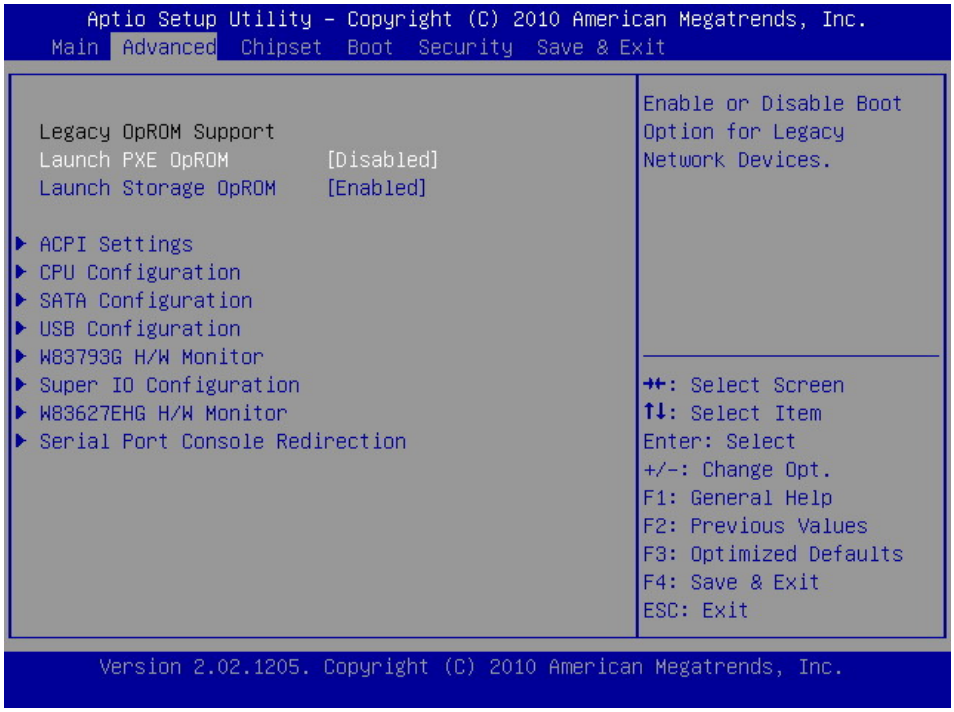
Exit: For selecting the exit options and loading default settings.

4.4 Advanced Menu

The Advanced menu items allow you to change the settings for the CPU and other system devices.

⇩Use the Advanced Setup option as follows:

1. Choose "Advanced" from the main menu. The following screen appears:



2. Use the arrow keys to move between fields. Modify the selected field using the PgUP/PgDN/+/- keys. Some fields let you enter numeric values directly.

3. After you have finished with the Advanced setup, press the <←> or <→> key to switch to other setup menu or press <F4> key to save setting.

Launch PXE OpROM: [Disabled]

Enables or disables the PXE (Preboot Execution Environment) function. The PXE will be performed on Lan 1 port (CN24, refer to the Chapter 1.7) when enable.

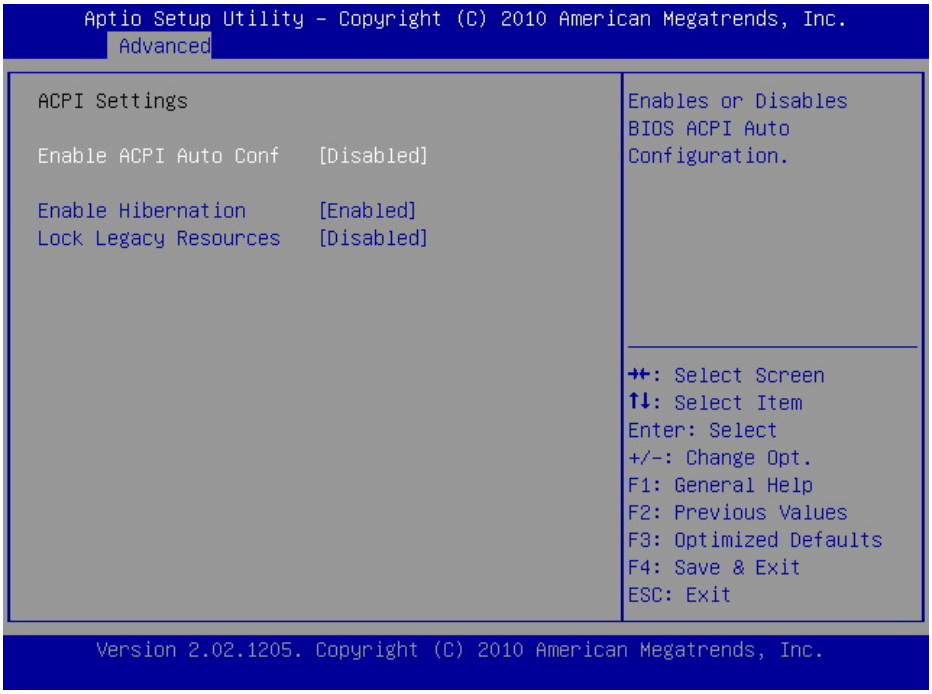
Launch Storage OpROM: [Enabled]

Use this setting to specify that legacy PCI option ROMs for PCI storage devices are to

be loaded and executed, if found. Typical examples of PCI storage devices include SCSI or similar devices.

4.4.1 ACPI Settings

This sub menu allows you to set or change the ACPI settings in the system.



Enable ACPI Auto Configuration: [Disabled]

Enables or Disables BIOS ACPI Auto Configuration.

Enable Hibernation: [Enabled]

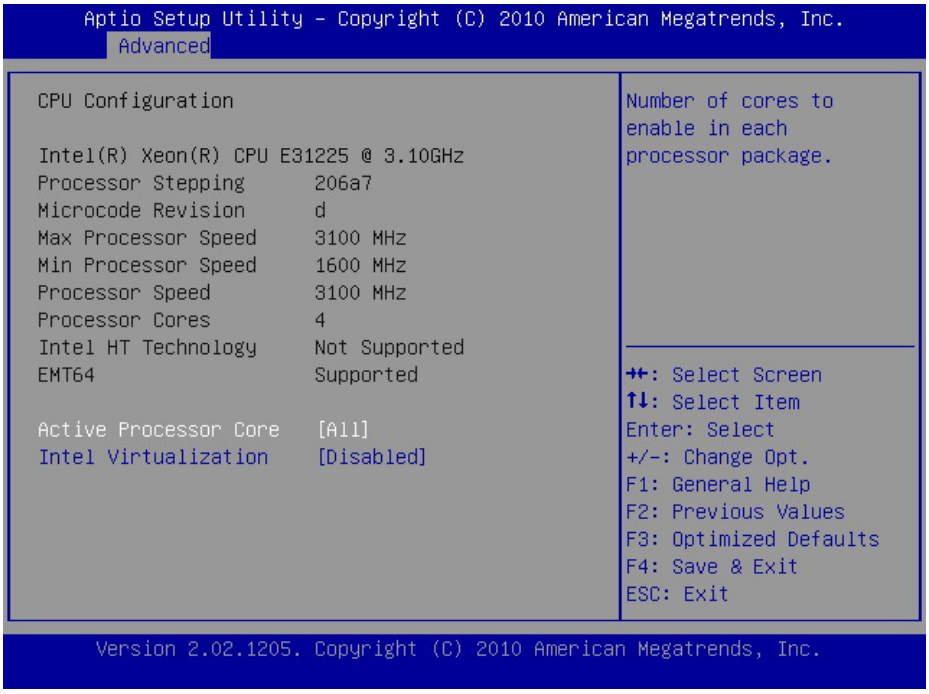
Enables or Disables Hibernation function.

Lock Legacy Resources: [Disabled]

The item allows you to lock legacy resources.

4.4.2 CPU Configuration

This sub menu shows the CPU related information which is automatically detected by BIOS and allows you to change the processor options.



Active Processor Cores: [All]

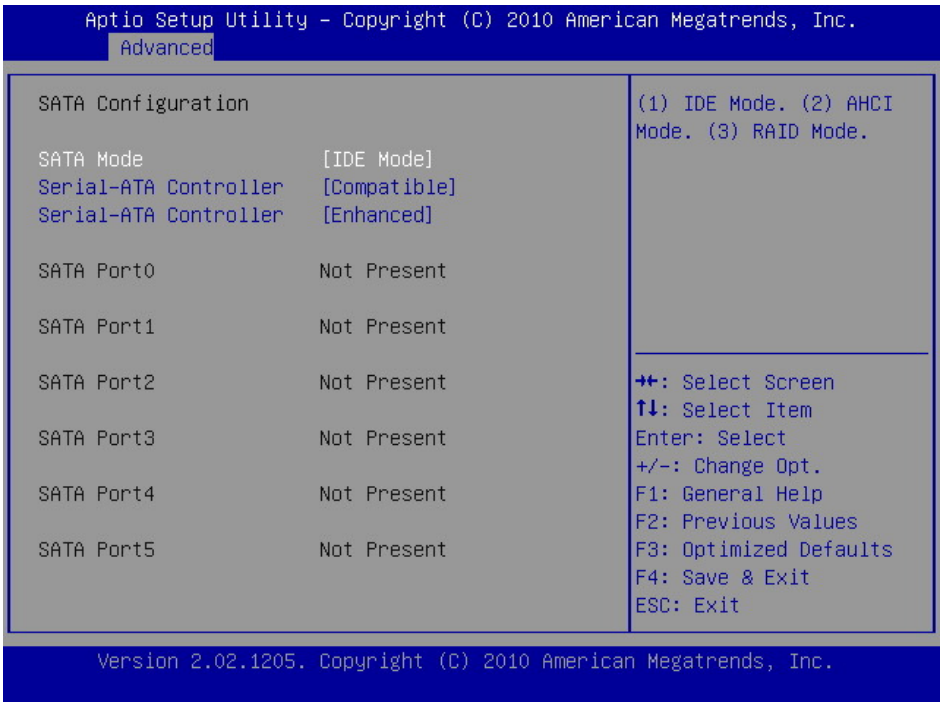
This item allows you to active all processor cores.

Intel(R) Virtualization: [Disabled]

This item allows you to enable or disable the Intel® Virtualization Technology.

4.4.2 SATA Configuration

This sub menu allows you to set or change the configurations for the SATA devices installed in the system.



SATA Mode: [IDE Mode]

This item allows you to configure the SATA mode. It has three options **[IDE Mode], [AHCI Mode] and [RAID Mode]; the default is [IDE Mode].**

Serial-ATA Controller 0: [Compatible]

This item allows you to configure the Serial-ATA Controller 0. It has two options **[Compatible] and [Enhanced]; the default is [Compatible].**

Serial-ATA Controller 1: [Enhanced]

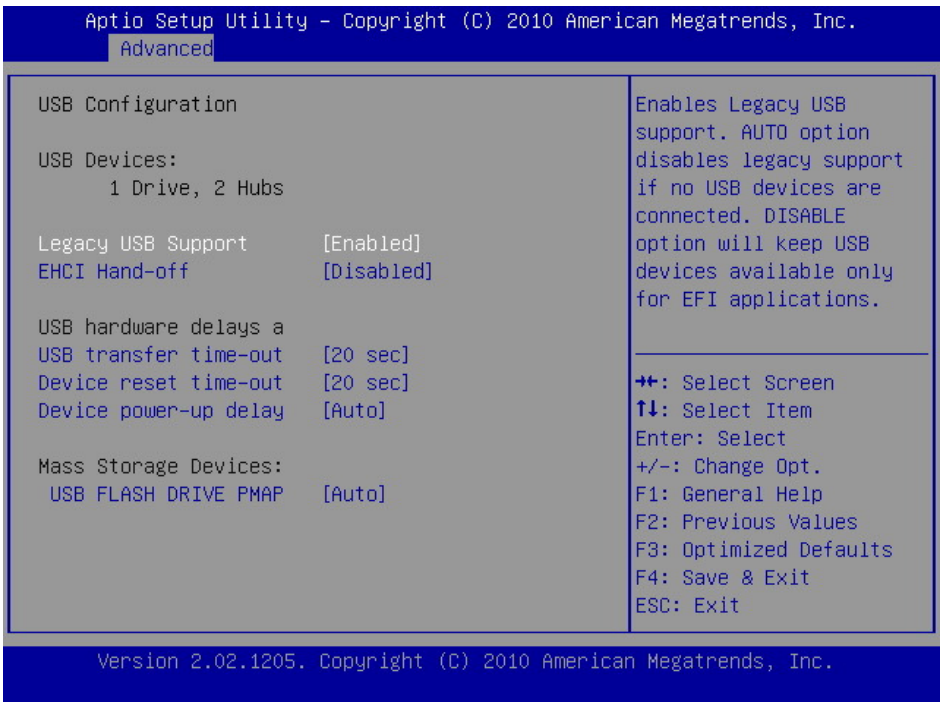
This item allows you to configure the Serial-ATA Controller 1. It has two options **[Compatible] and [Enhanced]; the default is [Enhanced].**

*** SATA Port0 ~ 5**

This information is auto-detected by BIOS and is not user-configurable. It will show "Not Present" if no IDE device is installed in the system.

4.4.4 USB Configuration

This sub menu allows you to set or change the configurations for the USB devices installed in the system.



Legacy USB Support: [Enabled]

Enables legacy USB support, Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI application.

EHCI Hand-off: [Disabled]

This item allows you to enable/disable the EHCI Hand-off function.

USB transfer time-out: [20 sec]

This item allows you to configure the USB transfer time-out.

Device reset time-out: [20 sec]

This item allows you to configure the Device reset time-out.

Device Power-up delay: [Auto]

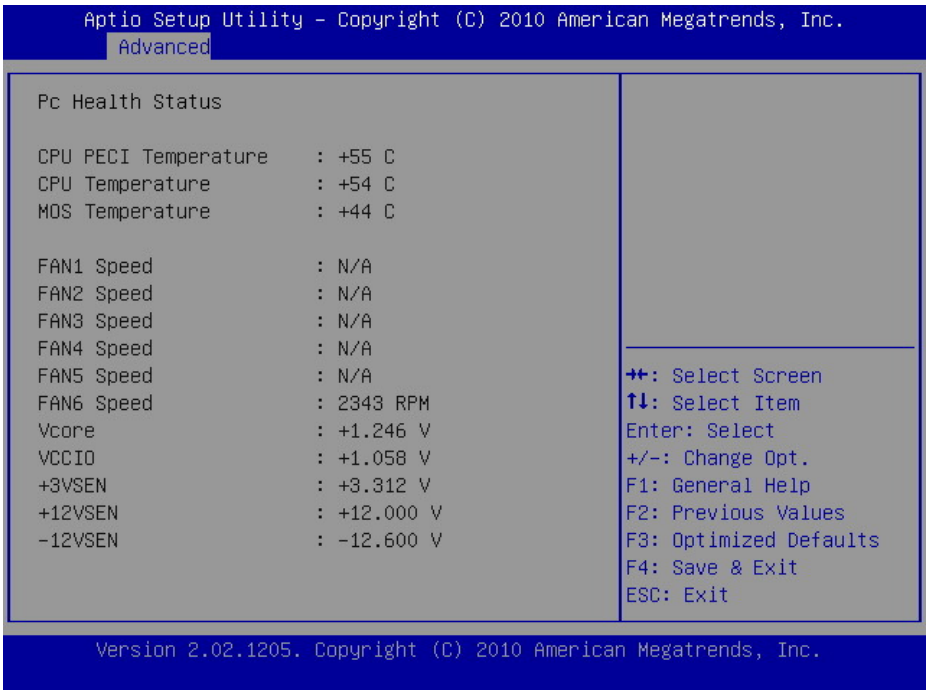
This item allows you to configure the maximum time the device will take before it properly reports itself to the host controller. The default is [Auto]; for a root port it is 100ms, for a Hub port the delay is taken from Hub description.

USB Flash Drive PMAP: [Auto]

This item only shows when plugging a USB flash device. User can choose [Auto], [Floppy], [Forced FDD], [Hard Disk] and [CD-ROM] to simulate USB flash device.

4.4.5 W83793G H/W Monitor / PC Health Status

This screen shows the CPU core voltage, System voltage, CPU temperature and FAN speed.

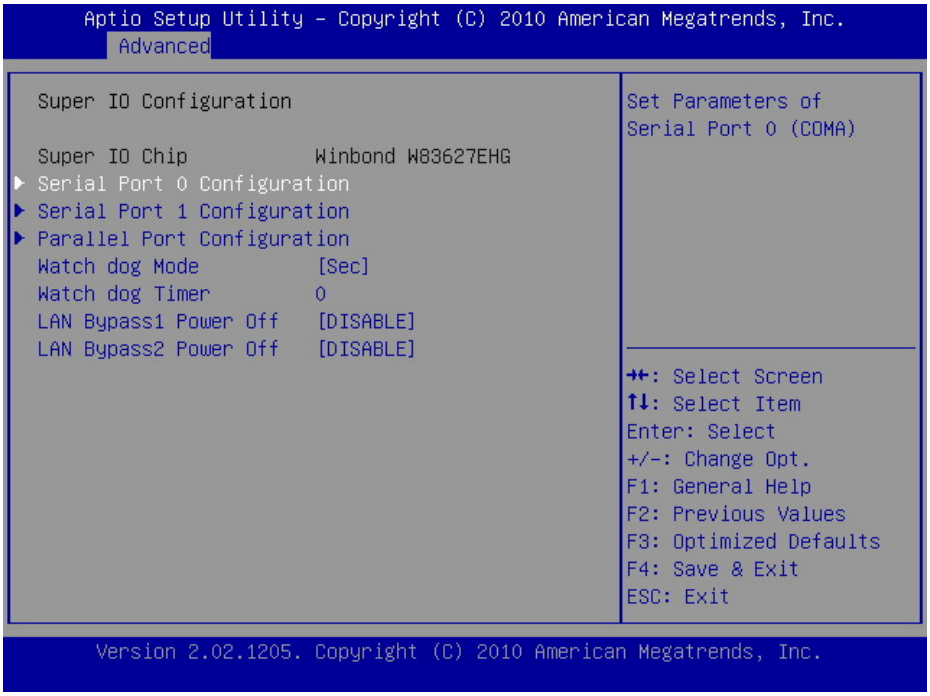


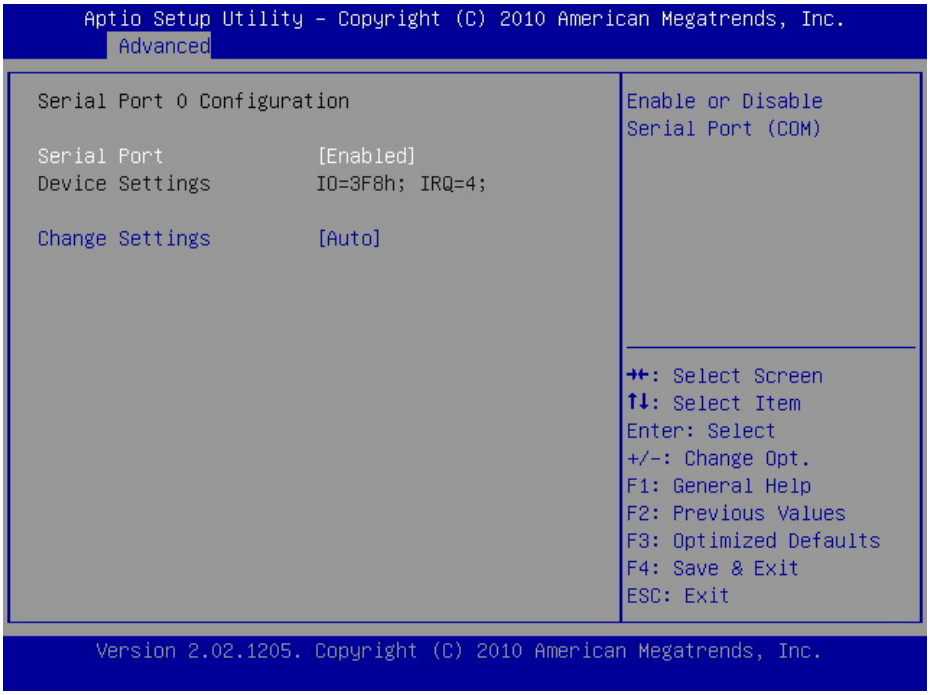
CPU PECI temperature:

CPU PECI Temperature shows the CPU T-junction temperature via PECI.

4.4.6 Super IO Configuration

This sub menu allows you to set or change the configurations for the Super I/O Configuration.





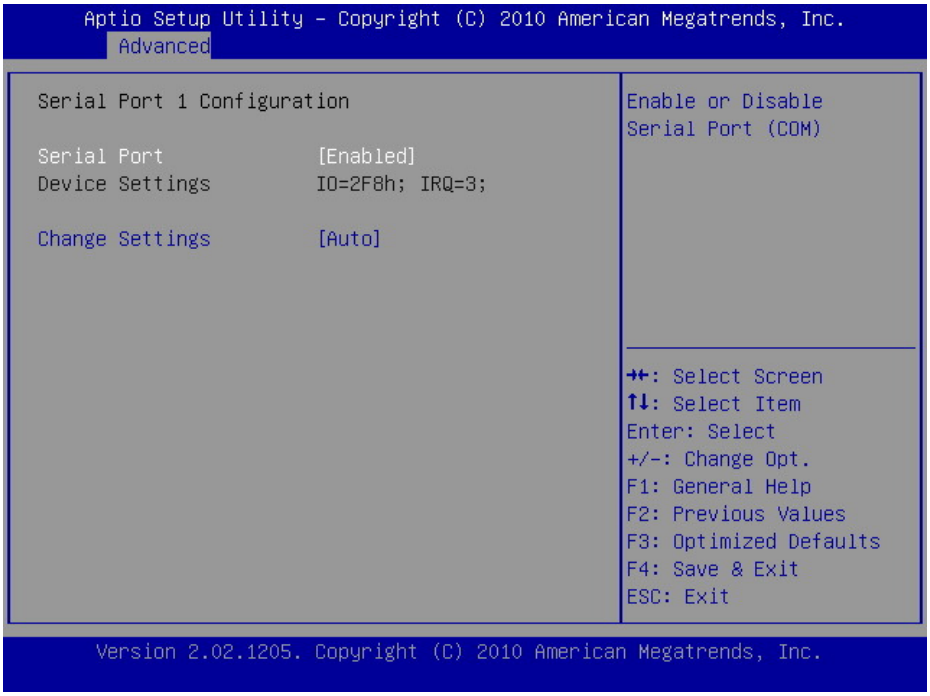
Serial Port 0 Configuration

Serial Port: [Enabled]

This item allows you to enable/disable the serial port 0.

Change Settings: [Auto]

Select optimal settings for serial port 0.



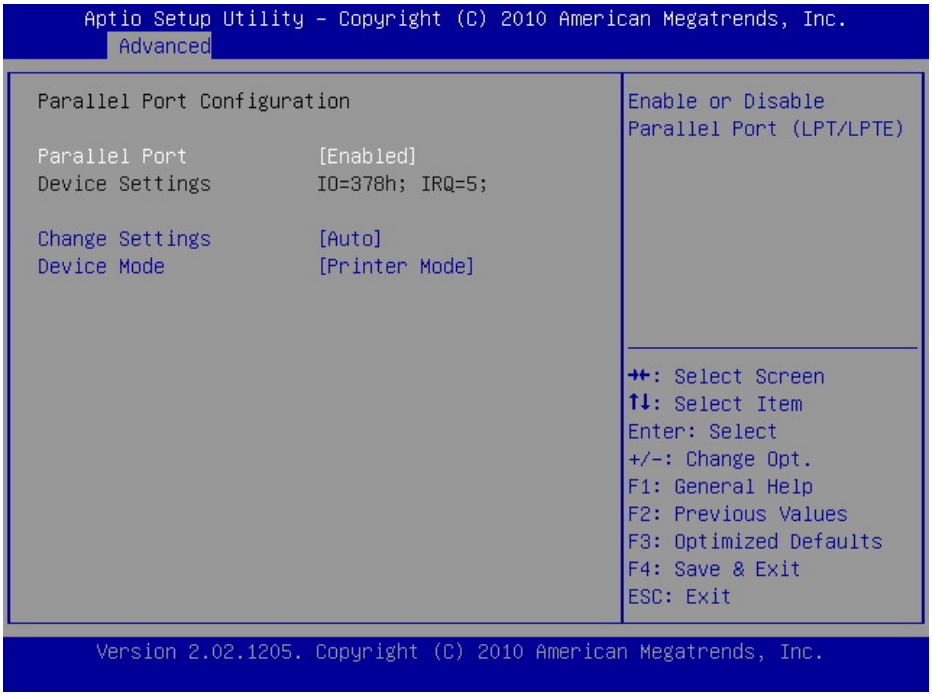
Serial Port 1 Configuration

Serial Port: [Enabled]

This item allows you to enable/disable the serial port 1.

Change Settings: [Auto]

Select optimal settings for serial port 1.



Parallel Port Configuration

Parallel Port: [Enabled]

This item allows you to enable/disable the Parallel Port.

Change Settings: [Auto]

Select optimal settings for parallel port.

Device Mode: [Printer Mode]

This item allows you to change the device mode of Parallel Port.

Watch Dog mode: [sec]

This item allows you to change the Watch Dog mode. **The default is [sec].**

Please refer to the Appendix A for Watchdog Timer Programming Guide if you want to control watchdog by OS.

Watchdog Timer:

This item allows you to set up the time for watchdog timer.

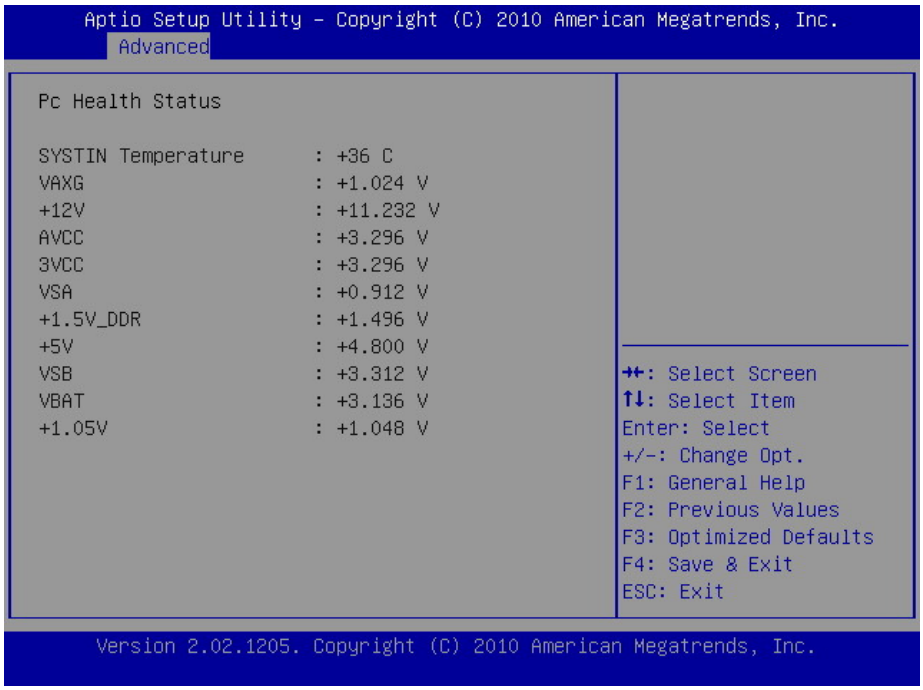
LAN Bypass1 Power off / LAN Bypass2 Power off: [Disable]

This item allows you to enable/disable the LAN Bypass1 or 2 when system power off.

Please refer to the Appendix B for LAN Bypass Programming Guide if you want to control LAN Bypass by OS when power on

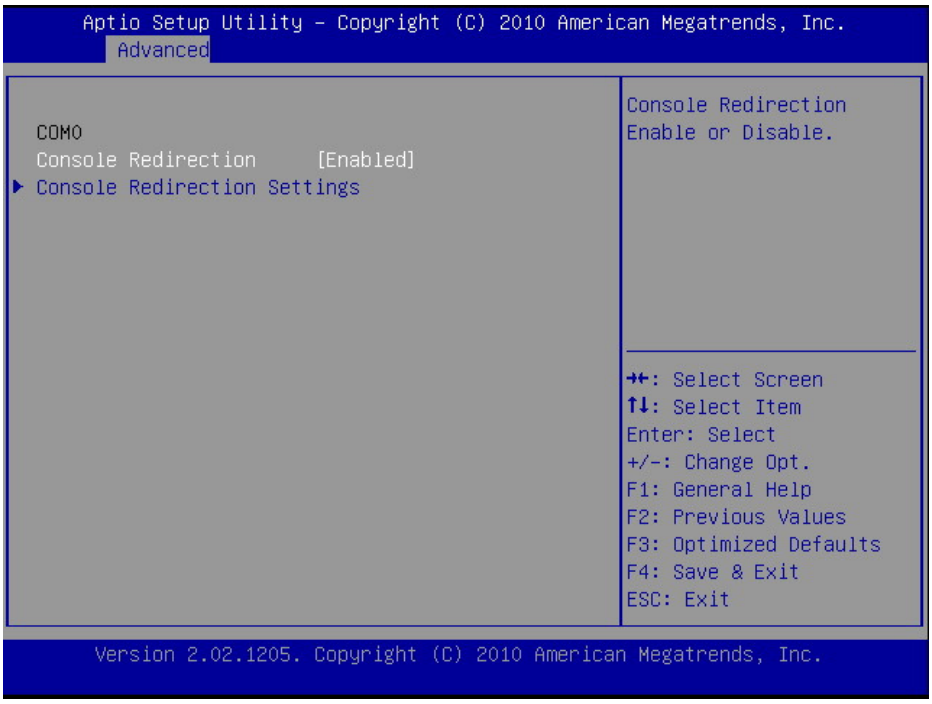
4.4.7 W83627EHG H/W Monitor

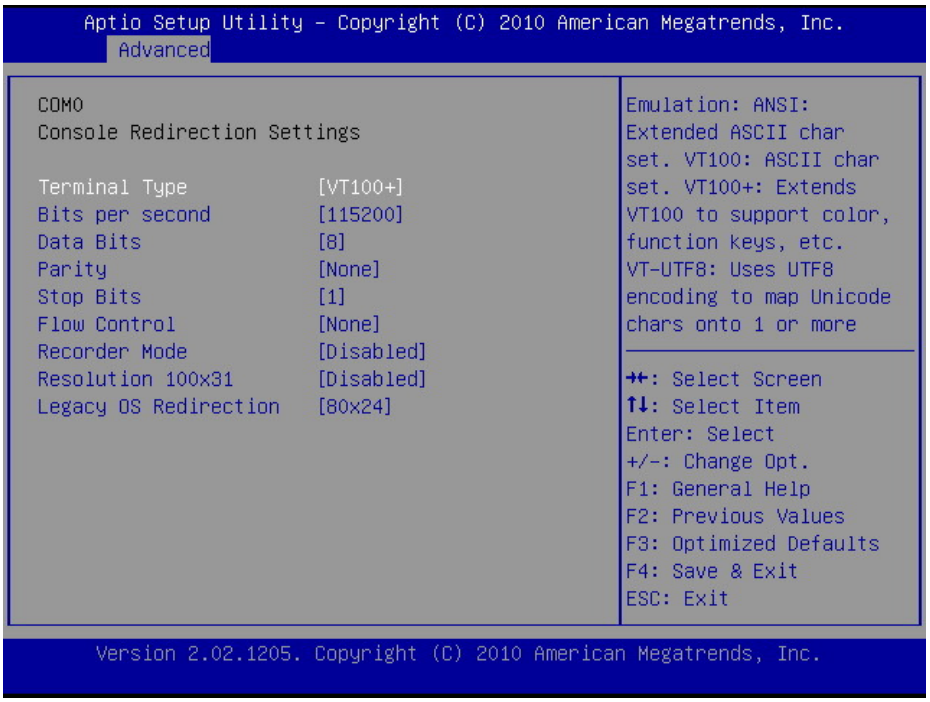
This screen shows the motherboard voltage and system temperature.



4.4.8 Serial Port Console Redirection

This sub menu allows you to change the setting of serial port console redirection.





Console Redirection: [Enabled]

This item allows you to enable/disable the console redirection feature.

Console Redirection Settings

Terminal Type: [VT100+]

This item allows you to select a terminal type to be used for console redirection.

Options available: VT100/VT100+/ANSI /VT-UTF8.

Bits per second: [115200]

This item allows you to select the baud rate for console redirection.

Options available: 9600/19200/57600/115200.

Data Bits: [8]

This item allows you to select the data bits for console redirection.

Options available: 5/6/7/8.

Parity: [None]

This item allows you to select the parity for console redirection.

A parity bit can be sent with the data bits to detect some transmission errors.

Even: parity bi is 0 if the num of 1's in the data bits is even.

Odd: parity bit is0if num of 1's the data bits is odd.

Mark: parity bit is always 1.

Space: Parity bit is always 0.

Mark and Space Parity do not allow for error detection.

Options available: None/Even/Odd/Mark/Space.

Stop Bits: [1]

This item allows you to select the stop bits for console redirection.

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Options available: 1/2.

Flow Control: [None]

This item allows you to select the flow control for console redirection.

Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

Options available: None/Hardware RTS/CTS.

Recorder Mode: [Disabled]

This item allows you to select the recorder mode for console redirection.

When this mode enabled, only text will be send. This is to capture Terminal data.

Options available: Enabled/Disabled.

Resolution 100x31: [Disabled]

This item allows you to select the resolution 100x31 for console redirection.

Enables or disables extended terminal resolution.

Options available: Enabled/Disabled.

Legacy OS Redirection: [80x24]

This item allows you to select the legacy OS redirection resolution for console redirection.

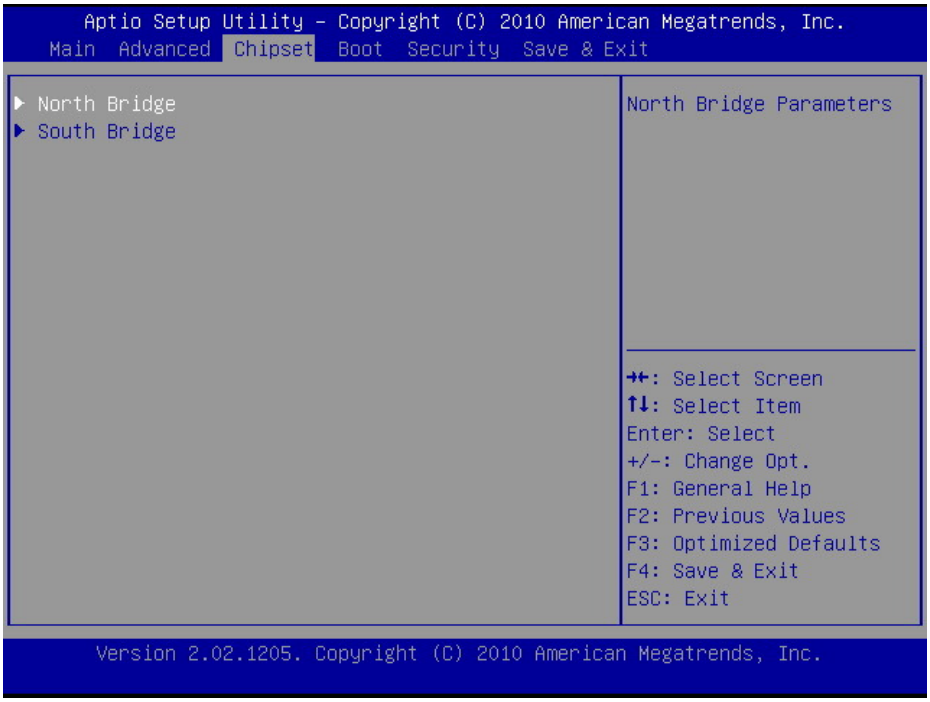
On Legacy OS, the number of Rows and Columns supported redirection.

Options available: 80x24/80X25.

4.5 Chipset Menu

⇩**Use the Chipset Setup option as follows:**

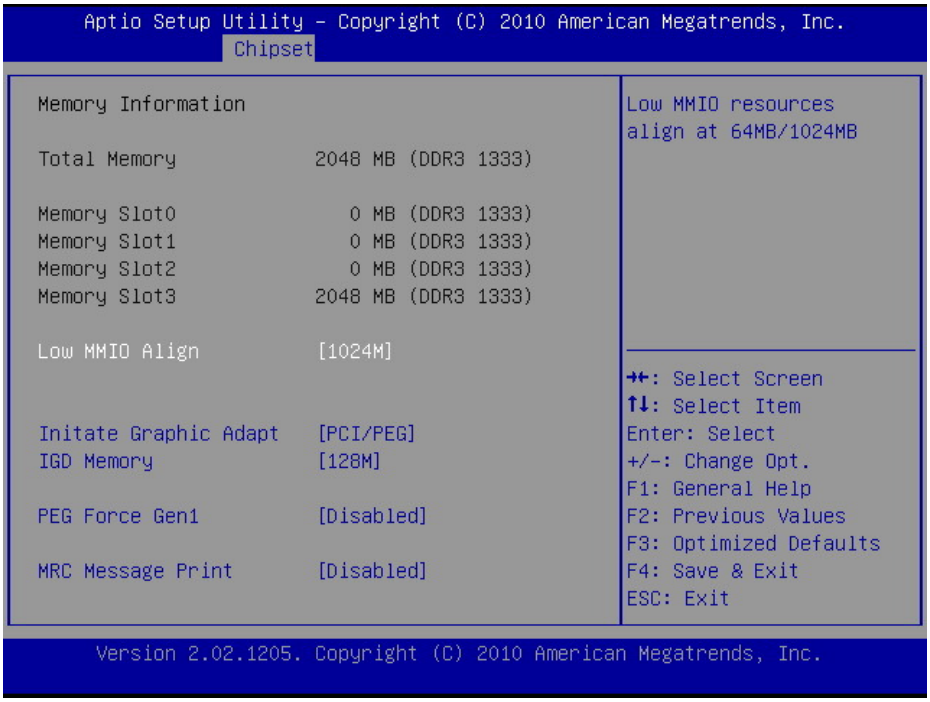
1. Choose "Chipset" from the main menu. The following screen appears.



2. Move between items and select values by using the arrow keys. Modify the selected field the PgUP/PgDN keys. For information on the various options, press <F1> key.

3. After you have finished with the Chipset Setup, press the <←> or <→> key to switch to other setup menu or press <F4> key to save setting.

4.5.1 North Bridge Chipset Configuration



Memory Information:

This item shows the memory related information which is automatically detected by BIOS.

Low MMIO Align: [1024MB]

This item allows you to configure the Low MMIO resources.

Options available: 64MB/1024MB.

Initiate Graphic Adapter: [PCI/PEG]

This item allows you to select which graphics controller to be the primary graphic device when booting up.

IGD Memory : [128M]

This item allows you to select the amount of system memory used by the internal graphics device.

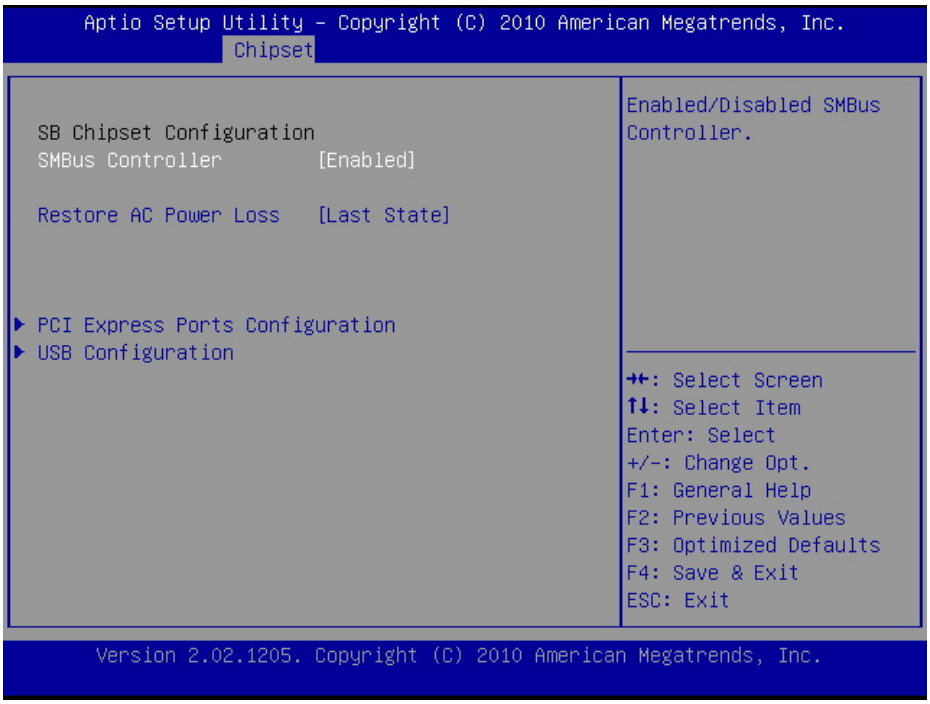
PEG Force Gen1

This item allows you to force PEG port downgrade to Gen1.

MRC Message Print: [Disabled]

This item allows you to enable/disable the MRC Message Print.

4.5.2 South Bridge Chipset Configuration



SMBus Controller: [Enabled]

This item allows you to enable/disable the system SMBUS function.

Restore AC Power Loss: [Last State]

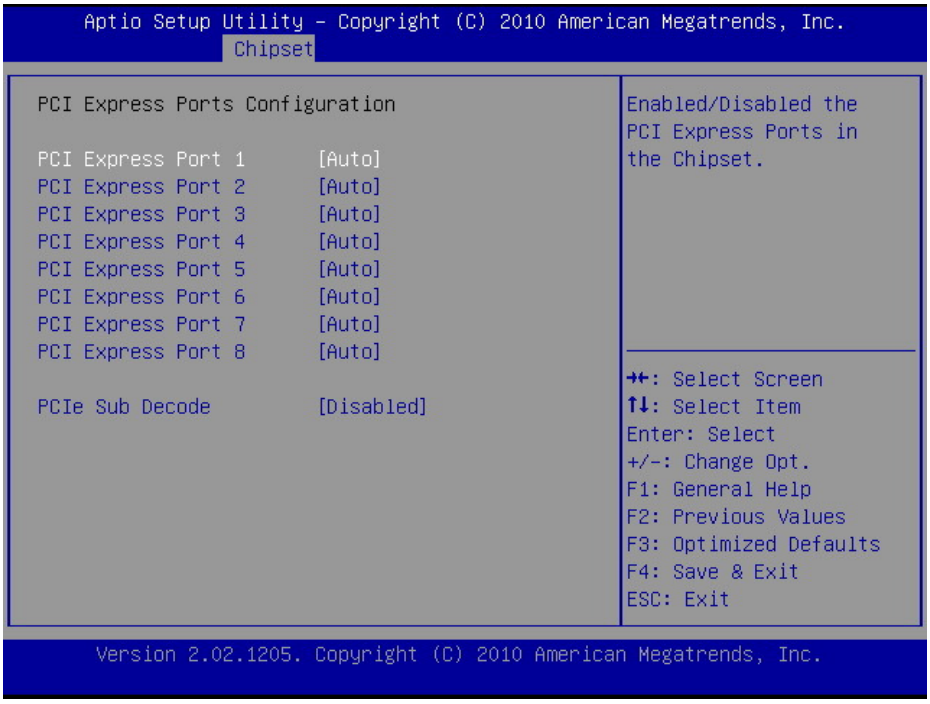
The system goes into on/off state after an AC power loss.

This item allows you to set the power state after an unexpected AC Power loss. If [Power Off] is selected, the AC Power remains off when the power recovers. If [Power On] is selected, the AC Power resumes and the system starts to boot up when the power recovers.

Options available: **Power Off/ Power On/Last State.**

PCI Express Ports Configuration

This sub menu allows you to change the setting of PCI Express ports.



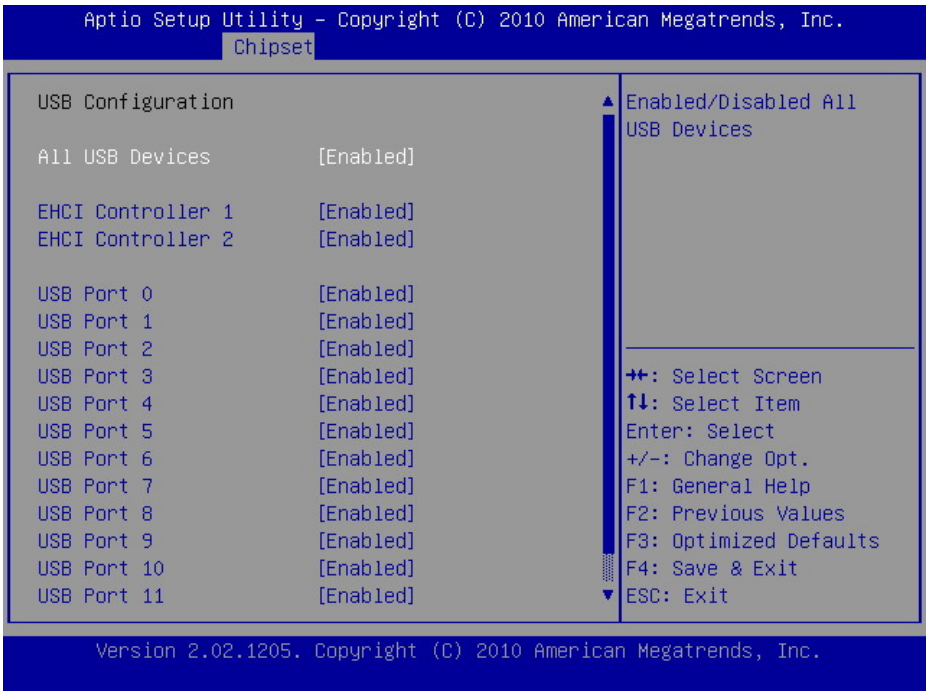
PCI Express Port 1~8 : [Auto]

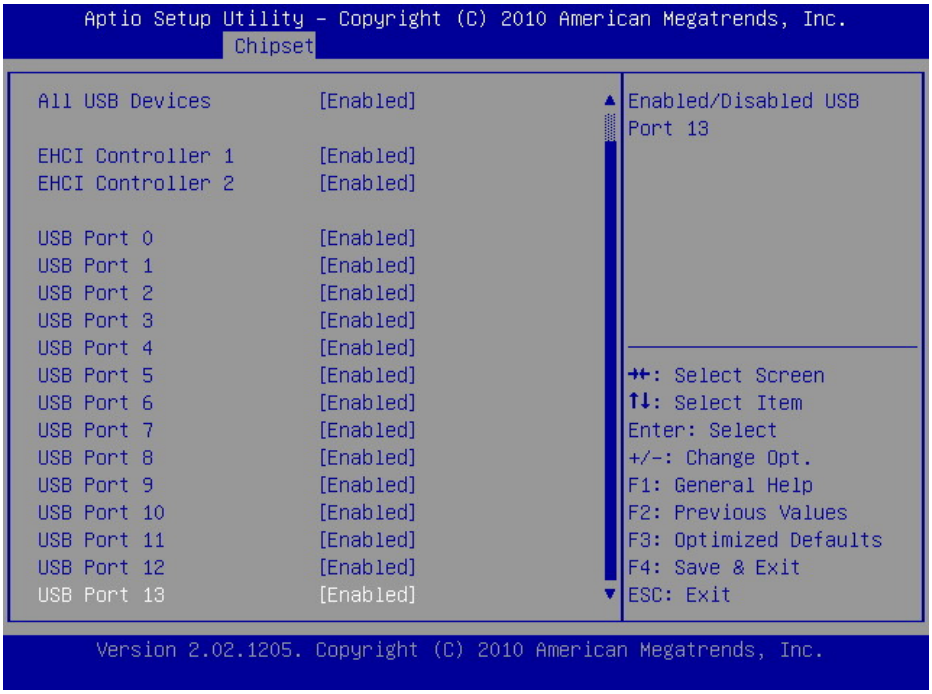
This item allows you to configure the PCI Express ports.

PCIe Sub Decode: [Disabled]

This item allows you to enable/disable the PCIe Sub Decode.

USB Configuration





All USB Devices

This item allows you to enable/disable the All USB Devices.

EHCI Controller 1 & 2

This item allows you to enable/disable the EHCI Controller 1 or 2.

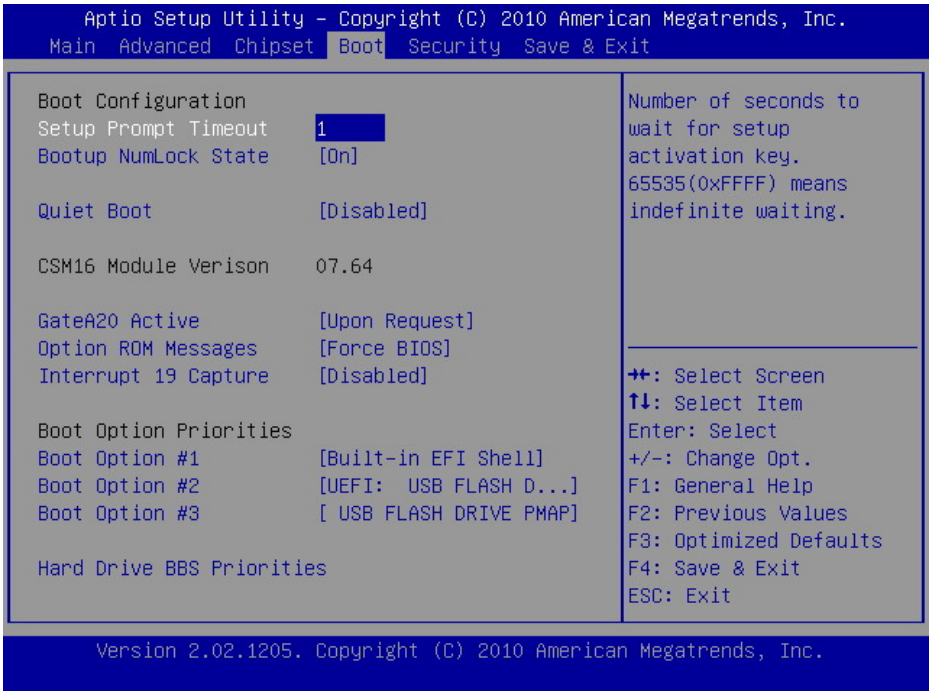
USB Port 1~13

This item allows you to enable/disable the USB Port 1~12.

4.6 Boot Menu

⇩Use the Boot Setup option as follows:

1. Choose "Boot" from the main menu. The following screen appears:



2. Move between items and select values by using the arrow keys. Modify the selected fields using the PnUP/PgDN Keys. For information on the various options, press <F1> key.

3. After you have finished with the Boot setup, press the <←> or <→> key to switch to other setup menu or press <F4> key to save setting.

Setup Prompt Timeout

Use the <+> and <-> keys to adjust the number of seconds to wait for setup activation key.

Bootup NumLock State

This item allows you to select "On" or "Off" power-on state for the NumLock.

Quiet Boot

If this option is set to Disabled, the BIOS displays normal POST messages. If Enabled, an OEM Logo is shown instead of POST messages.

GateA20 Active: [Upon Request]

This item allows you to configure the GateA20 Active feature.
[UPON REQUEST]: GA20 can be disabled using BIOS services.
[ALWAYS]: do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

Option ROM Messages: [Force BIOS]

This item allows you to select "Force BIOS" or "Keep Current" to set the display mode for Option ROM.

Interrupt 19 Capture: [Disabled]

This item allows you to enable/disable the Option ROM to trap Interrupt 19.

Boot Option Priorities

Choose boot priority from boot device.

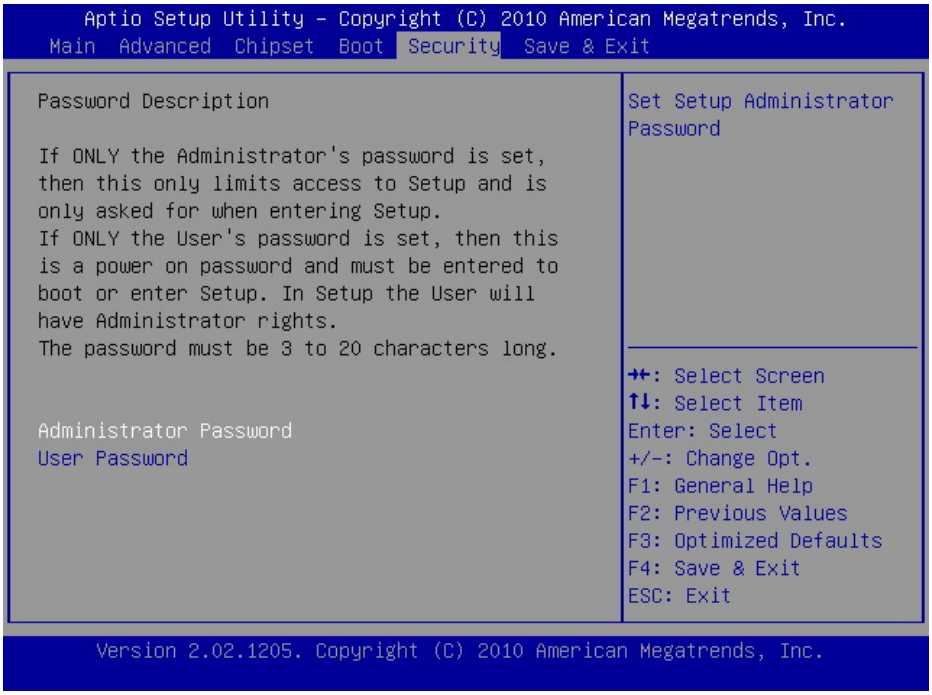
Boot Option #1~3:

These items allow you to change the boot priorities from boot devices.

4.7 Security Menu

⇩**Use the Security Setup option as follows:**

1. Choose "Security" from the main menu. The following screen appears:



2. Move between items and select values by using the arrow keys. Modify the selected fields using the PgUP/PgDN keys. Please press the <F1> key for information on the various options.

3. After you have finished with the Security setup, press the <←> or <→> key to switch to other setup menu or press <F4> key to save setting.

Administrator Password:

This item allows you to set or change the administrator password. The Administrator Password item on top of the screen shows the default Not Installed. After you have set a password, this item shows Installed.

User Password:

This item allows you to set or change the user password. The User Password item on top of the screen shows the default Not Installed. After you have set a

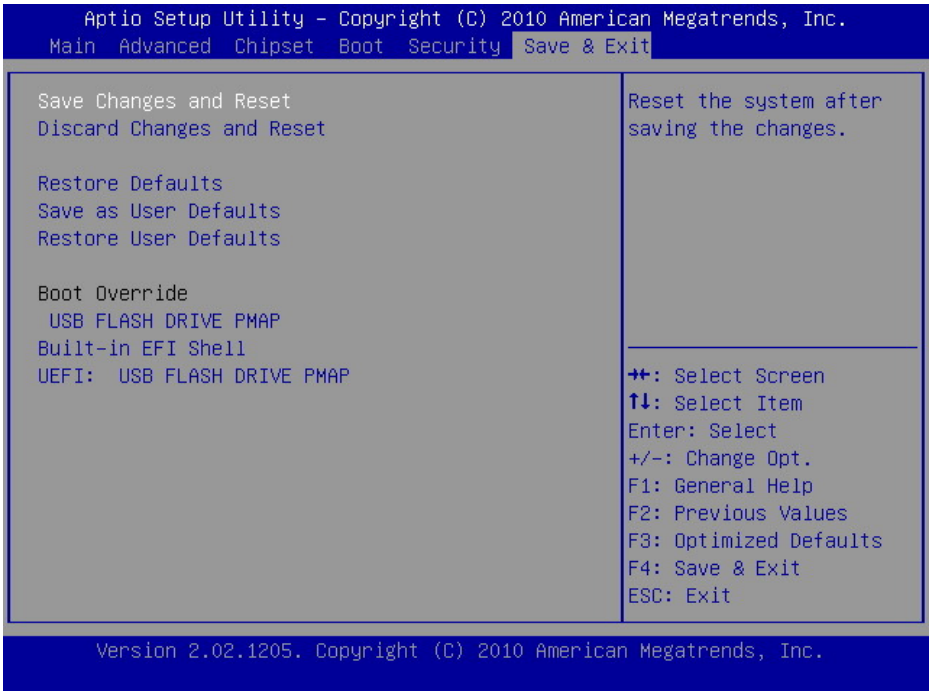
password, this item shows Installed.

4.8 Save & Exit Menu

The item allows you to save or discard your changes to the BIOS items, and load the optimal defaults or user defaults for the BIOS items.

⇩Use the Exit option as follows:

1. Choose "Exit" from the main menu, the following screen appears.



2. Move between items and select values by using the arrow keys. Modify the selected fields using the PgUP/PgDN keys. For information on the various options, please press <F1> key.

3. Press the <←> or <→> key to switch to other setup menu or press <F4> key to save setting.

Save Changes and Reset:

Store all changes you made into CMOS and reboot system. F4 key can be used for this operation.

Discard Changes and Reset:

Discard all changes you made and reboot system. ESC key can be used for this operation.

Restore Defaults:

This item allows you to load optimal defaults for each setting on the Setup Utility menus, which will provide the best performance settings for system. F9 key can be used for this operation.

Save as user Defaults:

This item allows you to save the user defaults.

Restore user Defaults:

This item allows you to restore the user defaults.

Boot Override:

This item allows you to select boot device for system to boot up one time without changing or saving setting. Restore the user defaults.

Chapter 5. Utility & Driver Installation

Please install the GbE modules properly before you install the OS, driver or other software.

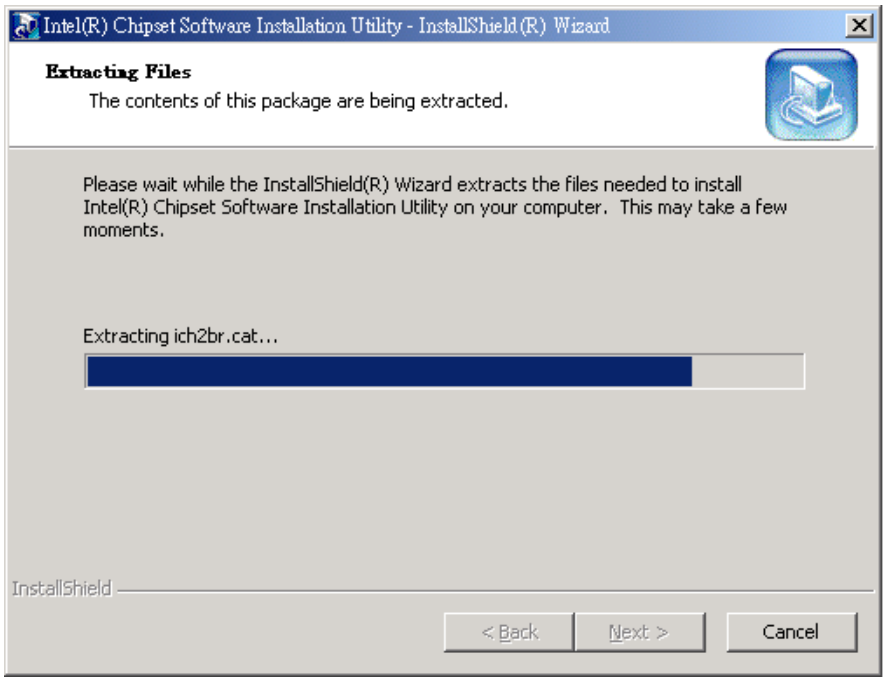
5.1 Operation System Supporting

PL-80310 can support Windows® and Linux® operation system as follows. Before installation, please check your OS version. If your OS is not in the following list, please upgrade your OS version.

OS	Version
Windows®	Windows Vista x64 Windows Server 2003 Windows Server 2008 Windows XP SP2 Windows XP SP3 Windows 7
Linux & Unix Like	Fedora 9 x64 (2.6.25) Redhat Enterprise 5.0 x64 Version 5.2 (2.6.18) Redhat Enterprise 5.0 x64 Version 5.3 (2.6.18-128.el5 Fedora Core 5 (2.6.15) Fedora 8 (2.6.23.1-42) CentOS 5.1 (2.6.18-53) FreeBSD 6.3-RC1

5.2 System Driver Installation

PL-80310 offers the system driver in the setup CD. Please install the driver following the procedures.



5.3 LAN Driver Installation

PL-80310 offers the LAN driver in the setup CD. Please click the Autorun file and install the driver following the procedures.

1. Insert the setup CD of PL-80310 into your CD-ROM drive.
2. Choose the Drivers file to click the Autorun icon.
3. Follow the procedures to finish the installation.

Appendix A: Watchdog Timer Programming Guide

Watchdog Timer overview

As systems continually become more complex, the likelihood that a platform will suffer a hard hang, an operating system (OS) software lockup, or an application lockup is also becoming more likely. Watchdog timer can be used to monitor system software operation and take corrective action if the software fails to function after the programmed period. This section describes the operation of the watchdog timer and how to program it.

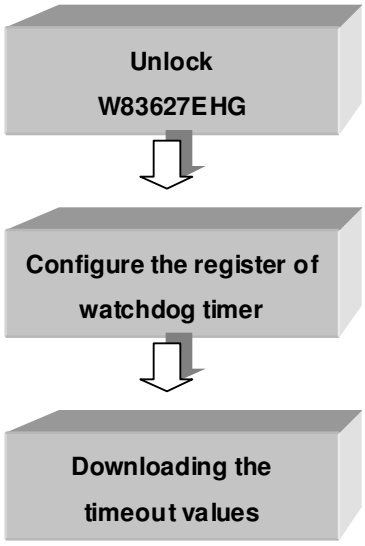
1. Programming the Watchdog Timer

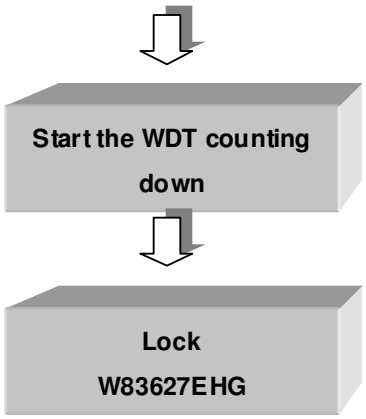
The WIN ENTERPRISES PL-80310 provides a watchdog timer that can reset the system or activate LAN bypass function. It provides the following function for user programming:

- Can be enabled and disabled by user's program
- Timer can be set from 1 to 255 seconds or 1 to 255 minutes
- Generates a KBRST# (P60) or activate WDTO# (P77) signal if the software fails to reset the timer when timeout.

2. Watchdog Timer Control Register

The I/O port address of the watchdog timer is 2EH and 2FH, 2EH is the address port, 2FH is the data port. You must first assign the address of register by writing address value into address port 2EH, then write/read data to/from the assigned register through data port 2FH





Watchdog Timer Registers		
Address of register (2EH)	**R/W**	**Value (2FH) and Description**
87H	----	Write this address to I/O address port 2EH twice to unlock the W83627EHG
07H	W	Write 08h to point to logical device 8 and select the register of watchdog timer.
30H	R/W	Write 01h to activate WDTO#. Disabled is set as default.
CRF5, Bit 3	R/W	Select WDTO# count mode. 0: Second Mode 1: Minute Mode
CRF5, Bit 1	R/W	Enable / Disable the WDTO# output low pulse to KBRST# 0: Disable 1: Enable
CRF6	R/W	Watchdog time-out value. 0: stop timer [default] 01~FFh: Writing a non-zero value to this register causes the counter to load the value to watchdog counter and start counting down. The amount of the count, in seconds or minutes, depends on the value set in register CRF5, bit 3. This number decides how long the watchdog timer waits for strobe before generating an interrupt or reset signal.

		Writing a new value to this register can reset the timer to count with the new value
AAH	-----	Write this address to I/O port 2EH to lock watchdog timer.

3. Example program 1

Enable watchdog timer and set 10 seconds as timeout interval and issue KBRST# as the time-out event occur.

```
;--------------------------------------------------------------------
;Enter the extended function mode, interruptible double-write
;--------------------------------------------------------------------
MOV DX,2EH   ; Unlock W83627EHG
MOV AL,87H
OUT DX,AL
OUT DX,AL
;--------------------------------------------------------------------
; Configure logical device 8
;--------------------------------------------------------------------
MOV AL,07H
OUT DX,AL      ; Point to Logical Device Number Reg.
INC DX
MOV AL,08H
OUT DX,AL      ; Select logical device 8
;--------------------------------------------------------------------
; Set second as counting unit and KBRST# time-out event
;--------------------------------------------------------------------
DEC DX
MOV AL,F5H
OUT DX,AL      ; Select CRF5
INC DX
IN AL,DX
AND AL,F5H     ; Set Watchdog time-our to second mode
OR AL,02H
OUT DX,AL      ; Enable the WDTO# output low pulse to KBRST#
;--------------------------------------------------------------------
; Load 10 seconds to Watchdog Counter and start counting down
;--------------------------------------------------------------------
DEC DX
MOV AL,F6H
```

```
OUT DX,AL       ; Select CRF6
INC DX
MOV AL,0AH
OUT DX,AL       ; Time-out occurs after 10 seconds
;-------------------------------------------------------------------------
; Exit extended function mode
;-------------------------------------------------------------------------
DEC DX
MOV AL,AAH
OUT DX,AL
```

4. Example program 2

Enable watchdog timer and set 2 minutes as timeout interval and set WDTO# signal as the time-out event to control LAN by-pass or activate hardware reset through JP2. Please refer to jumper setting section for more detail information.

```
;-------------------------------------------------------------------------
;Enter the extended function mode, interruptible double-write
;-------------------------------------------------------------------------
MOV DX,2EH   ; Unlock W83627EHG
MOV AL,87H
OUT DX,AL
OUT DX,AL
;-------------------------------------------------------------------------
; Configure logical device 8
;-------------------------------------------------------------------------
MOV AL,07H
OUT DX,AL       ; Point to Logical Device Number Reg.
INC DX
MOV AL,08H
OUT DX,AL       ; Select logical device 8
;-------------------------------------------------------------------------
; Set minute as counting unit
;-------------------------------------------------------------------------
```

```
DEC DX
MOV AL,F5H
OUT DX,AL       ; Select CRF5
INC DX
MOV AL,08H
OUT DX,AL       ; Set Watchdog time-our to minute mode
;-------------------------------------------------------------------------
; Load 2 minutes to Watchdog Counter and start counting down
;-------------------------------------------------------------------------
DEC DX
MOV AL,F6H
OUT DX,AL       ; Select CRF6
INC DX
MOV AL,02H
OUT DX,AL       ; Time-out occurs after 2 minutes
;-------------------------------------------------------------------------
; Exit extended function mode
;-------------------------------------------------------------------------
DEC DX
MOV AL,AAH
OUT DX,AL
```

Appendix B: LAN Bypass Programming Guide

WIN ENTERPRISES PL-80310 provides LAN bypass functionality to ensure that data can still pass through the device, even when it is powered off. This feature helps ensure the continuous flow of data through the device in the event of a hardware failure. For network security appliances deployed at the gateway, for example, it is crucial that they provide LAN bypass functionality to ensure that hardware failure on these appliances will not bring down the entire network. Related BIOS settings are in the "South Bridge Configuration" section.

1. LAN Bypass Definition

There are four bypass settings in BIOS setup.

Power off LAN Bypass1: Enable/Disable

Power on LAN Bypass1: Enable/Disable

Power off LAN Bypass2: Enable/Disable

Power on LAN Bypass2: Enable/Disable

Note: You must set "Power off LAN Bypass1" to "Enable" to get the "Power on LAN Bypass1" setup item and set "Power off LAN Bypass2" to "Enable" to get the "Power on LAN Bypass2" setup item.

There are three behavior of LAN Bypass function.

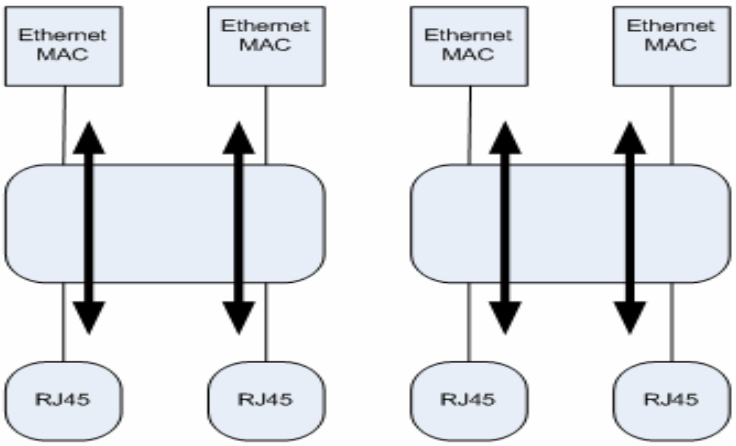
Power status	BIOS Bypass setting	Bypass Behavior
ON	Power off LAN Bypass1/2: Disable Power on LAN Bypass1/2: Disable	A
	Power off LAN Bypass1/2: Enable Power on LAN Bypass1/2: Enable	B
OFF	Power off LAN Bypass1/2: Disable *** Note	C
	Power off LAN Bypass1/2: Enable Power on LAN Bypass1/2: Disable	A

Note: If "Power off LAN Bypass1/2" set to "Disable", the "Power on LAN Bypass1/2" "Enable" can not be selected.

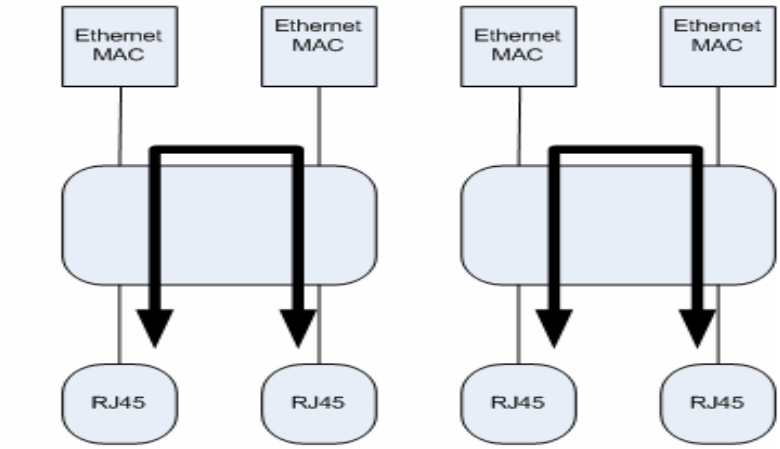
The PL-80310 provides four LAN ports with bypass function. The BIOS "Power on/off LAN Bypass1" settings control LAN ports on CN30 & CN31 (Segment 1)

and "Power on/off LAN Bypass2" settings control LAN ports on CN28 & CN29 (Segment 2). Each segment is controllable through GPIO pins.

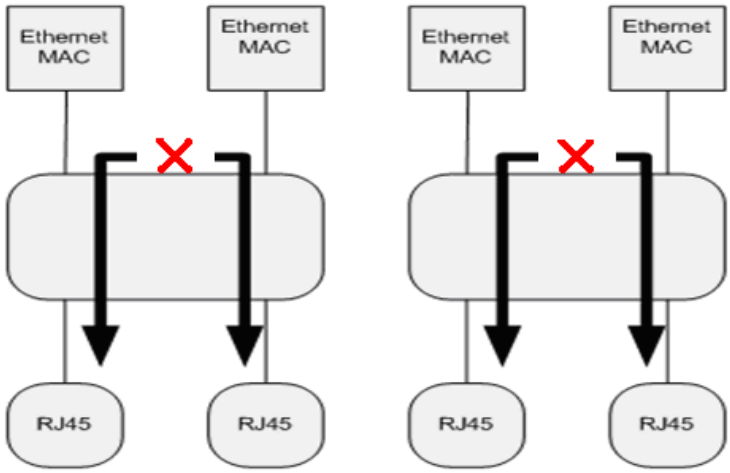
Bypass Behavior A:



Bypass Behavior B:



Bypass Behavior C:



2. How to control Segment 1 & 2 bypass function by watchdog timer

Please follow below steps to set the LAN bypass function control by watchdog timer.

(1). Setup jumper JP2 to 1-2 shorted to enable bypass function when watchdog timer time-out.

(2). Refer to watchdog timer section to set timer interval value and enable watchdog timer.

Note: Once the watchdog timer time-out you need to restart the system to reset the timer.

3. How to control Segment 1 & 2 LAN bypass function by GPIO during power on state

The bypass function can be enabled or disabled through ICH GPIO38 & GPIO39 during power on state. Below is the I/O port address and control bit.

Power ON State Bypass Control Status Register							
I/O Address: 4B8H							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	W	X	X	X	X	X	X

W: Write, X: Not used

Bit 7:

0 – Set segment 2 bypass to disable when power on

1 – Set segment 2 bypass to enable when power on

Bit 6:

0 – Set segment 1 bypass to disable when power on

1 – Set segment 1 bypass to enable when power on

Please follow below steps to set the LAN bypass function control by GPIO.

(1). Setup JP6 to 1-2 to enable bypass segment 1 function control by GPIO38.

(2). Setup JP7 to 1-2 to enable bypass segment 2 function control by GPIO39.

(3). Refer to below program code and set segment 1 & 2 LAN ports to bypass state or normal state.

Custom Embedded Solutions

Segment 1: Control by GPIO 38

Normal state (Behavior A)

```
==============================
MOV DX, 4B8H        ;address
IN AX, DX           ;read value
AND AL, 0BFH        ;mask bit 6
OR   AL, 00H        ;set bit 6 = 0
OUT DX, AL          ;send value
```

Bypass Enabled (Behavior B)

```
==============================
MOV DX, 4B8H        ;address
IN AX, DX           ;read value
AND AL, 0BFH        ;mask bit 6
OR AL, 40H          ;set bit 6 = 1
OUT DX, AL          ;send value
```

Segment 2: Control by GPIO 39

Normal state (Behavior A)

```
==============================
MOV DX, 4B8H        ;address
IN AX, DX           ;read value
AND AL, 07FH        ;mask bit 7
OR AL, 00H          ;set bit 7 = 0
OUT DX, AL          ;send value
```

Bypass Enabled (Behavior B)

```
==============================
MOV DX, 4B8H        ;address
IN AX, DX           ;read value
AND AL, 07FH        ;mask bit 7
OR AL, 80H          ;set bit 7 = 1
OUT DX, AL          ;send value
```

4. How to control Segment 1 & 2 LAN bypass function by GPIO during power off state

The power off bypass function can be enabled or disabled through W83627EHG GPO30 ~33. Below is the I/O port address and control bit.

Power off State Bypass Control Status Register							
Logical device 9, CRF1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	R/W	R/W	R/W	R/W

R/W: Read/Write, X: Not used

Bit [1:0]

01 - Set segment 1 bypass to enable when power off

10 - Set segment 1 bypass to disable when power off

Bit [3:2]

01 - Set segment 2 bypass to enable when power off

10 - Set segment 2 bypass to disable when power off

Refer to below program code and set segment 1 & 2 LAN ports to bypass state or disable when power is off.

Segment 1: Control by CRF1 bit 1 & 0

Bypass disabled when power off

```
;--------------------------------------------------------------------------
;Enter the extended function mode, interruptible double-write
;--------------------------------------------------------------------------
 MOV DX, 87H             ;address
 MOV AL, 2EH             ;Index
 OUT DX, AL              ;enter super IO
 OUT DX, AL              ;enter super IO
;--------------------------------------------------------------------------
; Configure logical device 9
;--------------------------------------------------------------------------
 MOV DX, 2EH
```

```
MOV AL, 07H
OUT DX, AL              ;O 2E 07
MOV DX, 2FH
MOV AL, 09H
OUT DX, AL              ;O 2F 09 (select logic device 9)
;-------------------------------------------------------------------------
; Read CRF1 and set bit 1= 1, bit 0= 0 to disable bypass circuit
;-------------------------------------------------------------------------
MOV DX, 2EH
MOV AL, 0F1H
OUT DX, AL              ;O 2E F1
MOV DX, 2FH
IN AL, DX               ;read F1
AND AL, 0FCH            ;mask bit 1, bit 0
OR AL, 02H              ;set bit 1= 1, bit 0= 0
OUT DX, AL              ;send value
;-------------------------------------------------------------------------
; Exit extended function mode
;-------------------------------------------------------------------------
MOV DX, 2EH
MOV AL, 0AAH
OUT DX, AL              ;close super IO
```

Bypass enabled when power off

```
;-------------------------------------------------------------------------
;Enter the extended function mode, interruptible double-write
;-------------------------------------------------------------------------
MOV DX, 87H             ;address
MOV AL, 2EH             ;Index
OUT DX, AL              ;enter super IO
OUT DX, AL              ;enter super IO
;-------------------------------------------------------------------------
; Configure logical device 9
;-------------------------------------------------------------------------
MOV DX, 2EH
MOV AL, 07H
```

```
OUT DX, AL              ;O 2E 07
MOV DX, 2FH
MOV AL, 09H
OUT DX, AL              ;O 2F 09 (select logic device 9)
;-------------------------------------------------------------------------
; Read CRF1 and set bit 1= 0, bit 0= 1 to enable bypass circuit
;-------------------------------------------------------------------------
MOV DX, 2EH
MOV AL, 0F1H
OUT DX, AL              ;O 2E F1
MOV DX, 2FH
IN AL, DX               ;read F1
AND AL, 0FCH            ;mask bit 1, bit 0
OR AL, 01H              ;set bit 1= 0, bit 0= 1
OUT DX, AL              ;send value
;-------------------------------------------------------------------------
; Exit extended function mode
;-------------------------------------------------------------------------
MOV DX, 2EH
MOV AL, 0AAH
OUT DX, AL              ;close super IO
```

Segment 2: Control by CRF1 bit 3 & 2

Bypass disabled when power off

```
;-------------------------------------------------------------------------
;Enter the extended function mode, interruptible double-write
;-------------------------------------------------------------------------
MOV DX, 87H             ;address
MOV AL, 2EH             ;Index
OUT DX, AL              ;enter super IO
OUT DX, AL              ;enter super IO
;-------------------------------------------------------------------------
; Configure logical device 9
;-------------------------------------------------------------------------
MOV DX, 2EH
```

```
MOV AL, 07H
OUT DX, AL              ;O 2E 07
MOV DX, 2FH
MOV AL, 09H
OUT DX, AL              ;O 2F 09 (select logic device 9)
;-------------------------------------------------------------------------
 ; Read CRF1 and set bit 3= 1, bit 2= 0 to disable bypass circuit
;-------------------------------------------------------------------------
MOV DX, 2EH
MOV AL, 0F1 H
OUT DX, AL              ;O 2E F1
MOV DX, 2FH
IN AL, DX               ;read F1
AND AL, 0F3H            ;mask bit 3, bit 2
OR AL, 08H              ;set bit 3= 1, bit 2= 0
OUT DX, AL              ;send value
;-------------------------------------------------------------------------
; Exit extended function mode
;-------------------------------------------------------------------------
MOV DX, 2EH
MOV AL, 0AAH
OUT DX, AL              ;close super IO
```

Bypass enabled when power off

```
;-------------------------------------------------------------------------
;Enter the extended function mode, interruptible double-write
;-------------------------------------------------------------------------
MOV DX, 87H             ;address
MOV AL, 2EH             ;Index
OUT DX, AL              ;enter super IO
OUT DX, AL              ;enter super IO
;-------------------------------------------------------------------------
; Configure logical device 9
;-------------------------------------------------------------------------
MOV DX, 2EH
MOV AL, 07H
```

```
OUT DX, AL              ;O 2E 07
MOV DX, 2FH
MOV AL, 09H
OUT DX, AL              ;O 2F 09 (select logic device 9)
;-------------------------------------------------------------------------
 ; Read CRF1 and set bit 3= 0, bit 2= 1 to enable bypass circuit
;-------------------------------------------------------------------------
MOV DX, 2EH
MOV AL, 0F1H
OUT DX, AL              ;O 2E F1
MOV DX, 2FH
IN AL, DX               ;read F1
AND AL, 0F3H            ;mask bit 3, bit 2
OR AL, 04H              ;set bit3 = 0, bit 2= 1
OUT DX, AL              ;send value
;-------------------------------------------------------------------------
; Exit extended function mode
;-------------------------------------------------------------------------
MOV DX, 2EH
MOV AL, 0AAH
OUT DX, AL              ;close super IO
```

5. How to save bypass settings into CMOS data

Normally the LAN bypass function is set by BIOS settings. The user also can change the LAN bypass settings by previous program. But the new settings will be changed back to BIOS default when recycle the power supply or system reboot. If you want the new settings also update to BIOS setup setting, please add below sample code to the end of previous section program.

```
MOV DX, 72H
MOV AL, 29H
OUT DX, AL
MOV DX, 73H
MOV AL, #value#
OUT DX, AL
```

Segment 1	OFF	D	E	E	E	E	E	E	D	D
Segment 1	ON	D	D	E	E	E	D	D	D	D
Segment 2	OFF	D	D	D	E	E	E	E	E	E
Segment 2	ON	D	D	D	D	E	E	D	D	E
Value		7Bh	6Bh	63H	23H	03H	0BH	2BH	3BH	1BH

D=disable, E=enable

ON= power on bypass status

OFF= power off bypass status

For example:

Power off LAN Segment 1 bypass: Enable

Power on LAN Segment 1 bypass: Disable

Power off LAN Segment 2 bypass: Enable

Power on LAN Segment 2 bypass: Enable

Sample code:

```
MOV DX, 72H
MOV AL, 29H
OUT DX, AL
MOV DX, 73H
MOV AL, 0BH
OUT DX, AL
```

6. How to control R137 LAN bypass function by GPIO during power on state

The bypass function can be enabled or disabled through ICH GPIO33 during power on state. Below is the I/O port address and control bit.

Power ON State Bypass Control Status Register							
I/O Address: 4B8H							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	W	X	X	X	X	W	X

W: Write, X: Not used

Bit 1

1 – Set segment 1 bypass to disable when power on

0 – Set segment 1 bypass to enable when power on

Segment 1: Control by GPIO 33

Normal state (Behavior A)

```
==============================
MOV DX, 4B8H        ;address
IN AX, DX           ;read value
AND AL, 0FDH        ;mask bit 1
OR   AL, 02H        ;set bit 1 = 1
OUT DX, AL          ;send value
```

Bypass Enabled (Behavior B)

```
==============================
MOV DX, 4B8H        ;address
IN AX, DX           ;read value
AND AL, 0FDH        ;mask bit 1
OR AL, 00H          ;set bit 1 = 0
OUT DX, AL          ;send value
```

Appendix C: Programming the GPIO

bit	7	6	5	4	3	2	1	0
GPIO	GPO 7	GPO 6	GPO 5	GPO 4	GPI 3	GPI 2	GPI 1	GPI 0

Programming of the GPI

0: LOW; 1: HIGH

GPI 3 Bit 3	GPI 2 Bit 2	GPI 1 Bit 1	GPI 0 Bit 0	Data
0	0	0	0	x0
0	0	0	1	x1
0	0	1	0	x2
0	0	1	1	x3
0	1	0	0	x4
0	1	0	1	x5
0	1	1	0	x6
0	1	1	1	x7
1	0	0	0	x8
1	0	0	1	x9
1	0	1	0	xA
1	0	1	1	xB
1	1	0	0	xC
1	1	0	1	xD
1	1	1	0	xE
1	1	1	1	xF

Note: x is the reserved data.

Programming of the GPO

0: LOW; 1: HIGH

GPO 7 Bit 7	GPO 6 Bit 6	GPO 5 Bit 5	GPO 4 Bit 4	Data
0	0	0	0	0x
0	0	0	1	1x

0	0	1	0	2x
0	0	1	1	3x
0	1	0	0	4x
0	1	0	1	5x
0	1	1	0	6x
0	1	1	1	7x
1	0	0	0	8x
1	0	0	1	9x
1	0	1	0	Ax
1	0	1	1	Bx
1	1	0	0	Cx
1	1	0	1	Dx
1	1	1	0	Ex
1	1	1	1	Fx

Note: x is the reserved data.

DOS DEBUG

Program 1: Initializing the GPIO

```
-O 2E 87
-O 2E 87
-O 2E 29    //configuration register(CR29)
-O 2F 01    //set GPIO ,not GAME PORT
-O 2E 07    //point to logical device number reg.
-O 2F 07    //select logical device 7
-O 2E 30    //configuration register(CR30)
-O 2F 01    //open logical device control
-O 2E F0    //configuration register(CRf0)
-O 2F 0F    // 00001111 : 0=ouput; 1=input
```

Program 2: Programming of the GPI

```
-O 2E F1
-I 2F        // read value (00 ~ FF)
```

Program 3: Programming of the GPO

-O 2E F1 -O 2F Xx // X= (0 ~ F) output value; x=(0 ~ F) don't care

Appendix D: System Resources

Interrupt Controller:

The PL-80310 is a fully PC compatible appliance. If you would like to use extra add-on cards, please make sure that the IRQs do not conflict.

Any remaining IRQs then may be assigned to this PCI Bus. You are able to use Microsoft's Diagnostic (MDS.EXE) utility included in Windows directory to see their map.

IRQ	Assignment
IRQ0	Timer
IRQ1	Keyboard
IRQ2	Interrupt rerouting from IRQ8 through IRQ15
IRQ3	COM2
IRQ4	COM1
IRQ5	PCI-PCI Bridge
IRQ6	PCI-PCI Bridge
IRQ7	LPT1
IRQ8	RTC
IRQ9	ISA/free
IRQ10	PCI-PCI Bridge
IRQ11	PCI-PCI Bridge
IRQ12	ISA/free
IRQ13	Coprocessor
IRQ14	ISA/free
IRQ15	ISA/free

DMA Channel Assignment:

Channel 4 is by default used to cascade to two controllers

Channel	Assignment
DMA0	ISA/Free
DMA1	ISA/Free
DMA2	ISA/Free
DMA3	ISA/Free
DMA4	AT DMA controller /Cascade
DMA5	ISA/Free
DMA6	ISA/Free
DMA7	ISA/Free

Memory Map:

The following table indicates memory of PL-80310. The address ranges specify the runtime code length.

Memory below 1MB (1MB ~ 640KB)

Address Range	Type	Owner
A0000 ~ AFFFF	ISA	VGA Adapter
B0000 ~ BFFFF	ISA	VGA Adapter
C0000 ~ CC3FF	ISA	Adapter ROM
E0000 ~ EFFFF	ISA	Mapped RAM
F0000 ~ FFFFF	ISA	System BIOS

Memory above 1MB (1MB ~ 1012352 KB)

Address Range	Type	Owner
D0000000~DFFFFFF3	PCI	VGA Adapter
FDFFB800~FDFFBBFF	PCI	IDE Controller
FE000000~FE3FFFFB	PCI	VGA Adapter
FE400000~FE4FFFFF	PCI	PCI-PCI Bridge
FE500000~FE6FFFFF	PCI	PCI-PCI Bridge
FE700000~FE7FFFFF	PCI	PCI-PCI Bridge
FE800000~FE8FFFFF	PCI	PCI-PCI Bridge
FE900000~FE9FFFFF	PCI	PCI-PCI Bridge
FEA00000~FEAFFFFF	PCI	PCI-PCI Bridge
FEB00000~FEBFFFFF	PCI	PCI-PCI Bridge

System Memory Map

Start High	Start Low	Size High	Size	Type
00000000	00000000	00000000	0009FC00	Available
00000000	0009FC00	00000000	00000400	Reserved
00000000	000E0000	00000000	00020000	Reserved
00000000	00100000	00000000	3DCA0000	Available
00000000	3DDA0000	00000000	0000E000	ACPI Space
00000000	3DDAE000	00000000	00042000	NVS Space
00000000	3DDF0000	00000000	00010000	Reserved
00000000	3DE00000	00000000	02200000	Reserved
00000000	FEE00000	00000000	00001000	Reserved
00000000	FFE00000	00000000	00200000	Reserved

I/O Map:

The addresses shown in the table are typical locations

I/O Port	Assignment
0 ~ F	AT DMA controller
20 ~ 21	AT interrupt controller
2E ~ 2F	Motherboard Resource
40 ~ 43	8254 Compatible Programmable Timer
60	IBM Enhanced keyboard controller

61	AT Style Speaker
64	IBM Enhanced keyboard controller
70 ~ 71	Real Time Clock
72 ~ 75	Motherboard Resource
80 ~ 90	AT DMA controller
94 ~ 9F	AT DMA controller
A0 ~ A1	AT interrupt controller
C0 ~ DE	AT DMA controller
F0 ~ FF	Math Coprocessor
2F8 ~ 2FF	COM2
378 ~ 37F	LPT1
3B0 ~ 3BB	VGA Adapter
3C0 ~ 3DF	VGA Adapter
3F8 ~ 3FF	COM1
400 ~ 41E	SMBus Controller
480 ~ 4BF	Motherboard Resource
4D0 ~ 4D1	Motherboard Resource
800 ~ 87F	Motherboard Resource
8F0 ~ 8FF	Motherboard Resource
A00 ~ A0F	Motherboard Resource
A10 ~ A1F	Motherboard Resource
CF8 ~ CFF	Motherboard Resource
6800 ~ 680E	IDE Controller
6880 ~ 6882	IDE Controller
6C00 ~ 6C06	IDE Controller
7000 ~ 7002	IDE Controller
7080 ~ 7086	IDE Controller
7400 ~ 741E	USB Controller
7480 ~ 749E	USB Controller
7800 ~ 781E	USB Controller
7880 ~ 789E	USB Controller
7C00 ~ 7C06	VGA Adapter
8000 ~ 8FFF	PCI-PCI Bridge
9000 ~ 9FFF	PCI-PCI Bridge
A000 ~ AFFF	PCI-PCI Bridge

B000 ~ BFFF	PCI-PCI Bridge
C000 ~ CFFF	PCI-PCI Bridge
D000 ~ DFFF	PCI-PCI Bridge
E000 ~ EFFF	PCI-PCI Bridge
FFA0 ~ FFAE	IDE Controller

Appendix E: Cable Development Kit

The PL-80310 offers some cables for development use.

DK001

Item & Description	Part No.	Qty
Ethernet Cat.5 Cable 2M/ RoHS	CB-EC5200-00	1
Cross Over 2M Color/ RoHS	CB-CO5202/4-00	1
RJ45 to DB9 2M Cable/ RoHS	CB-RJDB91-00	1
2m null modem cable/ RoHS	CB-DB9200-01	1
VGA CABLE (2mm) 15CM/ RoHS	CB-IVGA01-00	1
KB/MS CABLE 15CM/ RoHS	CB-IPS200-00	1
USB CABLE w/ Bracket/ RoHS	CB-IUSB01-00	1

CB-EC5200-00

CB -CO5202/4-00

CB -RJDB91-00

CB-DB9200-00

CB-IVGA01-00

CB-IPS200-00

CB-IUSB01-00