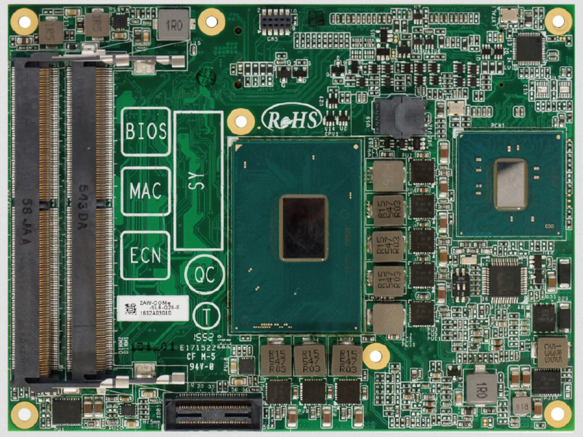
Custom Embedded Solutions



COM Express

MB-73430

User's Manual

COM Express®

Custom Embedded Solutions

Version:

Release Date:

Part Number:

Revision History

Revision	Description	Date	By
1.0	Initial Release	2016.01.29	JH

Preface

This user manual offers detailed information about components, pinouts, connectors and BIOS Setups of WIN's MB-73430. For more information about design and development for COM Express™ applications, please refer to documents released from the PCI Industrial Computer Manufacturers Group (PICMG):

- COM Express™ Design Guide
- COM Express™ Specification

Disclaimer

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Hazardous substance-Free (RoHS) Compliant

This product is designed and developed on hazardous substance-free components and parts and totally RoHS (Restriction of Hazardous Substances Directive 2002/95/EC) compliant.

Certification

WIN Enterprises, Inc. is certified to DIN EN ISO 9001 and 14001 standards.

Electrostatic Sensitive Device

This product is an electrostatic sensitive device (ESD) and packaged accordingly. In any case, this product can not be opened, handled, stored or transported without proper ESD protection mechanisms and please store and ship this products in its original manufacturer's packaging. Failure to comply with these guidelines will make this product damaged and avoid Limited Warranty offered by WIN Enterprises, Inc.

Table of Contents

1. Introduction

COM Express™ is an open industry standard defined exclusively for COMs (computer on modules) and offers a fast solution of forward/backward compatibility for legacy I/O interface and the latest technologies available. COM Express™ modules are available in following form factors:

Type	Size
COM Express® mini	84mm x 55mm
COM Express® Compact	95mm x 95mm
COM Express® Basic	125mm x 95mm
COM Express® Extended	155mm x110mm

Adapting Intel® Hyper-Threading Technology (up to 4 cores, 8 threads), CPU/chipset-controlled DDR4 dual-channel memory 1866/2133 MHz, Intel® Flexible Display Interface and Direct Media Interface, MB-73430 is a PICMG COM.0 R2.1-compliant Basic Size Type 6 computer-on-module that featuring 64-bit 6th-Gen Intel® Core™/Celeron® (“Skylake-H”) processors and QM170 Chipset and designed and developed exclusively for applications demanding extremely high performance for graphic and data processing.

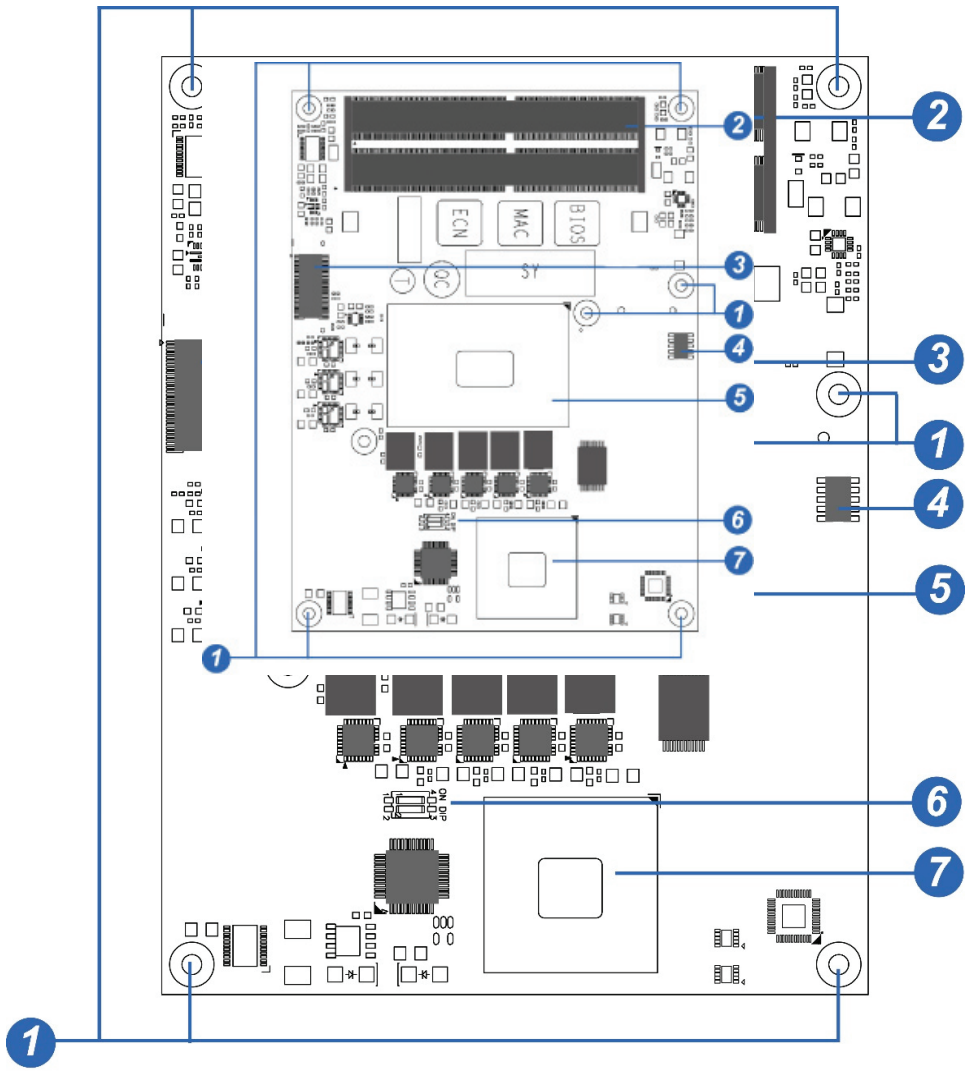
As a COM (computer on module), MB-73430 integrates all the core components and has to work with an application specific carrier board. Given its legacy-free design (no Super I/O, PS/2 keyboard and mouse), a COM module provides most of the functional requirements for any application in most of industries such as rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet (to name a few). For I/O pinout, a COM module offers PCI Express, Serial ATA, and LPC options through which supporting ranges of potential peripherals. Thanks to its robust thermal and mechanical strategies and combining with extended power-management, MB-73430 can perfectly satisfy all applications. The most important benefit users can enjoy is that COM Express™ modules is a scalable solution that can diversify the product range by using different performance class or form factor size modules for any new application is created by simply unplugging the old module and replace it with another new one and no more redesigning is required.

Types	Type 1	Type 2	Type 6	Type 10
Connector Row	A-B	A-B C-D	A-B C-D	A-B
PCI Express Lane	Up to 6	Up to 22	Up to 24	Up to 4
PCI	N/A	32 bit	N/A	N/A
IDE Channel	1	1		

LAN port	1	1	1	1
USB 2.0/USB 3.0	8 / 0	8 / 0	8 / 4	8 / 0
Display Interfaces	VGA, LVDS	VGA, LVDS,PEG/SDVO	VGA,LVDS,PEG, 3 X DDI	1x DDI

1.1 Hardware Briefing

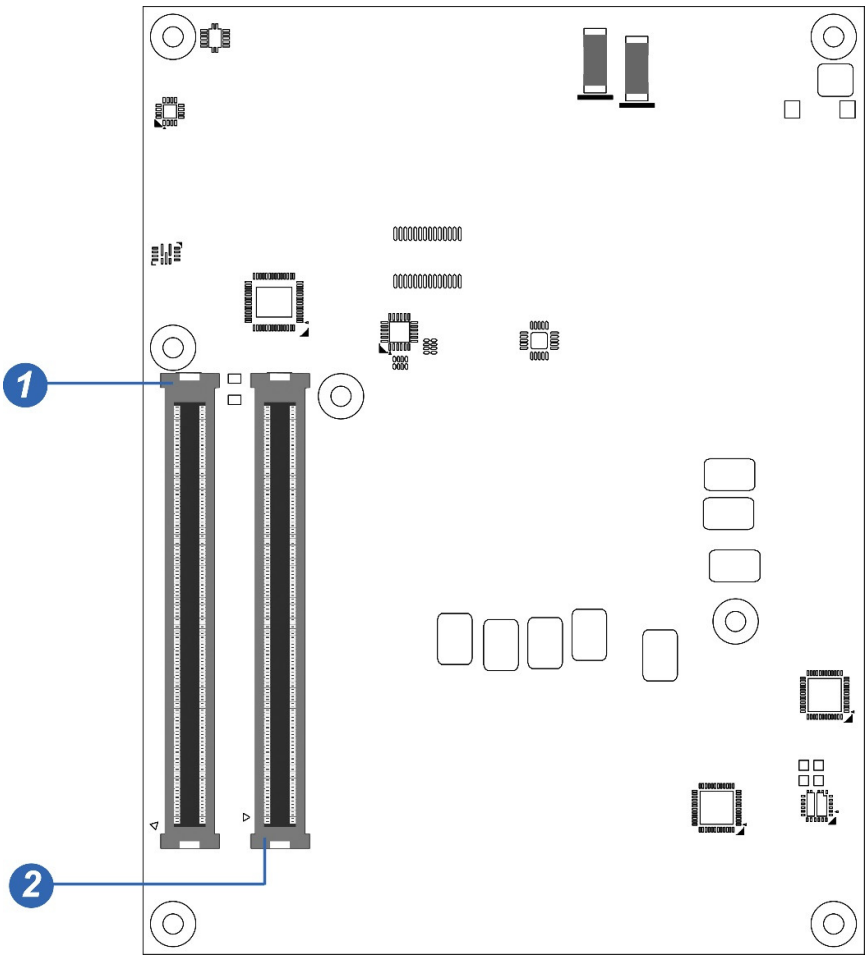
1.1.1 TOP VIEW



1.	Mounting holes	4.	Port 80
2.	SODIMMDDR4 slot	5.	Skylake-H CPU

3.	XDP (Debug Header)	*6.*	PCI Express Configuration Switch
7.	QM-170Chipset		

1.1.2. BOTTOM VIEW



1.	Board-to-board Connector A-B
2.	Board-to-board Connector C-D

2. Specifications

2.1. Core System

CPU

- 6th Generation Intel® Core™ and Celeron®
- Intel® Core™ i7-6820EQ 2.8/3.5GHz (Turbo), 0.35/1.0GHz (Turbo), 45W/35W(cTDP) (4C/GT2)
- Intel® Core™ i7-6822EQ 2/2.8GHz (Turbo), 0.35/1.0GHz (Turbo), 25W(4C/GT2) *
- Intel® Core™ i5-6440EQ 2.7/3.4GHz (Turbo), 0.35/1.0GHz (Turbo), 45W/35W(cTDP) (4C/GT2)
- Intel® Core™ i5-6442EQ 1.9/2.7GHz (Turbo), 0.35/1.0GHz (Turbo), 25W (4C/GT2) *
- Intel® Core™ i3-6100E 2.7GHz, 0.35/1.0GHz (Turbo), 35W (4C/GT2)
- Intel® Core™ i3-6102E 1.9GHz, 0.35/1.0GHz (Turbo), 25W (4C/GT2)

***Available upon request**

CPU Supported

- Intel® VT
- Intel® TXT
- Intel® SSE4.2
- Intel® HT Technology
- Intel® 64 Architecture
- Execute Disable Bit
- Intel® Turbo Boost Technology 2.0
- Intel® AVX2
- Intel® AES-NI
- PCLMULQDQ Instruction
- Intel® Device Protection Technology with Intel® Secure Key
- Intel® TSXNI

Note: Available features depend on processor SKU.

Cache

- Xeon®/Core™ i7 8MB
- Core™ i5 6MB
- Core™ i3 3MB

Chipset

- Mobile Intel® QM170

Embedded BIOS

- American Megatrends Inc. EFI with 8 MB CMOS backup, Intel® AMT 11 support supported

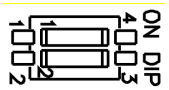
2.2. Expansion Busses

PCIe x16 (Gen3) x1 can be configure to:

1 x16

2 x 8

1 x 8 + 2 x 4



PCI Express Configuration Switch

Mode	Pin 1	Pin 2
1x PCIe x16 (default)	Off	Off
2x PCIe x8	On	Off
1x PCIe x8 + 2x PCIe x4	On	On
Reserved	Off	On

PCIe x1 (Gen3) X6 (AB): Lanes 0/1/2/3/4/5

PCIe x1 (Gen3) X2 (CD): Lane 6/7

Note: PCIe lanes 0/1/2/3 can also be configured to x2, x4 PCIe lanes 4/5/6/7 can also be configured to x2, x4.

LPC bus X1

SMBus (system) X1

I2C (user) X1

2.3. Video

CPU

Intel® Generation 9 Graphics integrated in CPU and featured with:

- DisplayPort, HDMI and LVD, can operate simultaneously (eDP integrated in LVDS)
- Encode/transcode high definition (HD)video supported
- High definition (HD)video (e.g. Blu-ray DVD) supported
- 3D video supported (via HDMI)
- Playback of Blu-ray Disc 3D content using HDMI (HDMI e1.4a)
- DirectX Video Acceleration (DXVA) supported
- HEVC/H.265, H.264, M/JPEG, MPEG2, VC1, WMV9, VP8/VP9 HW decode supported
- HEVC/H.265, M/JPEG, MPEG2 HW encode supported
- Advanced Scheduler 2.0, 1.0 and XPDM supported
- DirectX 12, DirectX 11.3, DirectX 11, DirectX 10.1, DirectX 10 and DirectX 9 supported
- Open Graphics Library(OpenGL) 4.4 supported
- OpenCL (Open Computing Language) supported

Note: features listed above is available depending on operation system

Display Interface

LVDS	single/dual channel 18/24-bit LVDS to LVDS (NXP IC) via eDP
eDP	4 lanes supported maximum, integrated in LVDS (BOM optional)
Digital Display Port x 3	DisplayPort/HDMI/DVI supported

2.4. Audio

Intel® HD Audio	Integrated inQM170
Audio Codec	in AW-COMe-EVAL carrier board

2.5. LAN

Intel® i219LM Ethernet controller

Integrated: MAC integrated in QM170

10/100/1000 Mbits/Gigabit Ethernet LAN supported

2.6. Multi I/O and Storage

USB	4x USB 3.0 (USB 0,1,2,3)
	4x USB 2.0 (USB 4,5,6,7)
SATA	4x SATA 6Gb/s (SATA 0,1,2,3)

GPIO 4 GPO and 4 GPI

Note: For SATA 6Gb/s, it is strongly recommended to install a SATA redriver on the carrier board.

2.7. Serial I/O

Chipset Nuvoton NCT5104D

Ports 2x UART for Rx/Tx only

	Description	IRQ	Address
COM 1	Supported by Super I/O (W83627DHG) on Carrier board	4	3F8h
COM 2	Supported by Super I/O (W83627DHG) on Carrier board	3	2F8h
COM 3	Supported by Module I/O (NCT5104DSEC) (SER0, A98/A99)	10	3E8h
COM 4	Supported by Module I/O (NCT5104DSEC) (SER1, A101/A102)	5	2E8h

2.8. Trusted Platform Module (TPM) (Optional)

Chipset SLB9660XT1.2

Type TPM 1.2

2.9. Debug Headers

Port 80 10-pin debug header for LPC debug card diagnosing module.

60-pin XDP merged connector for ICE debug of CPU/chipset (optional).

2.10. Power Specifications

Type ATX: Vin, VSB; ST: Vin

Rated Voltage Vin: 8.5V (9V-5%) – 20V (19+5%): VSB: ± 5%

RTC Battery: 2.0 – 3.3V

2.11. Operating Requirements

Type ATX: Vin, VSB; ST: Vin

Rated Voltage Vin: 8.5V (9V-5%) – 20V (19+5%): VSB: ± 5%

RTC Battery: 2.0 – 3.3V

Power Consumption	For detail information about power consumption, please contacts our business representatives.

2.12. Environmental Requirements

Operating Temperature	Standard: 0°-60 °C (32 – 140°C)
	Extended: -40 °– 85 °C (-40° – 180°F)
Storage Temperature	-40 °– 85 °C (-40o – 180oF)
	60 °C @ 95% relative humidity, non-condensing
Humidity	5-90% RH operating, non-condensing
	5-95% RH storage (and operating with conformal coating).
Vibration Resistance	IEC 60068-2-64
Halt	Vibration Stress

2.13. Regulatory Compliance

Hazardous substance-Free (RoHS) Compliant

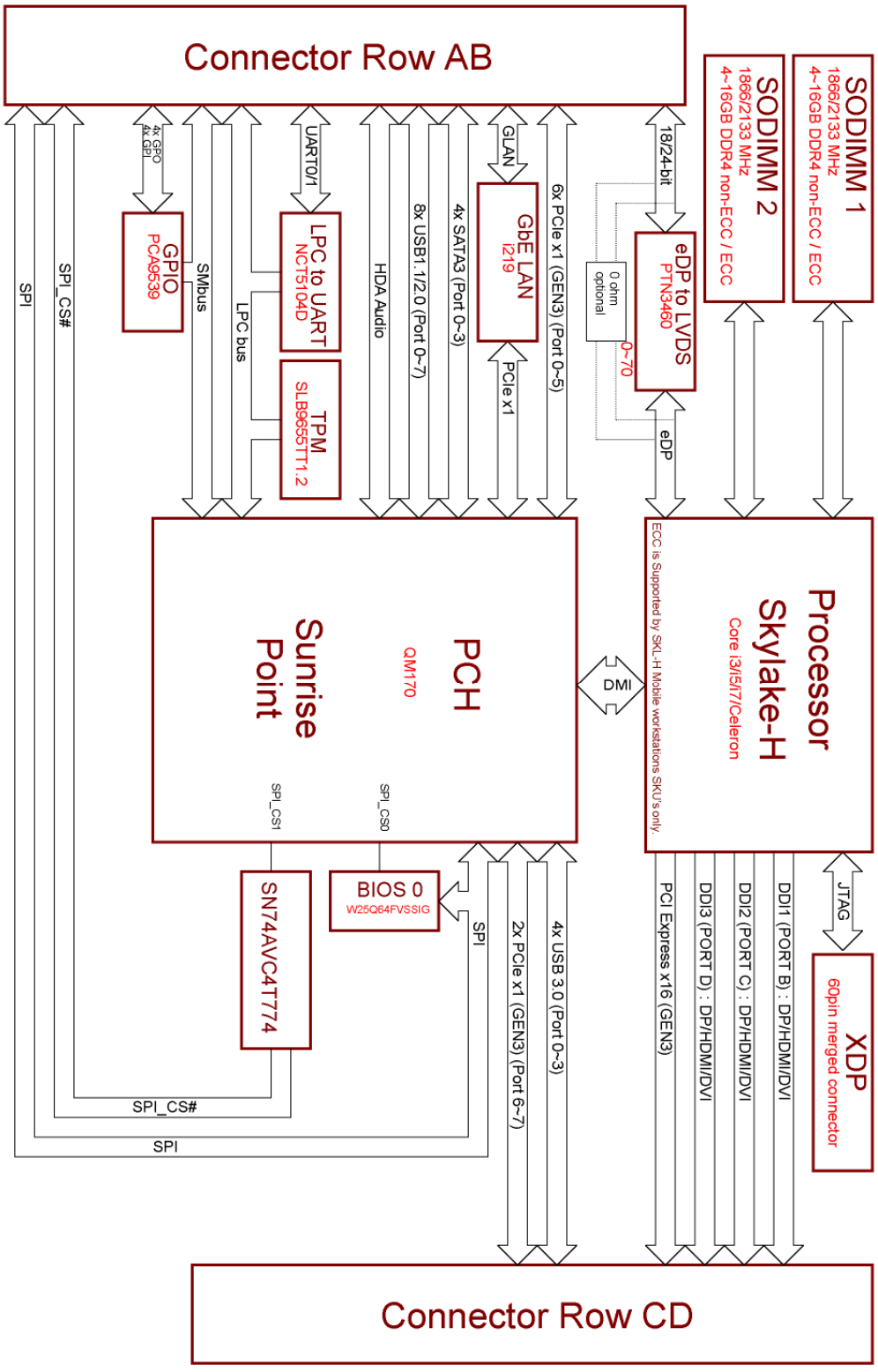
This product is designed and developed on hazardous substance-free components and parts and totally RoHS (Restriction of Hazardous Substances Directive 2002/95/EC) compliant.

2.15. Operating Systems

MB-73430 supports following operating systems:

- Red Hat® Enterprise 6.4
- Fedora® 20
- Microsoft® Windows 7 Professional 64 bit
- Microsoft® Windows® 7 Professional 32 bit
- Microsoft® Windows® 8.1 Professional 64 bit
- Windows® 10 Professional 64 bit

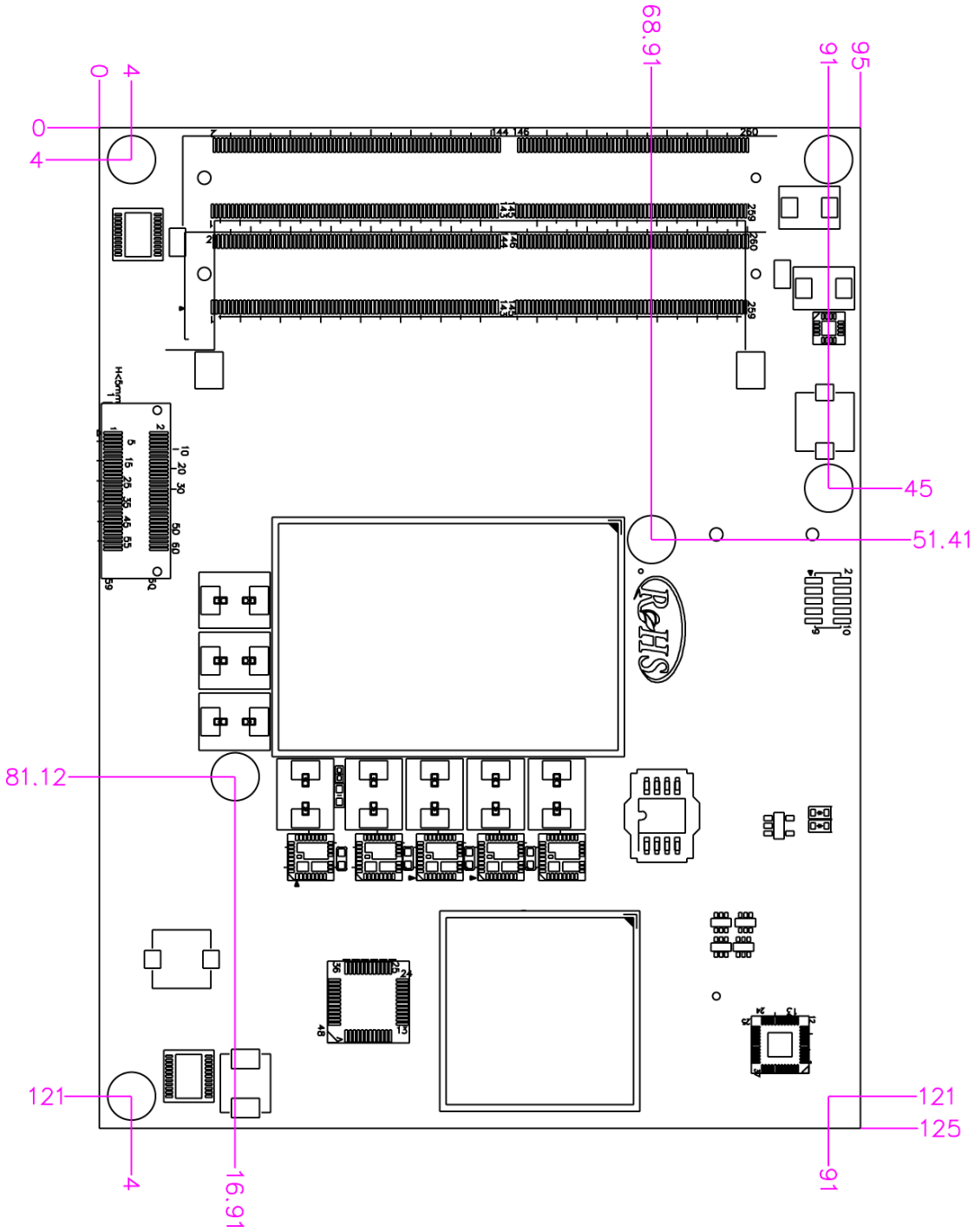
2.16. Functional Diagram

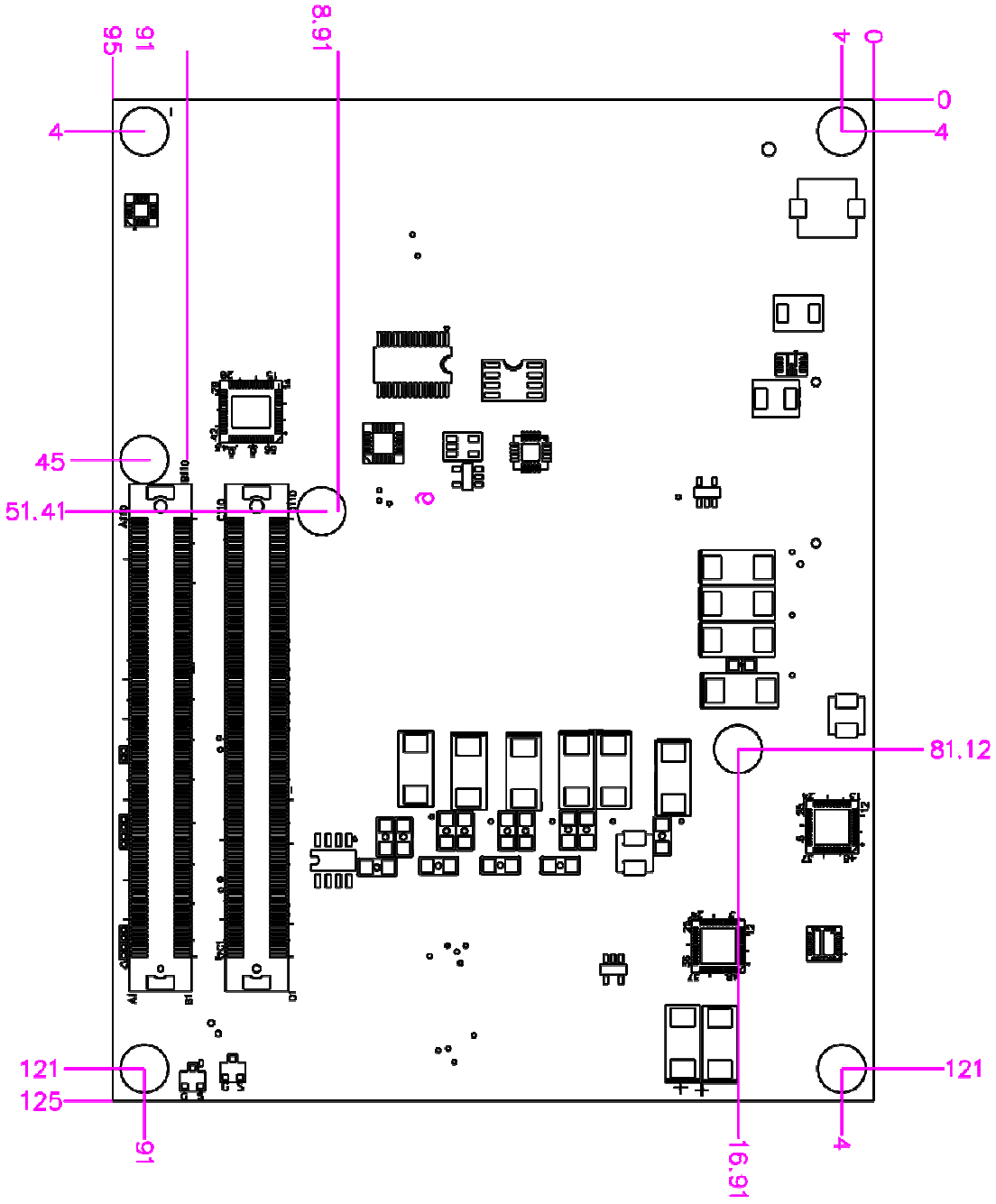


3. Mechanical Information

3.1 Mechanical Dimensions

Unit: mm

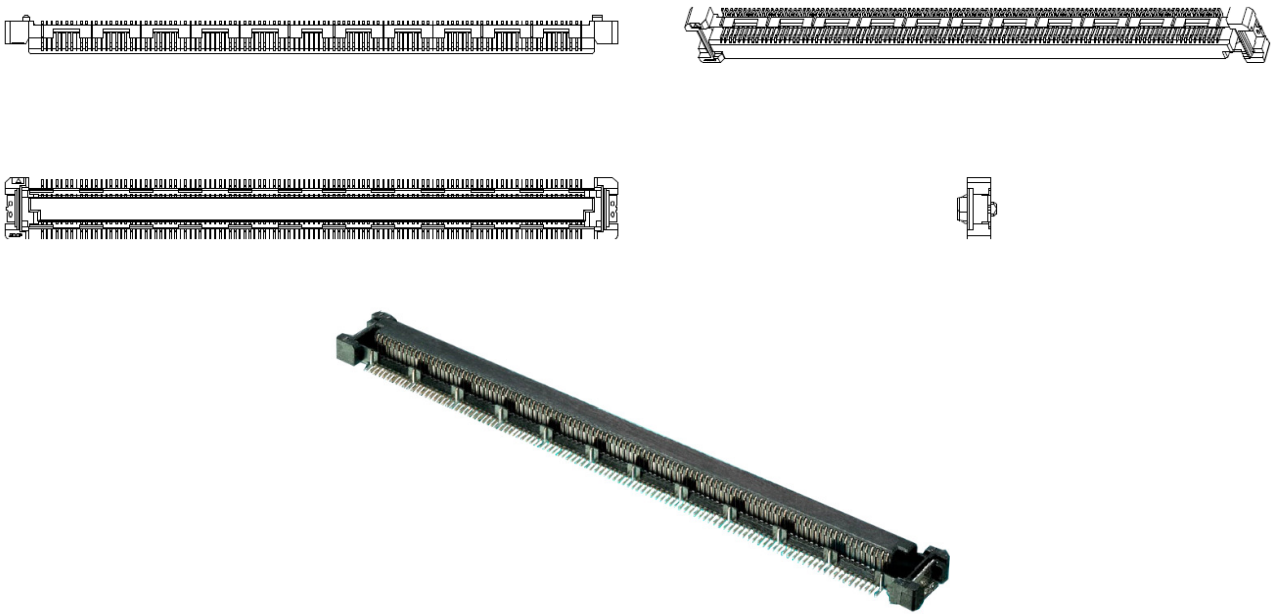




Unit: mm

3.2. Module Connector

The board-to-board connectors are 440-pin receptacles that are composed of 2 pieces of a 220-pin, 0.5 mm pitch receptacle.



Tyco 3-6318490-6

- 220-pin board-to-board connector with 0.5mm for a stacking height of 8 mm.
- This connector can be used with 8 mm through-hole standoffs (SMT type).

Common Specifications

- Current capacity: 0.5A per pin
- Rated voltage: 50 VAC
- Insulation resistance: 100M or greater @ 500 VDC
- Temperature rating: -40˚C ~ 85˚C
- UL certification (ECBT2.E28476)
- Copper alloy (contacts)
- Housing: thermo-plastic molded compound (L.C.P.)

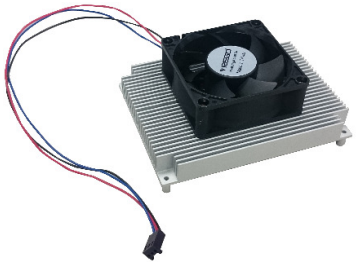
3.2. Thermal Solution (for reference only)

3.2.1. Heat Sink

It is recommended to use a heat sink or thermal fan as the thermal solution dependent on the actual application. Steps below are based on heat sinks, as an example.

3.2.2. Installation

Prepare parts below:



Heatsink assembly X 1

COM Express Carrier board X 1

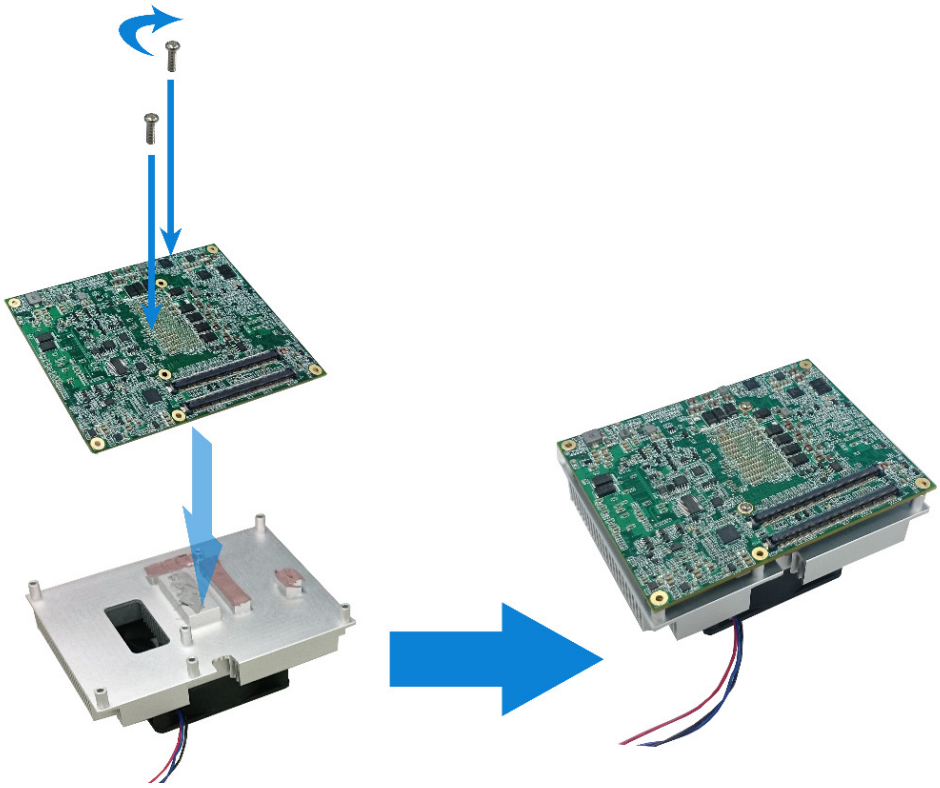
MB-COM Express EVAL

Fastening screws (M2.5, L = 8 mm) X 2

Fastening screws (M2.5, L = 16 mm) X 5

Step 1: Remove the protective film from the thermal pads.

Step 2: Align the mounting holes of the module, fit the module onto the heat thing by securing the two fastening screws (M2.5, L = 8 mm) as shown below.

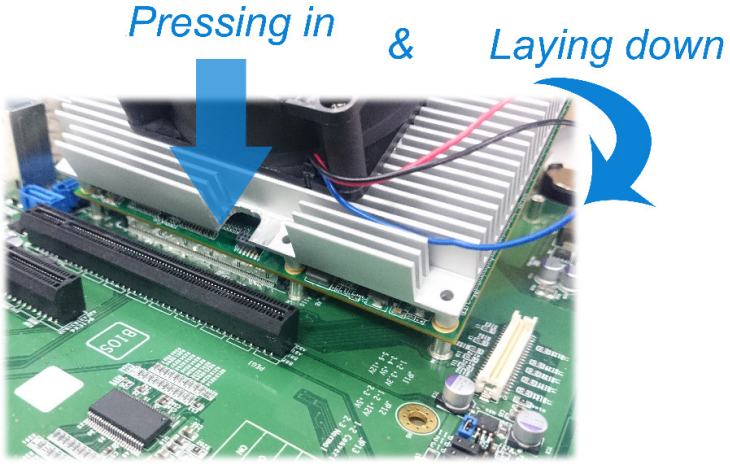


Step 3:

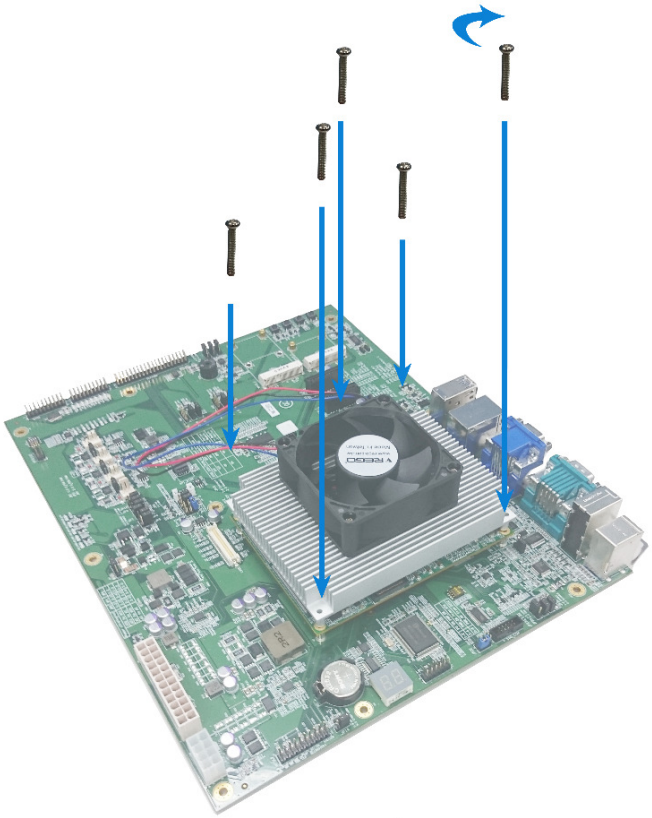
a. Tilt the heat sink assembly with the module and align the three studs of the module to the three studs of the carrier board.

b. Fit the heat sink assembly with the module by pressing where the arrow indicates.

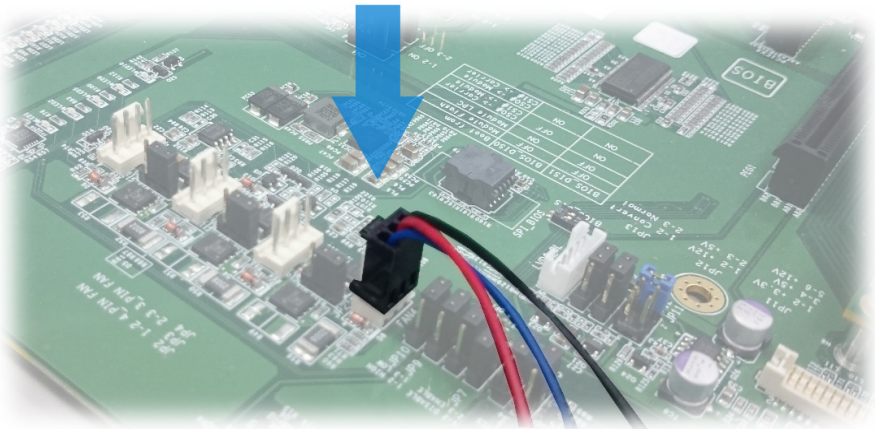
c. Lay down the heat sink assembly with the module.

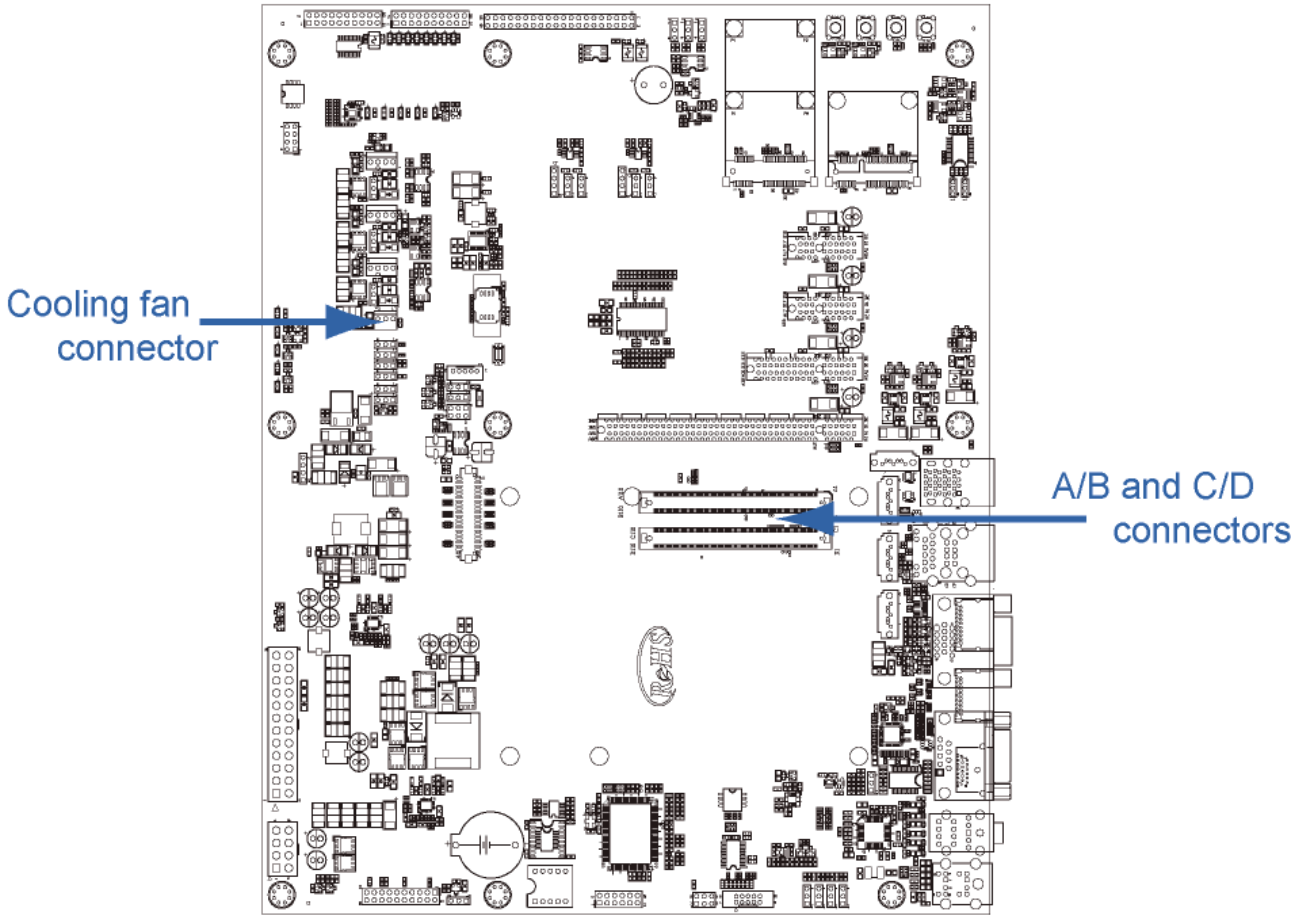


Step 4: Tighten the shipped five fastening screws (M2.5, L = 16 mm) to secure the module.



Step 5: Connect the power plug of the heat sink assembly..





3.3. Mounting Methods

3.3.1. Mechanical Specification

Dimensions

125.0 mm x 95.0 mm (4.92” x 3.75”)

Height

If a Module equips with a heat-spreader, the heat-spreader by itself does not constitute the complete thermal solution for a Module but provides a common interface between Modules and implementation-specific thermal solutions.

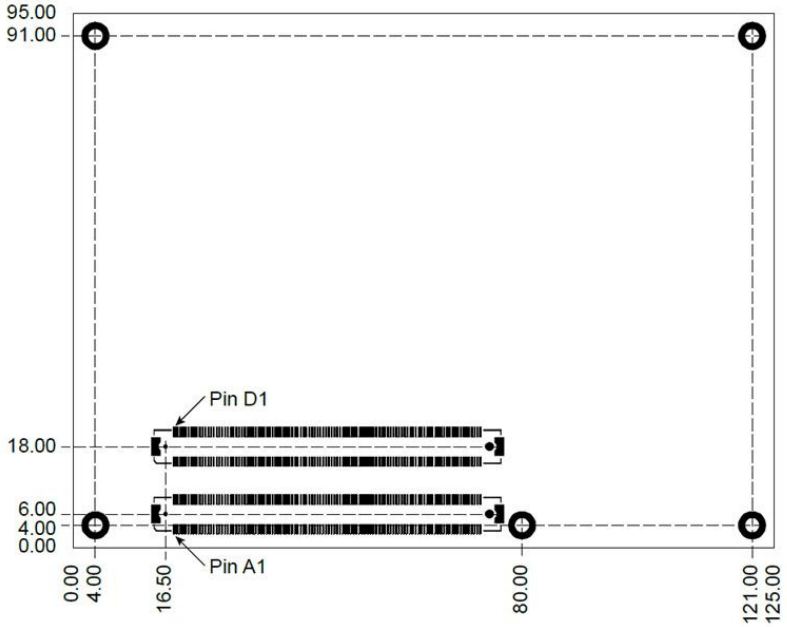
If implemented, a heat-spreader for the Basic form factor shall use an implementation specific set of holes and spacers to attach the heat-spreader to the Module. These implementation specific holes are

in addition to the Module mounting holes specified in below.

Module Size - Basic Module

The PCB size for the Basic Module shall be 125mm x 95mm. The PCB thickness should be 2mm to allow high layer count stack-ups and facilitate a standard “z” dimension between the Carrier Board and the top of the heat-spreader.

The holes shown in this drawing are intended for mounting the Module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers shall be used to attach the heat-spreader to the Module.



Unit: mm

Tolerances shall be ± 0.25mm [±0.010"], unless noted otherwise.

The 440 pin connector pair shall be mounted on the backside of the PCB and is seen “through” the board in this view.

The five mounting holes shown shall use 6mm diameter pads and shall have 2.7mm plated holes, for use with 2.5mm hardware. The pads shall be tied to the PCB ground plane.

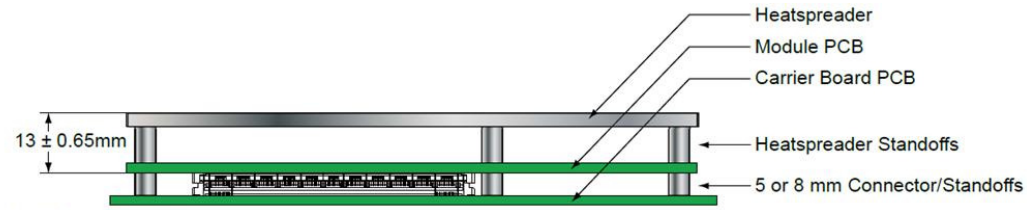
Modules shall include the 5 mounting holes as shown in Figure 6-3 above. These holes are primarily used to attach the Module to the Carrier.

For the Basic form factor a heat-spreader should not use the Module mounting holes as the only attachment points to a Module. The intent is to be able to provide a Module and heat-spreader as an assembly that can then be mounted to a Carrier without having to break the thermal interface between

the Module components and the heat-spreader.

The standoffs should be mounted on the Carrier Board. The height of the standoff is dependent on the stack height of the Carrier Board connector (5 mm or 8mm).
The overall Module height from the bottom surface of the Module board to the heat-spreader top surface shall be 13 mm for the Mini, the Compact, the Basic and the Extended Modules.

The Module PCB and heat-spreader plate thickness are vendor implementation specific, however, a 2 mm PCB with a 3 mm heat-spreader may be used which allows use of readily available standoffs.



All dimensions in mm.

Tolerances (unless otherwise specified):

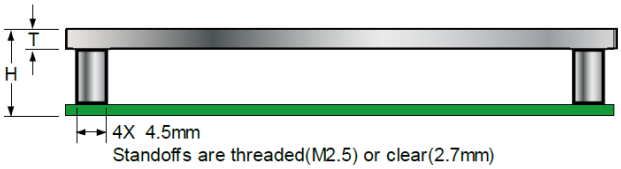
Z (height) dimensions should be ± 0.8mm [±0.031”] from top of Carrier Board to top of heatspreader.

Heat-spreader surface should be flat within 0.2mm [.008"] after assembly.

Interface surface finish should have a maximum roughness average (Ra) of 1.6μm [63μin].

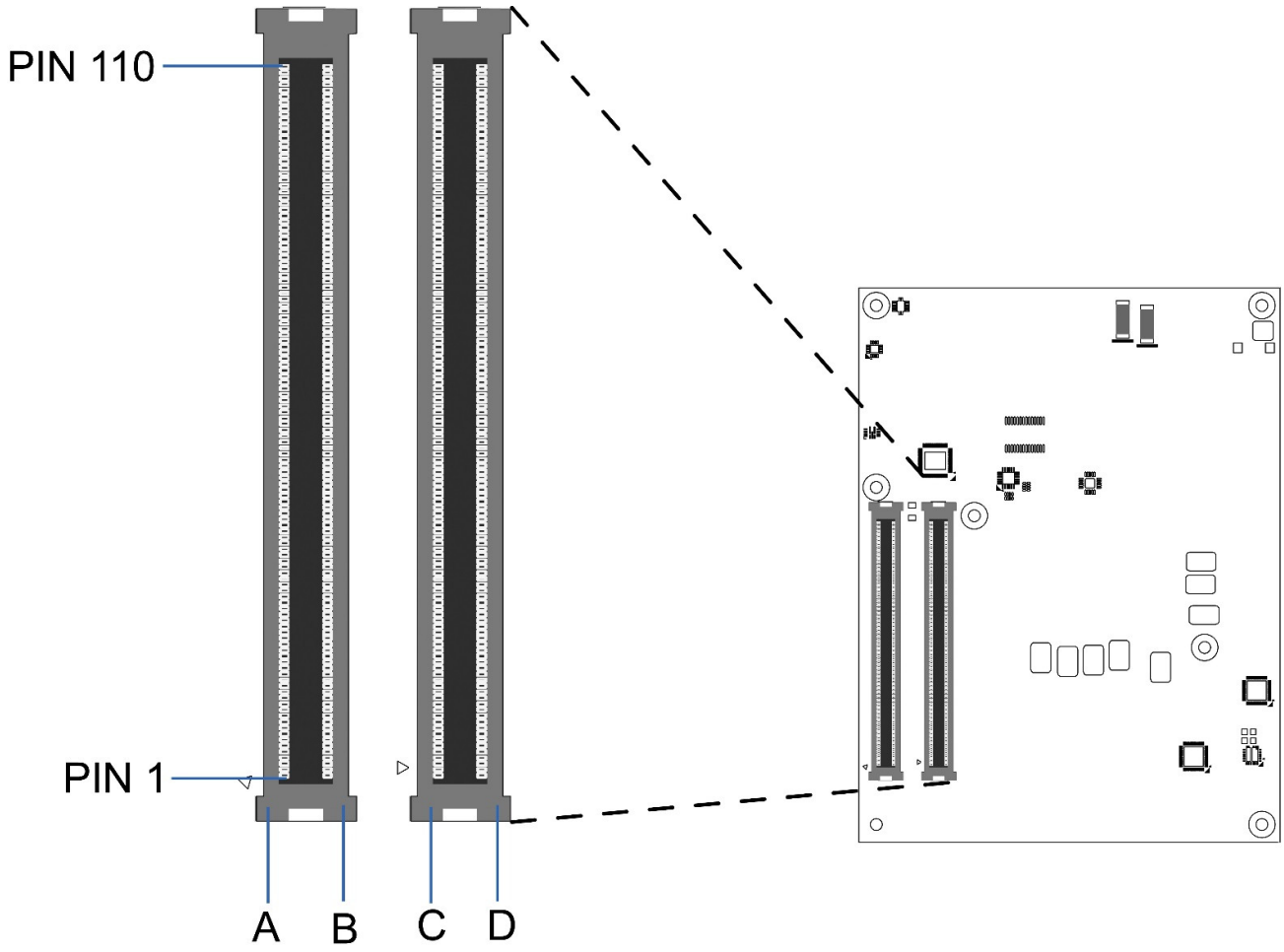
The critical dimension in Figure 6-10 is the Module PCB bottom side to heat-spreader topside. This dimension shall be 13.00mm ± 0.65mm [±0.026”].

Figure below shows a cross section of a Module and heat-spreader assembled to a Carrier Board using the 5mm stack height option. If 8mm Carrier Board connectors are used, the overall assembly height increases from 18.00mm to 21.00mm.



Thickness ´T´ is implemantation specific and may be 3mm.
Height 'H' (which includes PCB thickness) shall be 13.00mm

4. Pinout Definitions



4.1. Connector A/B

PIN	Row A	PIN	Row B
A1	**GND (FIXED)**	B1	**GND (FIXED)**
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK#	B8	LPC_DRQ0#

A9	GBE0_MDI1-	B9	LPC_DRQ1#
A10	GBE0_MDI1+	B10	LPC_CLK
A11	**GND (FIXED)**	B11	**GND (FIXED)**
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	GBE0_CTREF	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	SUS_STAT#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	**GND (FIXED)**	B21	**GND (FIXED)**
A22	SATA2_TX+	B22	SATA3_TX+
A23	SATA2_TX-	B23	SATA3_TX-
A24	SUS_S5#	B24	PWR_OK
A25	SATA2_RX+	B25	SATA3_RX+
A26	SATA2_RX-	B26	SATA3_RX-
A27	BATLOW#	B27	WDT
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1
A30	AC/HDA_RST	B30	AC/HDA_SDIN0
A31	**GND (FIXED)**	B31	**GND (FIXED)**
A32	AC/HDA_BITCLK	B32	SPKR
A33	AC/HDA_SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	**GND (FIXED)**	**B41**	**GND (FIXED)**
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#

A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	EXCD1_PERST#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#
A49	EXCD0_CPPE#	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	**GND (FIXED)**	B51	**GND (FIXED)**
A52	PCIE_TX5+	B52	PCIE_RX5+
A53	PCIE_TX5-	B53	PCIE_RX5-
A54	GPI0/SD_DATA0	B54	GPO1/SD_CMD
A55	PCIE_TX4+	B55	PCIE_RX4+
A56	PCIE_TX4-	B56	PCIE_RX4-
A57	GND	B57	GPO2/SD_WP
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	**GND (FIXED)**	B60	**GND (FIXED)**
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1/SD_DATA1	B63	GPO3/SD_CD#
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	**GND**	B66	WAKE0#
A67	GPI2/SD_DATA2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	**GND (FIXED)**	B70	**GND (FIXED)**
A71	LVDS_A0+ /eDP_TX2+	B71	LVDS_B0+
A72	LVDS_A0- / eDP_TX2-	B72	LVDS_B0-
A73	LVDS_A1+ / eDP_TX1+	B73	LVDS_B1+
A74	LVDS_A1- / eDP_TX1-	B74	LVDS_B1-
A75	LVDS_A2+ / eDP_TX0+	B75	LVDS_B2+
A76	LVDS_A2- / eDP_TX0-	B76	LVDS_B2-
A77	LVDS_VDD_EN / eDP_VDD_EN	B77	LVDS_B3+
A78	LVDS_A3+	B78	LVDS_B3-
A79	LVDS_A3-	B79	LVDS_BKLT_EN / eDP_BKLT_EN
A80	**GND (FIXED)**	B80	**GND (FIXED)**

A81	LVDS_A_CK+ / eDP_TX3+	B81	LVDS_B_CK+
A82	LVDS_A_CK- / eDP_TX3-	B82	LVDS_B_CK-
A83	LVDS_I2C_CK / eDP_AUX+	B83	LVDS_BKLT_CTRL / eDP_BKLT_CTRL
A84	LVDS_I2C_DAT / eDP_AUX-	B84	VCC_5V_SBY
A85	GPI3/SD_DATA3	B85	VCC_5V_SBY
A86	RSVD	B86	VCC_5V_SBY
A87	eDP_HPD	B87	VCC_5V_SBY
A88	PCIE_CLK_REF+	B88	BIOS_DIS1#
A89	PCIE_CLK_REF-	B89	VGA_RED
A90	**GND (FIXED)**	B90	**GND (FIXED)**
A91	SPI_POWER	B91	VGA_GRN
A92	SPI_MISO	B92	VGA_BLU
A93	GPO0/SD_CLK	B93	VGA_HSYNC
A94	SPI_CLK	B94	VGA_VSYNC
A95	SPI_MOSI	B95	VGA_I2C_CK
A96	TPM_PP	B96	VGA_I2C_DAT
A97	TYPE10#	B97	SPI_CS#
A98	SER0_TX	B98	RSVD
A99	SER0_RX	B99	RSVD
A100	**GND (FIXED)**	B100	**GND (FIXED)**
A101	SER1_TX / CAN_TX	B101	FAN_PWMOUT
A102	SER1_RX / CAN_RX	B102	FAN_TACHIN
A103	LID#	B103	SLEEP#
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	**GND (FIXED)**	B110	**GND (FIXED)**

4.1. Connector C/D

PIN	Row C	PIN	Row D
C1	**GND (FIXED)**	D1	**GND (FIXED)**
C2	GND	D2	GND

PIN	Row C	PIN	Row D
C3	USB_SSRX0-	D3	USB_SSTX0-
C4	USB_SSRX0+	D4	USB_SSTX0+
C5	GND	D5	GND
C6	USB_SSRX1-	D6	USB_SSTX1-
C7	USB_SSRX1+	D7	USB_SSTX1+
C8	GND	D8	GND
C9	USB_SSRX2-	D9	USB_SSTX2-
C10	USB_SSRX2+	D10	USB_SSTX2+
C11	**GND (FIXED)**	D11	**GND (FIXED)**
C12	USB_SSRX3-	D12	USB_SSTX3-
C13	USB_SSRX3+	D13	USB_SSTX3+
C14	**GND (FIXED)**	D14	**GND (FIXED)**
C15	DDI1_PAIR6+	D15	DDI1_CTRLCLK_AUX+
C16	DDI1_PAIR6-	D16	DDI1_CTRLDATA_AUX-
C17	RSVD	D17	RSVD
C18	RSVD	D18	RSVD
C19	PCIE_RX6+	D19	PCIE_TX6+
C20	PCIE_RX6-	D20	PCIE_TX6-
C21	**GND (FIXED)**	D21	**GND (FIXED)**
C22	PCIE_RX7+	D22	PCIE_TX7+
C23	PCIE_RX7-	D23	PCIE_TX7-
C24	DDI1_HPD	D24	RSVD
C25	DDI1_PAIR4+	D25	RSVD
C26	DDI1_PAIR4-	D26	DDI1_PAIR0+
C27	RSVD	D27	DDI1_PAIR0-
C28	RSVD	D28	RSVD
C29	DDI1_PAIR5+	D29	DDI1_PAIR1+
C30	DDI1_PAIR5-	D30	DDI1_PAIR1-
C31	**GND (FIXED)**	D31	**GND (FIXED)**
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL
C35	RSVD	D35	RSVD
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+
C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-

PIN	Row C	PIN	Row D
C38	DDI3_DDC_AUX_SEL	D38	RSVD
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+
C40	DDI3_PAIR0-	D40	DDI2_PAIR0-
C41	**GND (FIXED)**	D41	**GND (FIXED)**
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+
C43	DDI3_PAIR1-	D43	DDI2_PAIR1-
C44	DDI3_HPD	D44	DDI2_HPD
C45	RSVD	D45	RSVD
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-
C48	RSVD	D48	RSVD
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+
C50	DDI3_PAIR3-	D50	DDI2_PAIR3-
C51	**GND (FIXED)**	D51	**GND (FIXED)**
C52	PEG_RX0+	D52	PEG_TX0+
C53	PEG_RX0-	D53	PEG_TX0-
C54	TYPE0#	D54	PEG_LANE_RV#
C55	PEG_RX1+	D55	PEG_TX1+
C56	PEG_RX1-	D56	PEG_TX1-
C57	TYPE1#	D57	TYPE2#
C58	PEG_RX2+	D58	PEG_TX2+
C59	PEG_RX2-	D59	PEG_TX2-
C60	**GND (FIXED)**	D60	**GND (FIXED)**
C61	PEG_RX3+	D61	PEG_TX3+
C62	PEG_RX3-	D62	PEG_TX3-
C63	RSVD	D63	RSVD
C64	RSVD	D64	RSVD
C65	PEG_RX4+	D65	PEG_TX4+
C66	PEG_RX4-	D66	PEG_TX4-
C67	RSVD	D67	GND
C68	PEG_RX5+	D68	PEG_TX5+
C69	PEG_RX5-	D69	PEG_TX5-
C70	GND (FIXED)	D70	GND (FIXED)
C71	PEG_RX6+	D71	PEG_TX6+
C72	PEG_RX6-	D72	PEG_TX6-

PIN	Row C	PIN	Row D
C73	**GND (FIXED)**	D73	**GND (FIXED)**
C74	PEG_RX7+	D74	PEG_TX7+
C75	PEG_RX7-	D75	PEG_TX7-
C76	GND	D76	GND
C77	RSVD	D77	RSVD
C78	PEG_RX8+	D78	PEG_TX8+
C79	PEG_RX8-	D79	PEG_TX8-
C80	**GND (FIXED)**	D80	**GND (FIXED)**
C81	PEG_RX9+	D81	PEG_TX9+
C82	PEG_RX9-	D82	PEG_TX9-
C83	RSVD	D83	RSVD
C84	GND	D84	GND
C85	PEG_RX10+	D85	PEG_TX10+
C86	PEG_RX10-	D86	PEG_TX10-
C87	GND	D87	GND
C88	PEG_RX11+	D88	PEG_TX11+
C89	PEG_RX11-	D89	PEG_TX11-
C90	**GND (FIXED)**	D90	**GND (FIXED)**
C91	PEG_RX12+	D91	PEG_TX12+
C92	PEG_RX12-	D92	PEG_TX12-
C93	**GND (FIXED)**	D93	**GND (FIXED)**
C94	PEG_RX13+	D94	PEG_TX13+
C95	PEG_RX13-	D95	PEG_TX13-
C96	**GND (FIXED)**	D96	**GND (FIXED)**
C97	RSVD	D97	RSVD
C98	PEG_RX14+	D98	PEG_TX14+
C99	PEG_RX14-	D99	PEG_TX14-
C100	GND (FIXED)	D100	GND (FIXED)
C101	PEG_RX15+	D101	PEG_TX15+
C102	PEG_RX15-	D102	PEG_TX15-
C103	**GND (FIXED)**	D103	**GND (FIXED)**
C104	VCC_12V	D104	VCC_12V
C105	VCC_12V	D105	VCC_12V
C106	VCC_12V	D106	VCC_12V
C107	VCC_12V	D107	VCC_12V

PIN	Row C	PIN	Row D
C108	VCC_12V	D108	VCC_12V
C109	VCC_12V	D109	VCC_12V
C110	**GND (FIXED)**	D110	**GND (FIXED)**

4.2. Signal Definitions

Followings are definition for signal on connectors A/B and C/D.

I	Input signal to the module
O	Output signal from the module
I/O	Bi-directional input/output signal
OD	Open drain output
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	3.3V output signal
O 5V	5V output signal
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O 3.3Vsb	Input 3.3V tolerant active in standby state
P	Power Input/Output
REF	Reference voltage output that may be sourced from a module power plane.
PDS	Pull-down strap. This is an output pin on the module that is either tied to GND or not connected. The signal is used to indicate the PICMG module type to the Carrier Board.
PU	pull-up resistor on module
PD	pull-down resistor on module

4.3. Signal Descriptions – Connector A/B

4.3.1. Audio Signals

Signal	Pin	Description	I/O	PU/PD	Comment
AC/HDA_SYNC	A29	Sample-synchronization signal to the CODEC (s).	O 3.3V		
AC/HDA_RST#	A30	Reset output to CODEC, active low.	O 3.3V		
AC/HDA_BITCLK	A32	Serial data clock generated by the external CODEC(s).	O 3.3V		
AC/HDA_SDOUT	A33	Serial TDM data output to the CODEC.	O 3.3V		
AC/HDA_SDIN2	B28	Serial TDM data inputs from up to 3 CODECs.	I 3.3V		not connected
AC/HDA_SDIN1	B29		I 3.3V		
AC/HDA_SDIN0	B30		I 3.3V		

4.3.2. Analog VGA

Signal	Pin	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	O Analog		not supported
VGA_GRN	B91	Green for monitor Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		not supported
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		not supported
VGA_HSYNC	B93	Horizontal sync output to VGA monitor.	O 3.3V		not supported
VGA_VSYNC	B94	Vertical sync output to VGA monitor.	O 3.3V		not supported
VGA_I2C_CK	B95	DDC clock line (I2C port dedicated to identify VGA monitor capabilities).	O 3.3V		not supported
VGA_I2C_DAT	B96	DDC data line.	I/O 3.3V		not supported

4.3.3. LVDS

Signal	Pin	Description	I/O	PU/PD	Comment
LVDS_A0+ / eDP_TX2+	A71	LVDS Channel A differential pairs.	O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_A0- / eDP_TX2-	A72		O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.

Signal	Pin	Description	I/O	PU/PD	Comment
LVDS_A1+ / eDP_TX1+	A73		O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_A1- / eDP_TX1-	A74		O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_A2+ / eDP_TX0+	A75		O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_A2- / eDP_TX0-	A76		O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_A3+	A78		O LVDS		
LVDS_A3-	A79		O LVDS		
LVDS_VDD_EN / eDP_VDD_EN	A77	LVDS panel power enable.	O 3.3V	PD, 100K	LVDS/eDP BOM optional. The default is LVDS.
LVDS_A_CK+ / eDP_TX3+	A81	LVDS Channel B differential clock.	O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_A_CK- / eDP_TX3-	A82		O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_I2C_CK / eDP_AUX+	A83	DDC lines used for flat panel detection and control.	O OD 3.3V	PU, 2.2K, 3.3V	LVDS/eDP BOM optional. The default is LVDS.
LVDS_I2C_DAT / eDP_AUX-	A84	DDC lines used for flat panel detection and control.	I/O OD 3.3V	PU, 2.2K, 3.3V	LVDS/eDP BOM optional. The default is LVDS.
LVDS_B0+	B71	LVDS Channel B differential pairs.	O LVDS		
LVDS_B0-	B72		O LVDS		
LVDS_B1+	B73		O LVDS		
LVDS_B1-	B74		O LVDS		
LVDS_B2+	B75		O LVDS		
LVDS_B2-	B76		O LVDS		
LVDS_B3+	B77		O LVDS		

Signal	Pin	Description	I/O	PU/PD	Comment
LVDS_B3-	B78		O LVDS		
LVDS_BKLT_EN / eDP_BKLT_EN	B79	LVDS panel backlight enable.	O 3.3V	PD, 100K	
LVDS_B_CK+	B81	LVDS Channel B differential clock.	O LVDS		
LVDS_B_CK-	B82		O LVDS		
LVDS_BKLT_CTRL / eDP_BKLT_CTRL	B83	LVDS panel backlight brightness control.	O 3.3V		

4.3.4. eDP

Signal	Pin	Description	I/O	PU/PD	Comment
LVDS_A0+ / eDP_TX2+	A71	eDP differential pairs.	O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_A0- / eDP_TX2-	A72		O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_A1+ / eDP_TX1+	A73		O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_A1- / eDP_TX1-	A74		O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_A2+ / eDP_TX0+	A75		O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_A2- / eDP_TX0-	A76		O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_VDD_EN / eDP_VDD_EN	A77	eDP power enable.	O 3.3V	PD, 100K	LVDS/eDP BOM optional. The default is LVDS.
LVDS_A_CK+ / eDP_TX3+	A81	eDP differential pairs.	O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_A_CK- / eDP_TX3-	A82		O LVDS O eDP		LVDS/eDP BOM optional. The default is LVDS.
LVDS_I2C_CK / eDP_AUX+	A83	eDP AUX+	O OD 3.3V	PU, 2.2K, 3.3V	LVDS/eDP BOM optional. The default is LVDS.
LVDS_I2C_DAT / eDP_AUX-	A84	eDP AUX-	I/O OD3.3V	PU, 2.2K, 3.3V	LVDS/eDP BOM optional. The default is LVDS.
eDP_HPD	A87	Detection of Hot Plug / Unplug and notification ofthe link layer.	I 3.3V	PD, 100K	BOM optional. The default is NC.

LVDS_BKLT_EN / eDP_BKLT_EN	B79	eDP backlight enable.	O3.3V	PD, 100K
LVDS_BKLT_CTRL / eDP_BKLT_CTRL	B83	eDP backlight brightness control.	O3.3V	

4.3.5. Gigabit Ethernet

Signal	Pin	Description	I/O	PU/PD	Comment
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB		
GBE0_MDI0-	A12	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following:	I/O Analog		
GBE0_MDI0+	A13		I/O Analog		
GBE0_MDI1-	A9		I/O Analog		
GBE0_MDI1+	A10		I/O Analog		
GBE0_MDI2-	A6		I/O Analog		
GBE0_MDI2+	A7		I/O Analog		
GBE0_MDI3-	A2		I/O Analog		
GBE0_MDI3+	A3		I/O Analog		

	1000BASE-T	100BASE-TX	10BASE-T
MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
MDI[2]+/-	B1_DC+/-		
MDI[3]+/-	B1_DD+/-		

This set of differential pairs, in conjunction with the GBE1_MDI[0:3] pairs, may also be used to implement a 10 Gigabit / sec interface, as described in

Signal	Pin	Description	I/O	PU/PD	Comment
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.			not connected
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	O 3.3VSB		

4.3.6. SATA

Signal	Pin	Description	I/O	PU/PD	Comment
SATA0_TX+	A16	Serial ATA or SAS Channel 0 transmit differential pair.	O SATA		Supports SATA 3.0
SATA0_TX-	A17		O SATA		Supports SATA 3.0
SATA0_RX+	A19	Serial ATA or SAS Channel 0 receive differential pair.	I SATA		Supports SATA 3.0
SATA0_RX-	A20		I SATA		Supports SATA 3.0
SATA1_TX+	B16	Serial ATA or SAS Channel 1 transmit differential pair.	O SATA		Supports SATA 3.0
SATA1_TX-	B17		O SATA		Supports SATA 3.0
SATA1_RX+	B19	Serial ATA or SAS Channel 1 receive differential pair.	I SATA		Supports SATA 3.0
SATA1_RX-	B20		I SATA		Supports SATA 3.0
SATA2_TX+	A22	Serial ATA or SAS Channel 2 transmit differential pair.	O SATA		Supports SATA 3.0
SATA2_TX-	A23		O SATA		Supports SATA 3.0
SATA2_RX+	A25	Serial ATA or SAS Channel 2 receive differential	I		Supports SATA 3.0

Signal	Pin	Description	I/O	PU/PD	Comment
			SATA		
SATA2_RX-	A26	pair.	I SATA		Supports SATA 3.0
SATA3_TX+	B22	Serial ATA or SAS Channel 3 transmit differential	O SATA		Supports SATA 3.0
SATA3_TX-	B23	pair.	O SATA		Supports SATA 3.0
SATA3_RX+	B25	Serial ATA or SAS Channel 3 receive differential	I SATA		Supports SATA 3.0
SATA3_RX-	B26	pair.	I SATA		Supports SATA 3.0
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	I/O 3.3V	PU, 10K, 3.3VSB	

4.3.7. PCI Express

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_TX0+	A68	PCI Express channel 0, Transmit Output	O PCIE		Supports PCI-E GEN3.0
PCIE_TX0-	A69	differential pair.	O PCIE		Supports PCI-E GEN3.0
PCIE_RX0+	B68	PCI Express channel 0, Receive Input	I PCIE		Supports PCI-E GEN3.0
PCIE_RX0-	B69	differential pair.	I PCIE		Supports PCI-E GEN3.0
PCIE_TX1+	A64	PCI Express channel 1, Transmit Output	O PCIE		Supports PCI-E GEN3.0
PCIE_TX1-	A65	differential pair.	O PCIE		Supports PCI-E GEN3.0
PCIE_RX1+	B64	PCI Express channel 1, Receive Input	I PCIE		Supports PCI-E GEN3.0
PCIE_RX1-	B65	differential pair.	I PCIE		Supports PCI-E GEN3.0
PCIE_TX2+	A61	PCI Express channel 2, Transmit Output	O PCIE		Supports PCI-E GEN3.0
PCIE_TX2-	A62	differential pair.	O		Supports PCI-E GEN3.0

Signal	Pin	Description	I/O	PU/PD	Comment
			PCIE		
PCIE_RX2+	B61	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI-E GEN3.0
PCIE_RX2-	B62		I PCIE		Supports PCI-E GEN3.0
PCIE_TX3+	A58	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI-E GEN3.0
PCIE_TX3-	A59		O PCIE		Supports PCI-E GEN3.0
PCIE_RX3+	B58	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI-E GEN3.0
PCIE_RX3-	B59		I PCIE		Supports PCI-E GEN3.0
PCIE_TX4+	A55	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Supports PCI-E GEN3.0
PCIE_TX4-	A56		O PCIE		Supports PCI-E GEN3.0
PCIE_RX4+	B55	PCI Express channel 4, Receive Input differential pair.	I PCIE		Supports PCI-E GEN3.0
PCIE_RX4-	B56		I PCIE		Supports PCI-E GEN3.0
PCIE_TX5+	A52	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Supports PCI-E GEN3.0
PCIE_TX5-	A53		O PCIE		Supports PCI-E GEN3.0
PCIE_RX5+	B52	PCI Express channel 5, Receive Input differential pair.	I PCIE		Supports PCI-E GEN3.0
PCIE_RX5-	B53		I PCIE		Supports PCI-E GEN3.0
PCIE_CLK_REF+	A88	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if the design involves more than one PCI Express device.
PCIE_CLK_REF-	A89		O PCIE		

4.3.8. Express Card

Signal	Pin	Description	I/O	PU/PD	Comment
EXCD0_PERST#	A48	PCI Express Card: reset.	O 3.3V		
EXCD1_PERST#	B47		O 3.3V		
EXCD0_CPPE#	A49	PCI Express Card: PCI Express capable card request.	I 3.3V	PU, 10K, 3.3V	
EXCD1_CPPE#	B48		I 3.3V	PU, 10K, 3.3V	

4.3.9. LPC Bus

Signal	Pin	Description	I/O	PU/PD	Comment
LPC_SERIRQ	A50	LPC serial interrupt.	I OD 3.3V	PU, 10K, 3.3V	
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle.	O 3.3V		
LPC_AD0	B4	LPC multiplexed address, command and data bus.	I/O 3.3V		
LPC_AD1	B5		I/O 3.3V		
LPC_AD2	B6		I/O 3.3V		
LPC_AD3	B7		I/O 3.3V		
LPC_DRQ0#	B8	LPC serial DMA request.	I 3.3V		not connection
LPC_DRQ1#	B9		I 3.3V		not connection
LPC_CLK	B10	LPC clock output –33MHz nominal.	O 3.3V		

4.3.10. USB

Signal	Pin	Description	I/O	PU/PD	Comment
USB0-	A45	USB differential data pairs for Port 0	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0+	A46		I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB differential data pairs for Port 1	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46		I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB differential data pairs for Port 2	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43		I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB differential data pairs for Port 3	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43		I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB differential data pairs for Port 4	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40		I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5-	B39	USB differential data pairs for Port 5	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40		I/O		USB 2.0 compliant.

Signal	Pin	Description	I/O	PU/PD	Comment
					Backwards compatible to USB 1.1
USB6-	A36	USB differential data pairs for Port 6	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+	A37		I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7-	B36	USB differential data pairs for Port 7	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+	B37		I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low.	I 3.3VSB	PU, 10K, 3.3VSB	Do not pull this line high on the Carrier Board.
USB_2_3_OC#	A44	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low.	I 3.3VSB	PU, 10K, 3.3VSB	Do not pull this line high on the Carrier Board.
USB_4_5_OC#	B38	USB over-current sense, USB channels 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low.	I 3.3VSB	PU, 10K, 3.3VSB	Do not pull this line high on the Carrier Board.
USB_6_7_OC#	A38	USB over-current sense, USB channels 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low.	I 3.3VSB	PU, 10K, 3.3VSB	Do not pull this line high on the Carrier Board.

4.3.12. SPI (BIOS only)

Signal	Pin	Description	I/O	PU/PD	Comment
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU, 10K, 3.3VSB	Carrier shall be left as no-connect.
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module– nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier Board.	PWR3.3VSB		
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU, 10K, 3.3VSB	Carrier shall be left as no-connect.
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB		Carrier shall pull to SPI_POWER when external SPI is provided but not used.

4.3.13. Miscellaneous

Signal	Pin	Description	I/O	PU/PD	Comment
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU, 10K, 3.3VSB	

Signal	Pin	Description	I/O	PU/PD	Comment
TPM_PP	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD, 1K, if TPM on module	Modules implementing a TPM shall pull down TPM_PP
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PD, 10K	
SPKR	B32	Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.	O 3.3V		
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU, 10K, 3.3V	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD3.3V	PD, 100K	
FAN_TACHIN	B102	Fan tachometer input for a fan with a two pulse output.	I OD3.3V	PU, 10K, 3.3V	

4.3.14. SMBus

Signal	Pin	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line.	O OD 3.3VSB	PU, 8.2K, 3.3VSB	
SMB_DAT	B14	System Management Bus bidirectional data line.	I/O OD 3.3VSB	PU, 8.2K, 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.			

4.3.15. I2C Bus

Signal	Pin	Description	I/O	PU/PD	Comment

I2C_CK	B33	General purpose I2C port clock output.	I/O OD 3.3VSB	PU, 1K, 3.3VSB
I2C_DAT	B34	General purpose I2C port data I/O line.	I/O OD 3.3VSB	PU, 1K, 3.3VSB

4.3.16. General Purpose I/O (GPIO)

Signal	Pin	Description	I/O	PU/PD	Comment
GPI0/SD_DATA0	A54	General purpose input pins. Pulled high internally on the Module.	I 3.3V	PU, 10K, 3.3V	Support GPI
GPI1/SD_DATA1	A63		I 3.3V	PU, 10K, 3.3V	Support GPI
GPI2/SD_DATA2	A67		I 3.3V	PU, 10K, 3.3V	Support GPI
GPI3/SD_DATA3	A85		I 3.3V	PU, 10K, 3.3V	Support GPI
GPO0/SD_CLK	A93	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V	PU, 10K, 3.3V	Support GPO
GPO1/SD_CMD	B54		O 3.3V	PU, 10K, 3.3V	Support GPO
GPO2/SD_WP	B57		O 3.3V	PU, 10K, 3.3V	Support GPO
GPO3/SD_CD#	B63		O 3.3V	PU, 10K, 3.3V	Support GPO

4.3.17. Serial Interface Signals

Signal	Pin	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter.	O 3.3V		
SER0_RX	A99	General purpose serial port receiver.	I 3.3V	PU, 47K, 3.3V	
SER1_TX / CAN_TX	A101	General purpose serial port transmitter. This pin is shared with CAN_TX.	O 3.3V		Support SER1_TX
SER1_RX / CAN_RX	A102	General purpose serial port receiver This pin is shared with CAN_RX.	I 3.3V	PU, 47K, 3.3V	Support SER1_RX

4.3.18. Power and System Management

Signal	Pin	Description	I/O	PU/PD	Comment
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
PWRBTN#	B12	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.	I 3.3VSB	PU, 10K, 3.3VSB	
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.			
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or other configurable devices time to be programmed.	I 3.3V	PU, 10K, 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3VSB	PU, 10K, 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be	O 3.3V	PD, 100K	

Signal	Pin	Description	I/O	PU/PD	Comment
		initiated by the module software.			
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
BATLOW#	A27	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	I 3.3VSB	PU, 10K, 3.3VSB	
LID#	A103	LID switch. Low active signal used by the ACPI operating system for a LID switch.	I OD3.3VSB	PU, 10K, 3.3VSB	
WAKE0#	B66	PCI Express wake up signal	I 3.3VSB	PU, 1K, 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU, 1K, 3.3VSB	Connect WAKE0 together.
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3VSB	PU, 10K, 3.3VSB	

4.3.19. Power and Ground

Signal	Pin	Description	I/O	PU/PD	Comment
VCC_12V	A104	Primary power input: +12V nominal (wide range: 8.5V ~ 19V). All available VCC_12V pins on the connector(s) shall be used.	PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	A105		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	A106		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	A107		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	A108		PWR 12V		support voltage range from 19V to 8.5V

Signal	Pin	Description	I/O	PU/PD	Comment
VCC_12V	A109		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	B104		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	B105		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	B106	Primary power input: +12V nominal (wide range: 8.5V ~ 19V). All available VCC_12V pins on the connector(s) shall be used.	PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	B107		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	B108		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	B109		PWR 12V		support voltage range from 19V to 8.5V
VCC_5V_SBY	B84	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	PWR 5V		
VCC_5V_SBY	B85		PWR 5V		
VCC_5V_SBY	B86		PWR 5V		
VCC_5V_SBY	B87		PWR 5V		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	PWR		
GND (FIXED)	A1				
GND (FIXED)	A11				
GND (FIXED)	A21				
GND (FIXED)	A31				
GND (FIXED)	A41				
GND (FIXED)	A51				
GND	A57				
GND (FIXED)	A60	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.			
GND	A66				
GND (FIXED)	A70				
GND (FIXED)	A80				
GND (FIXED)	A90				

Signal	Pin	Description	I/O	PU/PD	Comment
GND (FIXED)	A100				
GND (FIXED)	A110				
GND (FIXED)	B1				
GND (FIXED)	B11				
GND (FIXED)	B21				
GND (FIXED)	B31				
GND (FIXED)	B41				
GND (FIXED)	B51				
GND (FIXED)	B60				
GND (FIXED)	B70				
GND (FIXED)	B80				
GND (FIXED)	B90				not supported
GND (FIXED)	B100				
GND (FIXED)	B110				

4.4. Signal Descriptions – Connector C/D

4.4.1. USB 3.0 Extension

Signal	Pin	Description	I/O	PU/PD	Comment
USB_SSTX0-	D3	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0.	O USB3.0		
USB_SSTX0+	D4		O USB3.0		
USB_SSRX0-	C3	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0.	I USB3.0		
USB_SSRX0+	C4		I USB3.0		
USB_SSTX1-	D6	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1.	O USB3.0		
USB_SSTX1+	D7		O USB3.0		
USB_SSRX1-	C6	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1.	I USB3.0		
USB_SSRX1+	C7		I USB3.0		
USB_SSTX2-	D9	Additional Transmit signal differential pairs for	O		

Signal	Pin	Description	I/O	PU/PD	Comment
			USB3.0		
USB_SSTX2+	D10	the SuperSpeed USB data path on USB2.	O USB3.0		
USB_SSRX2-	C9	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2.	I USB3.0		
USB_SSRX2+	C10		I USB3.0		
USB_SSTX3-	D12	Additional Transmit signal differential pairs for theSuperSpeed USB data path on USB3.	O USB3.0		
USB_SSTX3+	D13		O USB3.0		
USB_SSRX3-	C12	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3.	I USB3.0		
USB_SSRX3+	C13		I USB3.0		

4.4.2. PCI Express x1

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_TX6+	D19	PCI Express channel 6, Transmit Output differential pair.	O PCIE		
PCIE_TX6-	D20		O PCIE		
PCIE_RX6+	C19	PCI Express channel 6, Receive Input differential pair.	I PCIE		
PCIE_RX6-	C20		I PCIE		
PCIE_TX7+	D22	PCI Express channel 7, Transmit Output differential pair.	O PCIE		
PCIE_TX7-	D23		O PCIE		
PCIE_RX7+	C22	PCI Express channel 7, Receive Input differential pair.	I PCIE		
PCIE_RX7-	C23		I PCIE		

4.4.3. DDI Channels

DDI 1

Signal	Pin	Description	I/O	PU/PD	Comment
DDI1_HPD	C24	DDI1 Hot-Plug Detect	I 3.3V	PD, 100K	
DDI1_CTRLCLK_AUX+	D15	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high.	I/O PCIE (AUX+) I/O OD 3.3V (CLK)	PD, 100K	
DDI1_CTRLDATA_AUX-	D16	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high.	I/O PCIE (AUX-) I/O OD 3.3V (DATA)	PU, 100K, 3.3V	
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	I 3.3V	PD, 1M	
DDI1_PAIR0+	D26	DDI1 differential pairs	O PCIE		
DDI1_PAIR0-	D27		O PCIE		
DDI1_PAIR1+	D29		O PCIE		
DDI1_PAIR1-	D30		O PCIE		
DDI1_PAIR2+	D32		O		

Signal	Pin	Description	I/O	PU/PD	Comment
			PCIE		
DDI1_PAIR2-	D33		O PCIE		
DDI1_PAIR3+	D36		O PCIE		
DDI1_PAIR3-	D37		O PCIE		
DDI1_PAIR4+	C25		O PCIE		Not supported
DDI1_PAIR4-	C26		O PCIE		Not supported
DDI1_PAIR5+	C29		O PCIE		Not supported
DDI1_PAIR5-	C30		O PCIE		Not supported
DDI1_PAIR6+	C15		O PCIE		Not supported
DDI1_PAIR6-	C16		O PCIE		Not supported

DDI 2

Signal	Pin	Description	I/O	PU/PD	Comment
DDI2+A55:F66_HPD	D44	DDI2 Hot-Plug Detect	I 3.3V	PD, 100K	
DDI2_CTRLCLK_AUX+	C32	DP AUX+ function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE (AUX+) I/O OD 3.3V (CLK)	PD, 100K	
DDI2_CTRLDATA_AUX-	C33	DP AUX+ function if DDI2_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.	I/O PCIE (AUX-) I/O OD 3.3V (DATA)	PU, 100K, 3.3V	
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic	I 3.3V	PD, 1M	

Signal	Pin	Description	I/O	PU/PD	Comment
		ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.			
DDI2_PAIR0+	D39	DDI2 differential pairs	O PCIE		
DDI2_PAIR0-	D40		O PCIE		
DDI2_PAIR1+	D42		O PCIE		
DDI2_PAIR1-	D43		O PCIE		
DDI2_PAIR2+	D46		O PCIE		
DDI2_PAIR2-	D47		O PCIE		
DDI2_PAIR3+	D49		O PCIE		
DDI2_PAIR3-	D50		O PCIE		

DDI 3

Signal	Pin	Description	I/O	PU/PD	Comment
DDI3_HPD	C44	DDI3 Hot-Plug Detect	I 3.3V	PD, 100K	
DDI3_CTRLCLK_AUX+	C36	DP AUX+ function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high.	I/O PCIE (AUX+) I/O OD 3.3V (CLK)	PD, 100K	
DDI3_CTRLDATA_AUX-	C37	DP AUX+ function if DDI3_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high.	I/O PCIE (AUX-) I/O OD 3.3V (DATA)	PU, 100K, 3.3V	
DDI3_DDC_AUX_SEL	C38	Selects the function of	I	PD, 1M	

Signal	Pin	Description	I/O	PU/PD	Comment
		DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	3.3V		
DDI3_PAIR0+	C39	DDI3 differential pairs	O PCIE		
DDI3_PAIR0-	C40		O PCIE		
DDI3_PAIR1+	C42		O PCIE		
DDI3_PAIR1-	C43		O PCIE		
DDI3_PAIR2+	C46		O PCIE		
DDI3_PAIR2-	C47		O PCIE		
DDI3_PAIR3+	C49		O PCIE		
DDI3_PAIR3-	C50		O PCIE		

4.4.4. PCI Express Graphics x16 (PEG)

Signal	Pin	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics transmit differential pairs.	I PCIE		
PEG_RX0-	C53		I PCIE		
PEG_RX1+	C55		I PCIE		
PEG_RX1-	C56		I PCIE		

Signal	Pin	Description	I/O	PU/PD	Comment
PEG_RX2+	C58		I PCIE		
PEG_RX2-	C59		I PCIE		
PEG_RX3+	C61		I PCIE		
PEG_RX3-	C62		I PCIE		
PEG_RX4+	C65		I PCIE		
PEG_RX4-	C66		I PCIE		
PEG_RX5+	C68		I PCIE		
PEG_RX5-	C69		I PCIE		
PEG_RX6+	C71		I PCIE		
PEG_RX6-	C72		I PCIE		
PEG_RX7+	C74		I PCIE		
PEG_RX7-	C75		I PCIE		
PEG_RX8+	C78		I PCIE		
PEG_RX8-	C79		I PCIE		
PEG_RX9+	C81		I PCIE		
PEG_RX9-	C82		I PCIE		
PEG_RX10+	C85		I PCIE		
PEG_RX10-	C86		I PCIE		

Signal	Pin	Description	I/O	PU/PD	Comment
PEG_RX11+	C88		I PCIE		
PEG_RX11-	C89		I PCIE		
PEG_RX12+	C91		I PCIE		
PEG_RX12-	C92		I PCIE		
PEG_RX13+	C94		I PCIE		
PEG_RX13-	C95		I PCIE		
PEG_RX14+	C98		I PCIE		
PEG_RX14-	C99		I PCIE		
PEG_RX15+	C101		I PCIE		
PEG_RX15-	C102		I PCIE		
PEG_TX0+	D52	PCI Express Graphics transmit differential pairs.	O PCIE		
PEG_TX0-	D53		O PCIE		
PEG_TX1+	D55		O PCIE		
PEG_TX1-	D56		O PCIE		
PEG_TX2+	D58		O PCIE		
PEG_TX2-	D59		O PCIE		
PEG_TX3+	D61		O PCIE		
PEG_TX3-	D62		O PCIE		

Signal	Pin	Description	I/O	PU/PD	Comment
PEG_TX4+	D65		O PCIE		
PEG_TX4-	D66		O PCIE		
PEG_TX5+	D68		O PCIE		
PEG_TX5-	D69		O PCIE		
PEG_TX6+	D71		O PCIE		
PEG_TX6-	D72		O PCIE		
PEG_TX7+	D74		O PCIE		
PEG_TX7-	D75		O PCIE		
PEG_TX8+	D78		O PCIE		
PEG_TX8-	D79		O PCIE		
PEG_TX9+	D81		O PCIE		
PEG_TX9-	D82		O PCIE		
PEG_TX10+	D85		O PCIE		
PEG_TX10-	D86		O PCIE		
PEG_TX11+	D88		O PCIE		
PEG_TX11-	D89		O PCIE		
PEG_TX12+	D91		O PCIE		
PEG_TX12-	D92		O PCIE		

Signal	Pin	Description	I/O	PU/PD	Comment
PEG_TX13+	D94		O PCIE		
PEG_TX13-	D95		O PCIE		
PEG_TX14+	D98		O PCIE		
PEG_TX14-	D99		O PCIE		
PEG_TX15+	D101		O PCIE		
PEG_TX15-	D102		O PCIE		
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the Carrier board to reverse lane order.	I 3.3V		

4.4.5. Module Type Definition

Signal	Pin	Description				I/O	PU/PD	Comment
TYPE0#	C54	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10, these pins are not present (X).				PDS		
		TYPE2#	TYPE1#	TYPE0#				
TYPE1#	C57	X	X	X	Pin-out Type1	PDS		
		NC	NC	NC	Pin-out Type2			
		NC	NC	GND	Pin-out Type3 (no IDE)			
		NC	GND	NC	Pin-out Type4 (no PCI)			
		NC	GND	GND	Pin-out Type5 (no IDE, no PCI)			
		GND	NC	NC	Pin-out Type6 (no IDE, no PCI)			
TYPE2#	D57	The Carrier Board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible Module pin-out type is detected. The Carrier Board				PDS	PD, 0 ohm	

		logic may also implement a fault indicator such as an LED.			

4.4.6. Power and Ground

Signal	Pin	Description	I/O	PU/PD	Comment
VCC_12V	C104	Primary power input: +12V nominal (wide range: 8.5V ~ 19V).All available VCC_12V pins on the connector(s) shall be used.	PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	C105		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	C106		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	C107		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	C108		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	C109		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	D104	Primary power input: +12V nominal (wide range: 8.5V ~ 19V).All available VCC_12V pins on the connector(s) shall be used.	PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	D105		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	D106		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	D107		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	D108		PWR 12V		support voltage range from 19V to 8.5V
VCC_12V	D109		PWR 12V		support voltage range from 19V to 8.5V
GND FIXED)	C1	Ground - DC power and signal and AC signal return path.All available GND connector pins shall be used and tied to carrier board GND plane.			
GND (FIXED)	C11				
GND (FIXED)	C21				

Signal	Pin	Description	I/O	PU/PD	Comment
GND (FIXED)	C31				
GND (FIXED)	C41				
GND (FIXED)	C51				
GND (FIXED)	C60				
GND (FIXED)	C70				
GND	C76				
GND (FIXED)	C80				
GND	C84				
GND	C87				
GND (FIXED)	C90				
GND	C93				
GND	C96				
GND (FIXED)	C100				
GND	C103				
GND (FIXED)	C110				
GND FIXED)	D1				
GND (FIXED)	D11				
GND (FIXED)	D21				
GND (FIXED)	D31				
GND (FIXED)	D41				
GND (FIXED)	D51				

Signal	Pin	Description	I/O	PU/PD	Comment
GND (FIXED)	D60				
GND	D67				
GND (FIXED)	D70				
GND	D76				
GND (FIXED)	D80				
GND	D84				
GND	D87				
GND (FIXED)	D90				
GND	D93				
GND	D96				
GND (FIXED)	D100				
GND	D103				
GND (FIXED)	D110				

5. System Resources

5.1. System Memory Map

Address Range(decimal)	Address Range(hex)	Size	Description
(4GB-16MB)	FF000000 – FFFFFFFF	16 MB	High BIOS Area
(4GB-18MB) – (4GB-17MB-1)	FEE00000 – FEEFFFFF	1 MB	MSI Interrupts
(4GB-20MB) – (4GB-19MB-1)	FEC00000 – FECFFFFF	1 MB	APIC Configuration Space
15MB – 16MB	F00000 – FFFFFF	1 MB	ISA Hole
1MB -15MB	100000 -EFFFFF	14 MB	Main Memory
0K –1MB	00000 – FFFFFF	1 MB	DOS Compatibility Memory

5.2. Direct Memory Access Channels

5.3. I/O Map

Hex Range	Device
000-01F	N/A
020-02D and 030-03F	Interrupt controller 1, 8259 equivalent
02E-02F	LPC SIO () configuration index/data registers
040-043	Timer, 8254-2 equivalent
04e-04f	LPC SIO () configuration index/data registers
050-053	Timer, 8254-2 equivalent
060, 064,	8742 equivalent (keyboard)
061	NMI control and status
070-077	Real Time Clock Controller(bit 7 -NMI mask)
80	Port 80 debugger
081-090	N/A
092	Reset (Bit 0)/ Fast Gate A20 (Bit 1)
091 ， 93-9F	N/A
0A0-0B1 and 0B4-0BD	Interrupt controller 2, 8259 equivalent
0B2 and 0B3	APM control and status port respectively
0C0-0DF	N/A
0E0-0EF	N/A
0F0	Co-processor error register
0F1-0FF	N/A
100-169	N/A
170-177	N/A
178-1EF	N/A
1F0-1F7	N/A
1F8-2DF	N/A
2E0-2E7	Available
2E8 -2EF	Serial Port 4
2F0-2F7	Available
2F8-2FF	Serial Port 2
300-36F	Available
376	Available
378-37F	Available

Hex Range	Device
380-3AF	Available
3B0-3BB and 3BF	Mono/VGA mode video
3BC-3BE	Reserved for parallel port
3C0-3DF	VGA registers
3E0-3E7	Available
3E8-3Ef	Serial Port 3
3F0-3F7	Available
3F8-3FF	Serial port 1
400	Alias for ICH TCO base address.
4D0,4D1	Interrupt controller
CF8-CFB	PCI configuration address register (32 bit I/O only)
CF9	Reset Control register (8 bit I/O)
CFC-CFF	PCI configuration data register
F040	Smbus base address for SB.
1800	PM (ACPI) Base Address for SB
0A00~0AFF	Reserved for SIO functions base address (ex: PME /GPIO etc)

5.4. Interrupt Request (IRQ) Lines

5.4.1. PIC Mode

IRQ#	Typical interrupt Resources	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	IRQ1 via SERIRQ	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2)	IRQ3 via SERIRQ / PIRQ	Note (1)
4	Serial Port 1 (COM1)	IRQ4 via SERIRQ / PIRQ	Note (1)
5	Serial Port 4 (COM4)	IRQ5 via SERIRQ / PIRQ	Note (1)
6	Generic	IRQ6 via SERIRQ / PIRQ	No
7	Generic	IRQ7 via SERIRQ / PIRQ	Note (1)
8	Real-time clock	N/A	No
9	Generic	N/A	Note (1)
10	Serial Port 3 (COM3)	IRQ10 via SERIRQ / PIRQ	Note (1)
11	Generic	IRQ11 via SERIRQ / PIRQ	Note (1)
12	PS/2 Mouse	IRQ12 via SERIRQ / PIRQ	Note (1)

13	FERR# logic	N/A	No
14	Generic	IRQ14 via SERIRQ / PIRQ	Note (1)
15	Generic	IRQ15 via SERIRQ / PIRQ	Note (1)

Note (1): These IRQs can be used for PCI devices when onboard device is disabled.

5.4.2. APIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	IRQ1 via SERIRQ	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2)	IRQ3 via SERIRQ	Note (1)
4	Serial Port 1 (COM1	IRQ4 via SERIRQ	Note (1)
5	Serial Port 4 (COM4)	IRQ5 via SERIRQ	Note (1)
6	N/A	N/A	Note (1)
7	N/A	N/A	Note (1)
8	Real-time clock	N/A	No
9	N/A	IRQ9 via SERIRQ	Note (1)
10	Serial Port 3 (COM3)	IRQ10 via SERIRQ	Note (1)
11	N/A	N/A	Note (1)
12	PS/2 Mouse	IRQ12 via SERIRQ	Note (1)
13	FERR# logic	N/A	Note (1)
14	N/A	N/A	Note (1)
15	N/A	N/A	Note (1)
16	N/A	P.E.G Root Port, Intel HDA, PCIE Port 0/1/2/3/4/5/6, I.G.D, XHCI Controller, Gbe Controller, SMBus Controller	Note (1)
17	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)
18	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port	Note (1)
19	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
20	N/A	N/A	Note (1)
21	N/A	N/A	Note (1)
22	N/A	N/A	Note (1)
23	N/A	XHCI Controller	Note (1)

Note (1): These IRQs can be used for PCI devices when onboard device is disabled.

5.5. PCI Configuration Space Map

Bus Number	Device Number	Function Number	Routing	Description
00h	00h	00h	N/A	Intel host Bridge
00h	01h	00h	Internal	Intel PCI Express Graphics port
00h	02h	00h	Internal	Intel I.G.D
00h	08h	00h	Internal	Gaussian Mixture Model
00h	14h	00h	Internal	xHCI Controller
00h	16h	00h	Internal	Intel Management Engine Interface
00h	17h	00h	Internal	Intel AHCI controller
00h	1Ch	00h	Internal	Intel PCI Express Root port 1
00h	1Dh	00h	Internal	Intel PCI Express Root port 9
00h	1Dh	01h	Internal	Intel PCI Express Root port 10
00h	1Dh	02h	Internal	Intel PCI Express Root port 11
00h	1Dh	03h	Internal	Intel PCI Express Root port 12
00h	1Fh	00h	N/A	Intel LPC Interface Bridge
00h	1Fh	02h	Internal	Memory Controller
00h	1Fh	03h	Internal	HDA Controller
00h	1Fh	04h	Internal	SMBUS Controller
00h	1Fh	06h	Internal	Ethernet Controller

5.6. PCI Interrupt Routing Map

INT Line	P.E.G Root Port	xHCI Controller	ME Controller #1	GbE Controller	HD Audio Controller
Int0	INTA:16	INTA:16	INTA:16	INTA:16	INTA:16
Int1	INTB:17		INTD:19		
Int2	INTC:18		INTC:18		
Int3	INTD:19	INTD:19	INTB:17		
INT Line	**PCIE Port1**	**PCIE Port9**	**PCIE Port10**	**PCIE Port11**	**PCIE Port12**

Int0	INTA:16	INTA:16	INTB:17	INTC:18	INTD:19
Int1	INTB:17	INTB:17	INTC:18	INTD:19	INTA:16
Int2	INTC:18	INTC:18	INTD:19	INTA:16	INTB:17
Int3	INTD:19	INTD:19	INTA:16	INTB:17	INTC:18

INT Line	LPC Controller	SATA Controller	SMBus Controller	Thermal Subsystem
Int0	INTA:16	INTA:16	INTA:16	
Int1	INTB:17			
Int2	INTC:18			INTC:18
Int3	INTD:19			

5.7. SMBus Address Table

Device	Address
DIMMA	A0h
DIMMB	A4h
Extend GPIO	E8h

6. BIOS Setup

The following sections describe the BIOS setup. BIOS settings of this module can be viewed and set via BIOS settings. It is strongly recommended that only users with profound experiences are allowed to change the default BIOS settings.

►Main	BIOS Information
	Memory Information
	► System Date and Time

►Advanced	► Trusted Computing
	► CPU Configuration
	► ACPI Settings
	► AMT Configuration
	► PCH-FW Configuration
	► SMART Settings
	► W83627DHG Super IO Configuration
	► NCT5104DSEC Super IO Configuration
	► NCT7802Y HW Monitor
	► CSM Configuration

	► NVMe Configuration
	► USB Configuration
	► SATA Configuration
	► Trusted Computing
►Chipset	► System Agent (SA) Configuration ► PCH-IO Configuration
Security	Password Description
Boot	Boot Configuration
►Save & Exit	Save Options Default Options

6.1. Main

6.1.1. BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	BIOS source code provider.
Core Version	Info only	AMI BIOS core version.
Compliancy	Info only	Compliance with UEFI version.
Project Version	Info only	WIN BIOS version.
Build Date and Time	Info only	WIN date the BIOS was build.

6.1.2. Memory Information

Feature	Options	Description
Total Memory	Info only	Display installed memory size.

6.1.3. Date and Time

Feature	Options	Description
System Date	Weekday, MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)

System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds

6.2. Advanced

6.2.1. Trusted Computing

Feature	Options	Description
Security Device Support	**Enabled** Disabled	Enables or Disables BIOS support for security device. When disabled OS will not show Security Device. TCG EFI protocol and INT1A interface will not be available
TPM State	**Enabled** Disabled	Enable/Disable Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device.
Pending operation	**None** TPM Clear	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.
Select Device Type	TPM 1.2 TPM 2.0 **Auto**	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

6.2.2. CPU Configuration

Feature	Options	Description
CPU	Info only	Manufacturer, model, speed
CPU Signature	Info only	Display CPU Signature.
Microcode Patch	Info only	Display Microcode Patch.
Max CPU speed	Info only	Display Max CPU speed.
Min CPU speed	Info only	Display Min CPU speed.
CPU Speed	Info only	Display CPU Speed.
Processor Cores	Info only	Display Processor Cores.
Hyper Threading Technology	Info only	Display Intel HT Technology support or not.
Intel VT-x Technology	Info only	Display Intel VT-x Technology support or not.
Intel SMX Technology	Info only	Display Intel SMX Technology support or not.
64-bit	Info only	Display 64-bit support or not.
EIST Technology	Info only	Display EIST Technology support or not

Feature	Options	Description
CPU C3 state	Info only	Display CPU C3 state support or not
CPU C6 state	Info only	Display CPU C6 state support or not
CPU C7 state	Info only	Display CPU C7 state support or not
CPU C8 state	Info only	Display CPU C8 state support or not
CPU C9 state	Info only	Display CPU C9 state support or not
CPU C10 state	Info only	Display CPU C10 state support or not
L1 Data Cache	Info only	Display cache info.
L1 Code Cache	Info only	Display cache info.
L2 Cache	Info only	Display cache info.
L3 Cache	Inf o only	Display cache info.
L4 Cache	Inf o only	Display cache info.
Hyper-threading	Disabled **Enabled**	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.
Active Processor Cores	**All** 1 2 3	Number of cores to enable in each processor package.
Intel Virtualization Technology	Disabled **Enabled**	Enable/Disable support for the Intel virtualization technology.
Hardware Prefetcher	Disabled **Enabled**	Enable the Mid Level Cache (L2) streamer prefetcher.
Adjacent Cache Line Prefetch	Disabled **Enabled**	Enable the Mid Level Cache (L2) prefetching of adjacent cache lines.
CPU AES	Disabled **Enabled**	Enable/Disable CPU Advanced Encryption Standard instructions
Boot performance mode	Max Battery **Max Non-Turbo Performance** Turbo Performance	Select the performance state that the BIOS will set before OS handoff.
Intel(R) Speed Shift Technology	Disabled **Enabled**	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.
Intel(R) SpeedStep(TM)	Disabled **Enabled**	Allows more than two frequency ranges to be supported.

Feature	Options	Description
Turbo Mode	Disabled **Enabled**	Enable/Disable turbo mode.
CPU C state	Disabled **Enabled**	Enable or disable CPU C states
Enhanced C-states	Disabled **Enabled**	Enable/Disable C1E. When enabled, CPU will switch to minimum speed when all cores enter C-State.

6.2.3. ACPI Settings

Feature	Options	Description
Enable Hibernation	Disabled **Enabled**	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select ACPI sleep state the system will enter when the SUSPEND button is pressed.

6.2.4. AMT Configuration

Feature	Options	Description
Intel AMT	Disabled **Enabled**	Enable/Disable Intel (R) Active Management Technology BIOS Extension. Note : iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device
BIOS Hotkey Pressed	**Disabled** Enabled	Enable/Disable BIOS hotkey press.
MEBx Selection Screen	**Disabled** Enabled	Enable/Disable MEBx selection screen.
Hide Un-Configure ME Confirmation Prompt	**Disabled** Enabled	Hide Un-Configure ME without password Confirmation Prompt
MEBx Debug Message Output	**Disabled** Enabled	Enable MEBx debug message output.
Un-Configure ME	**Disabled** Enabled	Un-Configure ME without password.
Amt Wait Timer	0 - 65535	Set timer to wait before sending ASF_GET_BOOT_OPTIONS.

Feature	Options	Description
ASF	Disabled **Enabled**	Enable/Disable Alert Specification Format.
Activate Remote Assistance Process	**Disabled** Enabled	Trigger CIRA boot.
USB Provisioning of AMT	Disabled **Enabled**	Enable/Disable of AMT USB Provisioning.
PET Progress	Disabled **Enabled**	User can Enable/Disable PET Events progress to recieve PET events or not.
AMT CIRA Timeout	0	OEM defined timeout for MPS connection to be established. * 0 - use the default timeout value of 60 seconds. * - MEBX waits until the connection succeeds
WatchDog	**Disabled** Enabled	Enable/Disable WatchDog Timer.
OS Timer		Set OS watchdog timer.
BIOS Timer		Set BIOS watchdog timer.

6.2.5. PCH-FW Configuration

Feature	Options	Description
ME Unconfig on RTC Clear State	**Enabled** Disabled	Disabling this option will cause ME not to unconfigure on RTC clear

6.2.6. SMART Settings

Feature	Options	Description
SMART Self Test	**Disabled** Enabled	Run SMART Self Test on all HDDs during POST.

6.2.7. W83627DHG Super IO Configuration

Feature	Options	Description
W83627DHG Super IO Configuration	Info only	
Super IO Chip	Info only	
Serial Port 1	Submenu	

Feature	Options	Description

Configuration Port	Serial		Serial Port	**Enabled** Disabled	Enable or Disable Serial Port (COM)
			Device Settings	IO=3F8h; IRQ=4	Fixed configuration of serial port.
			Change Settings	**Auto** IO=3F8h; IRQ=4 IO=3F8h;IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h;IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h;IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h;IRQ=3,4,5,6,7,9,10,11,12	Select an optimal settings for Super IO device.
Serial Port 2 Configuration Port	Serial	Submenu	Serial Port	**Enabled** Disabled	Enable or Disable Serial Port (COM)
			Disabled"	IO=2F8h; IRQ=3	Fixed configuration of serial port.
			Device Settings	**Auto** IO=2F8h; IRQ=3 IO=3F8h;IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h;IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h;IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h;IRQ=3,4,5,6,7,9,10,11,12	Select an optimal settings for Super IO device.
			Change Settings	**Standard Serial Port Mode** IrDA Active pulse 1.6 uS IrDA Active pulse 3/16 bit time ASKIR Mode	
Watch Dog Function	Info only				
Watch dog Mode	**Sec.** Min.	Watch dog Mode (Second / Minute)			
Watch dog Timer	0	Watch dog count timer. 00 is disable, 01 occurs after 1 minute only.			
Watch dog count	Info only	Watchdog countdown value.			

6.2.8. NCT5104DSEC Super IO Configuration

Feature	Options	Description
NCT5104DSEC Super IO Configuration	Info only	
Super IO Chip	Info only	
Serial Port 1	Submenu	

Feature	Options	Description

Configuration Serial Port		Serial Port	**Enabled** Disabled	Enable or Disable Serial Port (COM)
		Device Settings	IO=3E8h; IRQ=10;	Fixed configuration of serial port.
		Change Settings	**Auto** IO=3E8h; IRQ=10; IO=3E8h; IRQ=5,10; IO=2E8h; IRQ=5,10; IO=2F0h; IRQ=5,10; IO=2E0h; IRQ=5,10;	Select an optimal settings for Super IO device.
Serial Port 2 Configuration Serial Port	Submenu	Serial Port	**Enabled** Disabled	Enable or Disable Serial Port (COM)
		Device Settings	IO=2E8h; IRQ=5;	Fixed configuration of serial port.
		Change Settings	**Auto** IO=2E8h; IRQ=5; IO=3E8h; IRQ=5,10; IO=2E8h; IRQ=5,10; IO=2F0h; IRQ=5,10; IO=2E0h; IRQ=5,10;	Select an optimal settings for Super IO device.
Watch Dog Function	Info only			
Watch dog Mode	**Sec.** Min.	Watch dog Mode (Second / Minute)		
Watch dog Timer	0	Watch dog count timer. 00 is disable.		
Watch dog count	Info only	Watchdog countdown value.		

6.2.9. NCT7802Y HW Monitor

Feature	Options	Description		
Pc Health Status	Info only			
Smart Fan Function	Disabled **Enabled**	Enable or Disable Smart Fan		
Smart Fan Mode Configuration	Submenu	Feature	Options	Description
		CPU Fan Control	**Smart Duty-Cycle Mode** Manual Duty	Smart Fan Mode Select

		Mode	
	Temperature 1	35	Specifies the temperature threshold at which the H/W monitor turns on CPU fan with specific PWM duty cycle 1.
	Temperature 2	45	Specifies the temperature threshold at which the H/W monitor turns on CPU fan with specific PWM duty cycle 2.
	Temperature 3	55	Specifies the temperature threshold at which the H/W monitor turns on CPU fan with specific PWM duty cycle 3.
	Temperature 4	65	Specifies the temperature threshold at which the H/W monitor turns on CPU fan with specific PWM duty cycle 4.
	Duty Cycle 1	45	Select the PWM percentage of duty cycle 1.
	Duty Cycle 2	55	Select the PWM percentage of duty cycle 2.
	Duty Cycle 3	65	Select the PWM percentage of duty cycle 3.
	Duty Cycle 4	80	Select the PWM percentage of duty cycle 4.
cpu temperature	Read only	Display CPU current temperature.	
CPU Fan Speed	Read only	Display CPU fan speed.	
VCC	Read only	Display actual voltage of the V3.30.	
+5V	Read only	Display actual voltage of the V5.00.	
Vcore	Read only	Display actual voltage of the Vcore.	
+1.2V	Read only	Display actual voltage of the V1.2.	
+1.05V	Read only	Display actual voltage of the V1.05.	

6.2.10. CSM Configuration

Feature	Options	Description
Compatibility Support Module Configuration	Info only	
CSM Support	Disabled **Enabled**	Enable/Disable CSM Support.
CSM16 Module Version	Info only	

Feature	Options	Description
GateA20 Active	**Upon Request** Always	UPON REQUEST - GA20 can be disabled using BIOS services. ALWAYS - do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.
Option ROM Messages	**Force BIOS** Keep Current	Set display mode for Option ROM.
INT19 Trap Response	**Immediate** Postponed	BIOS reaction on INT19 trapping by Option ROM: IMMEDIATE - execute the trap right away; POSTPONED - execute the trap during legacy boot.
Boot Option filter	**UEFI and Legacy** Legacy only UEFI only	This option controls Legacy/UEFI ROMs priority
Option ROM execution	Info only	
Network	**Do not launch** UEFI Legacy	Controls the execution of UEFI and Legacy PXE OpROM.
Storage	Do not launch UEFI **Legacy**	Controls the execution of UEFI and Legacy Storage OpROM.
Video	Do not launch UEFI **Legacy**	Controls the execution of UEFI and Legacy Video OpROM.
Other PCI devices	Do not launch **UEFI** Legacy	Determines OpROM execution policy for devices other than Network, Storage, or Video

6.2.11. NVMe Configuration

Feature	Options	Description
NVME controller and Drive information	Info Only	

6.2.12.USB Configuration

Feature	Options	Description
USB Configuration	Info only	
USB Module Version	Info only	

USB Controllers	Info only	X XHCI
USB Devices	Info only	X Drive, X Keyboards, X Mouse, X Hubs
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI OS driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable/Disable USB Mass Storage Driver Support.
USB hardware delays and time-outs:	Info only	
USB transfer time-out	1 sec 5 sec 10 sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
Mass Storage Devices	Info only	List current USB max stroge device.

6.2.13. SATA Configuration

Feature	Options	Description
SATA Controller(s)	**Enabled** Disabled	Enable or disable SATA Device.
SATA Mode Selection	**AHCI** RAID	Determines how SATA controller(s) operate.
Software Feature Mask	Submenu	**Feature** **Options** **Description**

Configuration		RAID0	Disabled **Enabled**	Enable or Disable RAID0 feature.
		RAID1	Disabled **Enabled**	Enable or Disable RAID1 feature.
		RAID10	Disabled **Enabled**	Enable or Disable RAID10 feature.
		RAID5	Disabled **Enabled**	Enable or Disable RAID5 feature.
		OROM UI Normal Delay	**2 Seconds** 4 Seconds 6 Seconds 8 Seconds	Select the delay time of the OROM UI Splash Screen in a normal status.
Aggressive LPM Support	**Enabled** Disabled	Enable PCH to aggressively enter link power state.		
Serial ATA Port 0	Info only			
Software Preserve	Info only			
Port 0	Disabled **Enabled**	Enable or Disable SATA Port		
Serial ATA Port 1	Info only			
Software Preserve	Info only			
Port 1	Disabled **Enabled**	Enable or Disable SATA Port		
Serial ATA Port 2	Info only			
Software Preserve	Info only			
Port 2	Disabled **Enabled**	Enable or Disable SATA Port		
Serial ATA Port 3	Info only			
Software Preserve	Info only			
Port 3	Disabled **Enabled**	Enable or Disable SATA Port		

6.2.14.System Agent (SA) Configuration

Feature	Options	Description
System Agent Bridge Name	Info only	Display System Agent Bridge name.

SA PCIe Code Version	Info only	
VT-d	Info only	Check VT-d function on System Agent.
VT-d	Disabled **Enabled**	VT-d capability.

Graphics Configuration	Submenu	**Feature**	**Options**	**Description**
		Graphics Configuration	Info only	
		IGFX VBIOS Version	Info only	Display VBIOS Version.
		Skip Scaning of External Gfx Card	**Disabled** Enabled	If Enable, it will not scan for External Gfx Card on PEG and PCH PCIE Ports
		Primary Display	**Auto** IGFX PEG PCIE	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.
		Internal Graphics	**Auto** Disabled Enable	Keep IGFX enabled based on the setup options.
		GTT Size	2MB 4MB **8MB**	Select the GTT Size.
		Aperture Size	128MB **256MB** 512MB 1024MB 2048MB 4096MB	Select the Aperture Size Note : Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM Support.
		DVMT Pre-Allocated	**XXM**	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
		DVMT Total Gfx Mem	**XXXM**	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.
		LCD Control	Submenu	

Feature	**Options**	**Description**
LCD Control	**Info only**	
~~LCD Panel~~	~~**VBIOS Default**~~	~~Select LCD panel~~

		Type	640X480 LVDS 800X600 LVDS 1024X768 LVDS 1280X1024 LVDS 1400X1050 LVDS1 1400X1050 LVDS2 1600X1200 LVDS 1366X768 LVDS 1680X1050 LVDS 1920X1200 LVDS 1440X900 LVDS 1600X900 LVDS 1280X800 LVDS 1920X1080 LVDS 2048X1536 LVDS	used by Internal Graphics Device by selecting the appropriate setup item.
		Panel Scaling	**Auto** Off Force Scaling	Select the LCD panel scaling option used by the Internal Graphics Device.
		Backlight Control	PWM Inverted PWM Normal	Back Light Control Setting.
		Active LFP	**Disabled** Enabled	Configuring LFP usage
		Panel Color Depth	**18 Bit** 24 Bit	Select the LFP Panel Color Depth

		Feature	**Options**	**Description**
PEG Port Configuration	Submenu	PEG Port Configuration	Info only	
		PEG 0:1:0	**Not Present**	Display PEG0 present or not.
		Enable Root Port	Disabled Enabled **Auto**	Enable or Disable the Root Port.
		Max Link Speed	**Auto** Gen1 Gen2	Configure PEG 0:1:0 Max Speed

			Gen3	
		PEG 0:1:1	**Not Present**	Display PEG1 present or not.
		Enable Root Port	Disabled Enabled **Auto**	Enable or Disable the Root Port.
		Max Link Speed	**Auto** Gen1 Gen2 Gen3	Configure PEG 0:1:1 Max Speed
		PEG 0:1:2	**Not Present**	Display PEG2 present or not.
		Enable Root Port	Disabled Enabled **Auto**	Enable or Disable the Root Port.
		Max Link Speed	**Auto** Gen1 Gen2 Gen3	Configure PEG 0:1:2 Max Speed

		Feature	Options	Description
GT - Power Management Control	Submenu	GT - Power Management Control	Info only	
		GT Info	Info only	Display Processor Graphics Technology (GT) Info.
		RC6(Render Standby)	Disabled **Enabled**	Check to enable render standby support.

6.2.15. PCH-IO Configuration

Feature	Options	Description
Intel PCH RC Version	Info only	Display Intel PCH RC Version.
Intel PCH SKU Name	Info only	Display Intel PCH Name.
Intel PCH Rev ID	Info only	Display Intel PCH Revision ID.

		Feature	Options	Description
PCI Express Configuration	Submenu	PCI Express Configuration	Info only	

		PCI Express Root Port 1	Submenu	PCI Express Root Port 1 Settings.
		PCI Express Root Port 9	Submenu	PCI Express Root Port 9 Settings.
		PCI Express Root Port 10	Submenu	PCI Express Root Port 10 Settings.
		PCI Express Root Port 11	Submenu	PCI Express Root Port 11 Settings.
		PCI Express Root Port 12	Submenu	PCI Express Root Port 12 Settings.

		Feature	Options	Description
		HD Audio Configuration	Info only	
HD Audio Configuration	Submenu	HD Audio	Disabled Enabled **Auto**	Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled Auto = HDA will be enabled if present, disabled otherwise.

PCH LAN Controller	**Enabled** Disabled	Enable or disable onboard NIC.
Wake On LAN	**Enabled** Disabled	Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)
State After G3	**S0 State** S5 State	Specify what state to go to when power is re-applied after a power failure (G3 state).

6.3. Security

Password Description

Feature	Options	Description
Administrator Password	Enter password	Set Administrator Password
User Password	Enter password	Set User Password

6.4.Boot

Boot Configuration

Feature	Options	Description
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the keyboard NumLock state
Quiet Boot	**Disabled**	Enables or disables Quiet Boot option

	Enabled	
Boot Option Priorities	Info only	
Boot Option #**X**	Selection	Sets the system boot orde

6.5. Save & Exit

Save Options

Feature	Options	Description
Save Changes and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset system setup without saving any changes.

7. BIOS Checkpoints, Beep Codes

7.1. Status Code Ranges

Status Code Range	Description
0x01-0x0F	SEC Status Codes & Errors
0x10-0x2F	PEI execution up to and including memory detection
0x30-0x4F	PEI execution after memory detection
0x50-0x5F	PEI errors
0x60-0xCF	DXE execution up to BDS
0xD0-0xDF	DXE errors
0xE0-0xE8	S3 Resume (PEI)
0xE9-0xEF	S3 Resume errors (PEI)
0xF0-0xF8	Recovery (PEI)
0xF9-0xFF	Recovery errors (PEI)

7.2. Standard Status Codes

7.2.1. SEC Status Codes

Status Code Range	Description
0x01-0x0F	SEC Status Codes & Errors
0x10-0x2F	PEI execution up to and including memory detection

0x30-0x4F	PEI execution after memory detection
0x50-0x5F	PEI errors
0x60-0xCF	DXE execution up to BDS
0xD0-0xDF	DXE errors
0xE0-0xE8	S3 Resume (PEI)
0xE9-0xEF	S3 Resume errors (PEI)
0xF0-0xF8	Recovery (PEI)
0xF9-0xFF	Recovery errors (PEI)

7.2.2. PEI Status Codes

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed

Status Code	Description
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	

Status Code	Description
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
S3 Resume Error Codes	
0xE8	S3 Resume Failed in PEI
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

7.2.3. PEI Beep Codes

Number of Beeps	Description
1	Memory not Installed
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

7.2.4. DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization

0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes

0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

7.2.5. DXE Beep Codes

Number of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Input or Output Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

7.2.6. ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state

0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode

7.3. OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D - 0x2A	OEM pre-memory initialization codes
0x3F-0x4E	OEM PEI post memory intialization codes
0x80-0x8F	OEM DXE initialization codes
0C0-0xCF	OEM BDS intialization codes

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