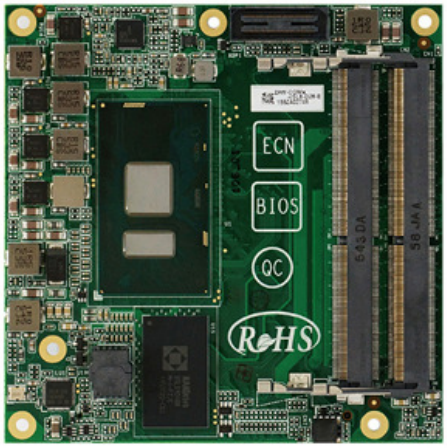
Custom Embedded Solutions



COM Express

MB-73440

User's Manual

COM Express®

Custom Embedded Solutions

Version:

Release Date:

Part Number:

Revision History

Revision	Description	Date	By
1.0	Initial Release	2016.5.23	T.C.

Preface

This user manual offers detail information about components, pinouts, connectors and BIOS Setups of WIN's MB-73440 board. For more information about design and development for COM Express™ applications, please refer to documents released from the PCI Industrial Computer Manufacturers Group (PICMG):

- COM Express™ Design Guide
- COM Express™ Specification

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Hazardous substance-Free (RoHS) Compliant

This product is designed and developed on hazardous substance-free components and parts and totally RoHS (Restriction of Hazardous Substances Directive 2002/95/EC) compliant.

Certification

WIN Enterprises, Inc. is certified to DIN EN ISO 9001 and 14001 standards.

Electrostatic Sensitive Device

This product is an electrostatic sensitive device (ESD) and packaged accordingly. In any case this product can not be opened, handled, stored or transported without proper ESD protection mechanisms and please store and ship this product in its original manufacturer's packaging. Failure to comply with these guidelines will make this product damaged and avoid Limited Warranty offered by WIN Enterprises, Inc.

Table of Contents

1. Introduction

COM Express™ is an open industry standard defined exclusively for COMs (computer on modules) and offers a fast solution of forward/backward compatibility for legacy I/O interface and the latest technologies available nowadays. COM Express™ modules are available in following form factors:

Type	Size
COM Express® mini	84mm x 55mm
COM Express® Compact	95mm x 95mm
COM Express® Basic	125mm x 95mm
COM Express® Extended	155mm x110mm

The MB-73440 board is a COM Express® COM.0 R2.1 Type 6 Compact size module featuring the 64-bit 6th Generation Intel® Core™ i7/i5/i3 and Intel® Celeron® Ultra-Low TDP processors (formerly "Skylake-U") with CPU, memory controller, graphics processor and I/O hub on a single chip. Leveraging the benefits provided by the 6th generation Intel® Core™ and Celeron™ System-on-Chip, the MB-73440 board is specifically designed for customers who need optimum processing and graphics performance with suitable power consumption using Intel's Configurable TDP in a long product life solution. The MB-73440 board's Intel® processors support Intel® Hyper-Threading Technology (up to 2 cores, 4 threads) and up to 32 GB of non-ECC DDR4 dual-channel memory at 1866/2133 MHz in dual stacked SODIMM sockets to provide excellent overall performance.

Integrated Intel® Generation 9 Low Power Graphics includes features such as OpenGL 4.4/4.3, DirectX 11.3/11, Intel® Clear Video HD Technology, Advanced Scheduler 2.0, 1.0, XPDM support, and DirectX Video Acceleration (DXVA2) support for AVC/VC1/MPEG2/HEVC/ VP8/JPEG hardware decode and AVC/MPEG2/HEVC/VP8/JPEG hardware encode. Graphics outputs include dual-channel 18/24-bit LVDS (eDP optional) and two DDI ports supporting HDMI/DVI/DisplayPort. The MB-73440 board is specifically designed for customers with high-performance processing graphics requirements who want to outsource the custom core logic of their systems for reduced development time.

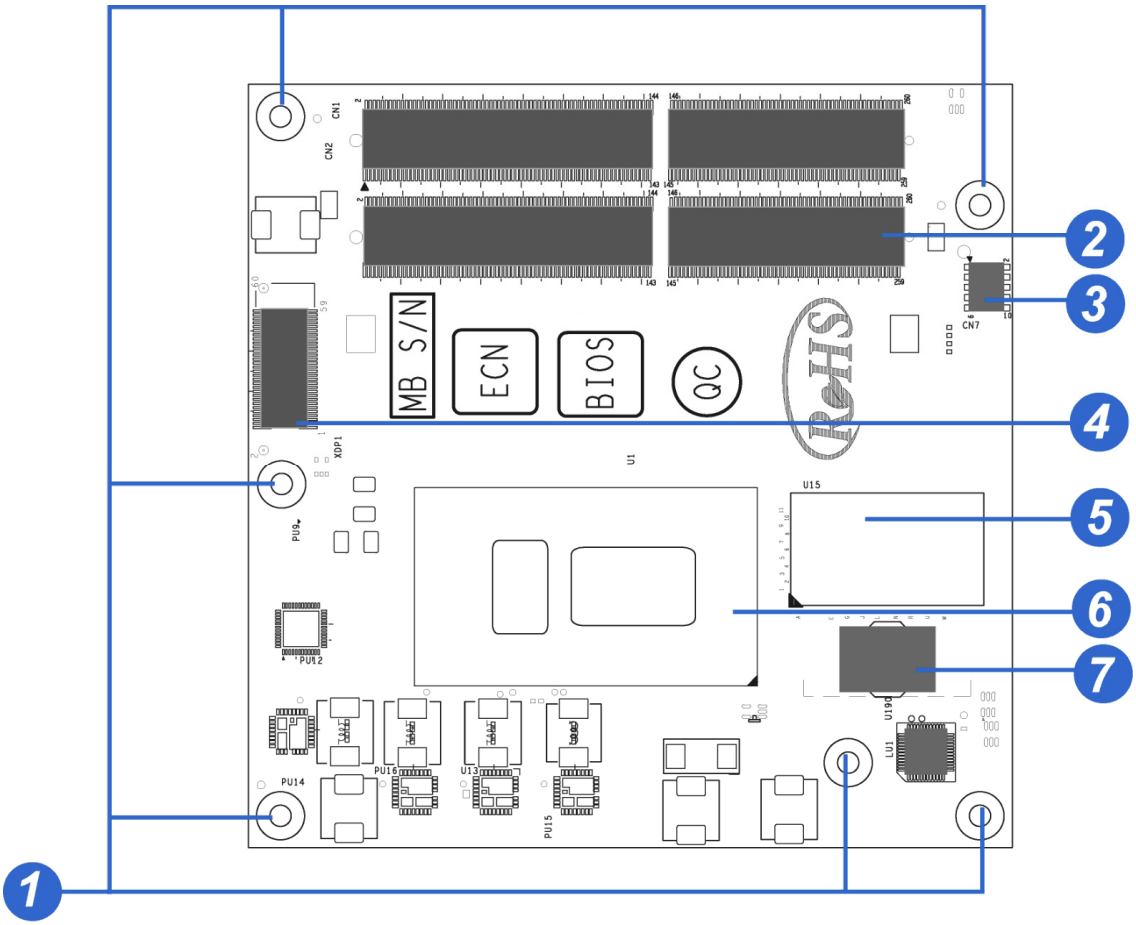
The MB-73440 board features a single onboard Gigabit Ethernet port, five PCIeGen3 /2 ports, four USB 3.0 ports, eight USB 2.0 ports, and up to three SATA 6Gb/s ports(Premium-U). Support is provided for SMBus and I2C. The module is equipped with SPI AMI EFI BIOS with CMOS backup.

Types	Type 1	Type 2	Type 6	Type 10
Connector Row	A-B	A-B C-D	A-B C-D	A-B
PCI Express Lane	Up to 6	Up to 22	Up to 24	Up to 4

PCI	N/A	32 bit	N/A	N/A
IDE Channel	1	1		
LAN port	1	1	1	1
USB 2.0/USB 3.0	8 / 0	8 / 0	8 / 4	8 / 0
Display Interfaces	VGA, LVDS	VGA, LVDS,PEG/SDVO	VGA,LVDS,PEG, 3 X DDI	1x DDI

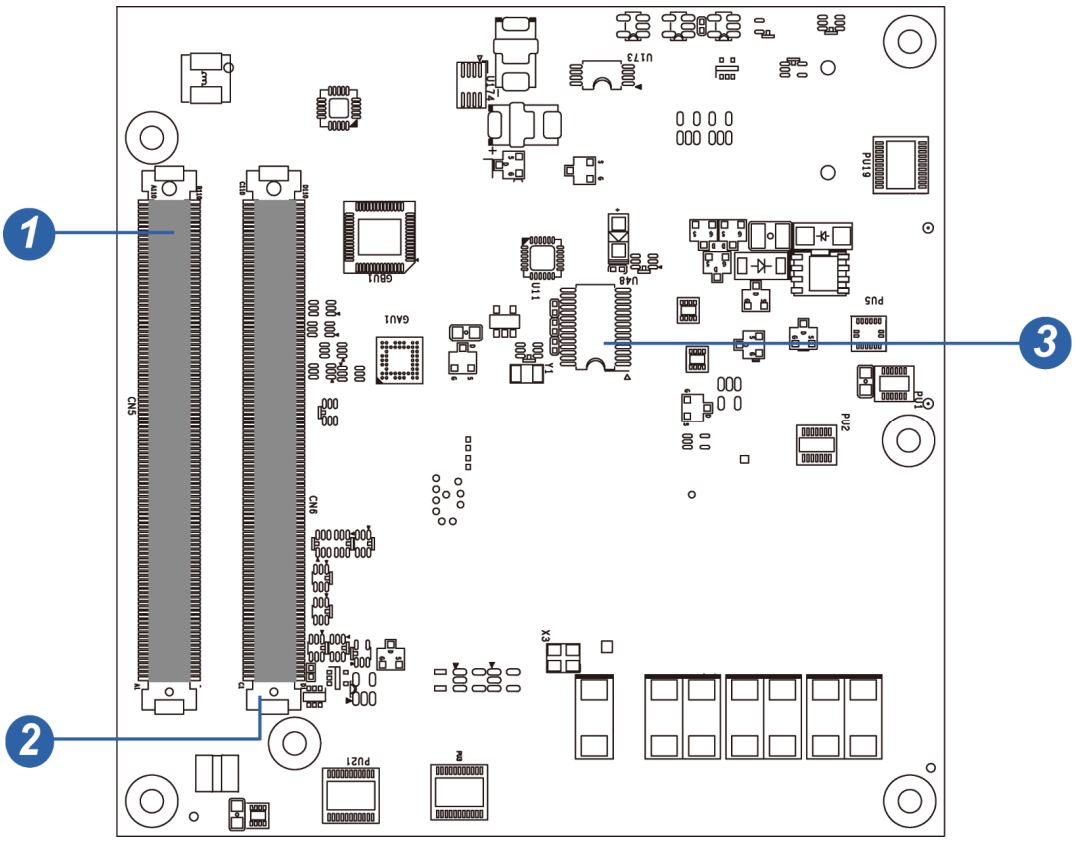
1.1. Hardware Briefing

1.1.1. TOP VIEW



1.	Mounting holes	*2.*	SODIMMDDR4 slot
3.	Port 80	*4.*	XDP (Debug Header)
5.	SATA SSD	*6.*	SkyLake-U
7.	BIOS		

1.1.2. BOTTOM VIEW



1.	Board-to-board Connector A-B
2.	Board-to-board Connector C-D
3.	TPM (1.2/2.0)

2. Specifications

2.1. CoreSystem

CPU

- Intel® Core™ i7-6600U 2.6 GHz (3.4 GHz Turbo), 15W (cTDP support) (2C/GT2)
- Intel® Core™ i5-6300U 2.4 GHz (3.0 GHz Turbo), 15W (cTDP support) (2C/GT2)
- Intel® Core™ i3-6100U 2.3 GHz (no Turbo), 15W (cTDP support) (2C/GT2)

CPU Supported

- Intel® VT
- Intel® TXT
- Intel® SSE4.2
- Intel® HT Technology
- Intel® 64 Architecture
- Intel®Execute Disable Bit
- Intel® Turbo Boost Technology 2.0
- Intel® AVX2
- Intel® AES-NI
- Intel®PCLMULQDQ Instruction
- Intel® Device Protection Technology with Intel® Secure Key
- Intel® TSXNI

Note: Availability of features may vary between processor SKUs.

L3 Cache

- Core™ i7 4 MB
- Core™ i5 3 MB
- Core™ i3 3 MB

Memory

Dual channel non-ECC 1866/2133 MHz DDR4 memory up to 32 GB in dual SODIMM socket

BIOS

AMI EFI with CMOS backup in 16MB SPI BIOS with Intel® AMT 11.0 support (AMT supported on i7/i5 SKUs only)

Platform Controller Hub

Integrated PCH-LP (i7/i5/i3: Premium PCH-LP)

2.2. Expansion Busses

PCIe x1 (Gen3)	X5	Core™i7/i5/i3, Lanes 1/2/3/4/6 can be configured to: x4 x2 x1
LPC bus	X1	
SMBus (system)	X1	

2.3. Video

GPU

Intel® Generation 9 Graphics integrated in CPU and featured with:

- Supports 3 displays (independently/simultaneously) via Display Port/HDMI/LVDS monitors (eDP optional in place of LVDS)
- Encode/transcode high definition (HD) video supported
- High definition (HD) video (e.g. Blu-ray DVD) supported
- Playback of Blu-ray Disc 3D content via HDMI (HDMI e1.4a)
- DirectX Video Acceleration (DXVA2) supported
- HEVC/H.265, H.264, M/JPEG, MPEG2, VC1, WMV9, VP8/VP9 HW decode supported
- HEVC/H.265, M/JPEG, MPEG2 HW encode supported
- Advanced Scheduler 2.0, 1.0 and XPDM supported

- DirectX 12, DirectX 11.3, DirectX 11, DirectX 10.1, DirectX 10 and DirectX 9 supported
- Open Graphics Library(OpenGL) 4.4 supported
- OpenCL (Open Computing Language) supported
- Advanced Scheduler 2.0, 1.0, XPDM support
- DirectX 11.3, OpenGL 4.4, OpenGL ES 2.0 and OpenCL 2.0
- Multi Display Support: 3 independent displays

  Note: features listed above is available depending on operating systems.

Display Interface

LVDS	Single/dual channel 18/24-bit LVDS to LVDS (NXP IC) via eDP-to-LVDS chip.
eDP	4 lanes supported maximum, integrated in LVDS (BOM optional)
Digital Display Port x 2	DisplayPort/HDMI/DVI supported

2.4. Audio

Intel® HD Audio	integrated on SoC
Audio Codec	Integrated in AW-COMe-EVAL carrier board

2.5. LAN

Intel PHY: Intel® Ethernet Controller i219LM

Interface: 10/100/1000 GbE connection

2.6. Multi I/O and Storage

USB	4x USB 3.0 (USB 1,2,3)
	8x USB 2.0 (USB 0,1,2,3,4,5,6,7)
SATA	3 x SATA 6Gb/s (SATA 0,1,2)
GPIO	4 GPO and 4 GPI

Note: For SATA 6Gb/s, it is strongly recommended to install a SATA re-driver on the carrier board.

2.7. Serial I/O

Ports	2x UART for Rx/Tx only (Availability depends on the carrier board you use with an W83627DHG LPC I/O chipset)

	Description	IRQ	Address
COM 1	Support by Super I/O (W83627DHG) from carrier board	4	3F8h
COM 2	Support by Super I/O (W83627DHG) from carrier board	3	2F8h

2.8. Trusted Platform Module (TPM) (Optional)

Chipset SLB9660XT1.2

Type TPM 1.2/TMP 2.0 (optional)

2.9. Debug Headers

Port 80 10-pin debug header for LPC debug card diagnosing module.

60-pin XDPmerged connector for ICE debug of CPU/chipset (optional)

2.10. Power Specifications

Power Modes	AT and ATX mode
Standard Voltage Input	ATX = 12V±5% / 5Vsb ±5% AT = 12V±5%
Wide Voltage Input	ATX = 5~20 V / 5Vsb ±5% AT = 5 ~20V
Power Management	ACPI 5.0 compliant
Power States	supports C1-C6, S0, S3, S4, S5 (Wake-on-USB S3, WoL S3/S4/S5)
Power Consumption	For information about power consumption, please contacts our business representative.

2.11. Environmental Requirements

Operating Temperature	Standard: 0°-60 °C (32 – 140° C) Extended: -40 °– 85 °C (-40 °– 180° F)
Storage Temperature	-40°– 85°C (-40° – 180° F) 60°C @ 95% relative humidity, non-condensing

Humidity	5-90% RH operating, non-condensing
	5-95% RH storage (and operating with conformal coating).
Vibration Resistance	IEC 60068-2-64
Halt	Vibration Stress

2.12. Regulatory Compliance

Hazardous Substance-free (RoHS) Compliant

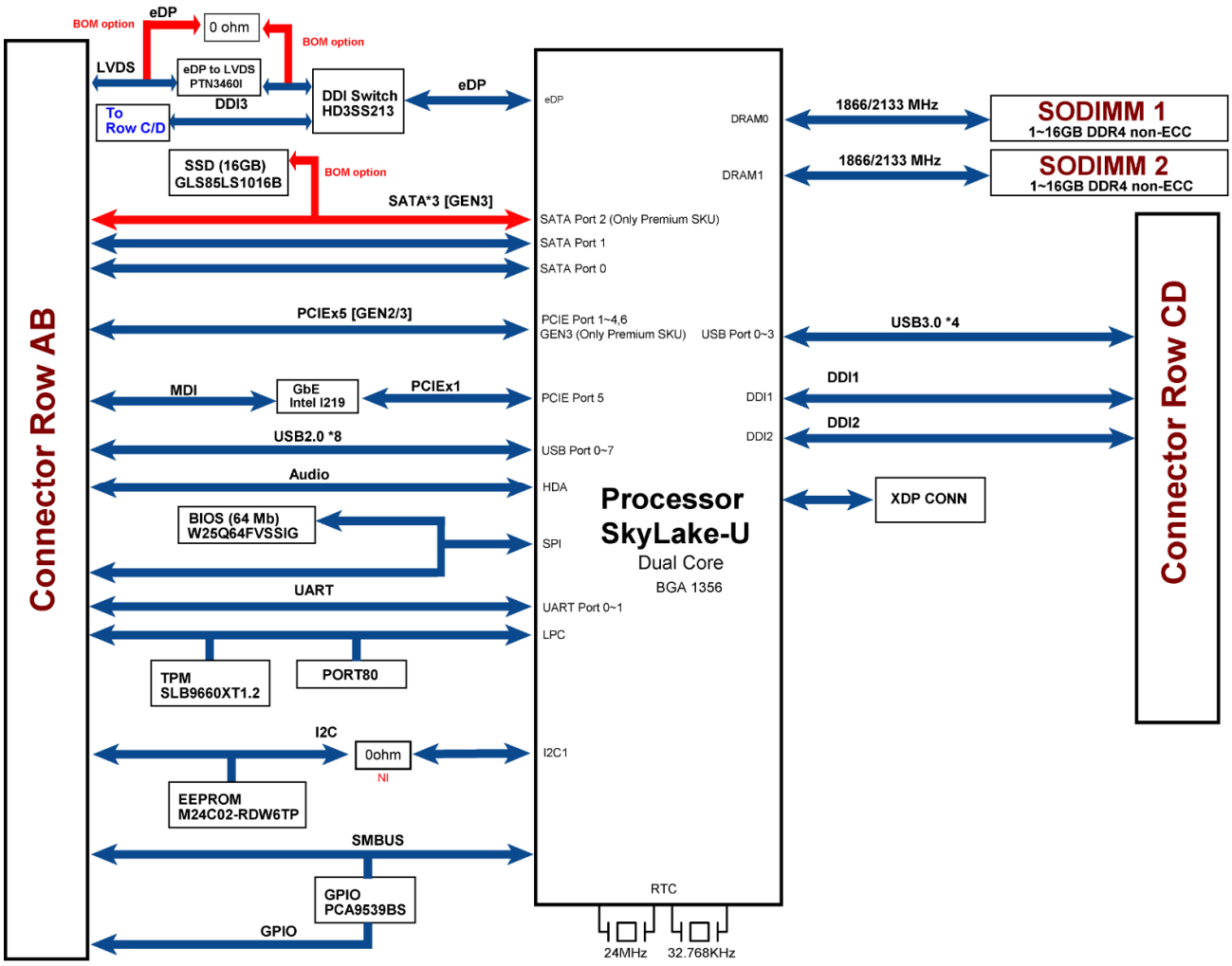
This product is designed and developed on hazardous substance-free components and parts and totally RoHS (Restriction of Hazardous Substances Directive 2002/95/EC) compliant.

2.13. Operating Systems

MB-73440 board supports following operating systems:

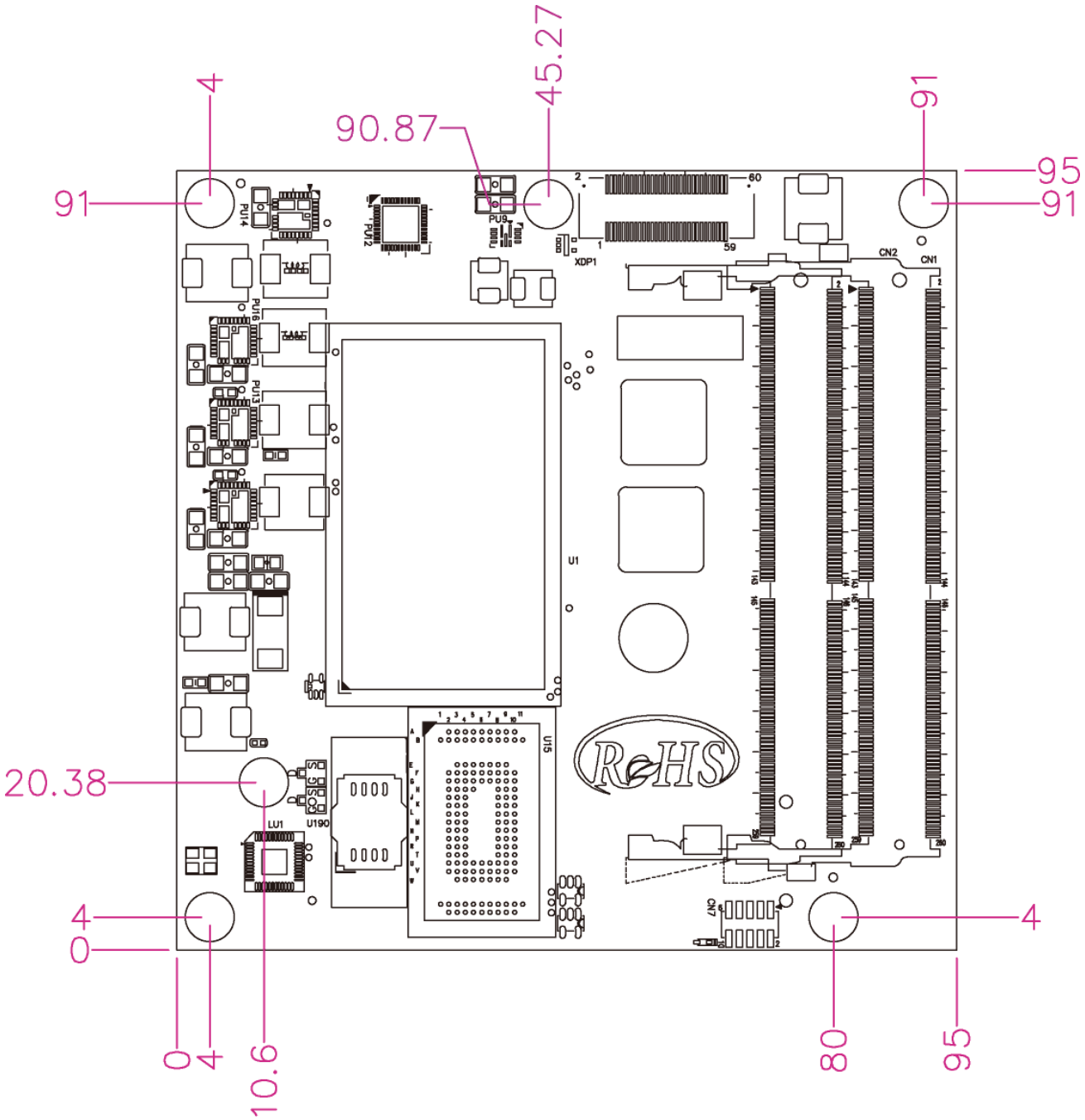
- Red Hat® Enterprise 6.4
- Fedora® 20
- Microsoft® Windows 7 Ultimate 64 bit
- Microsoft® Windows® 8.1 Professional 64 bit
- Windows® 10 Professional 64 bit

2.14. Functional Diagram

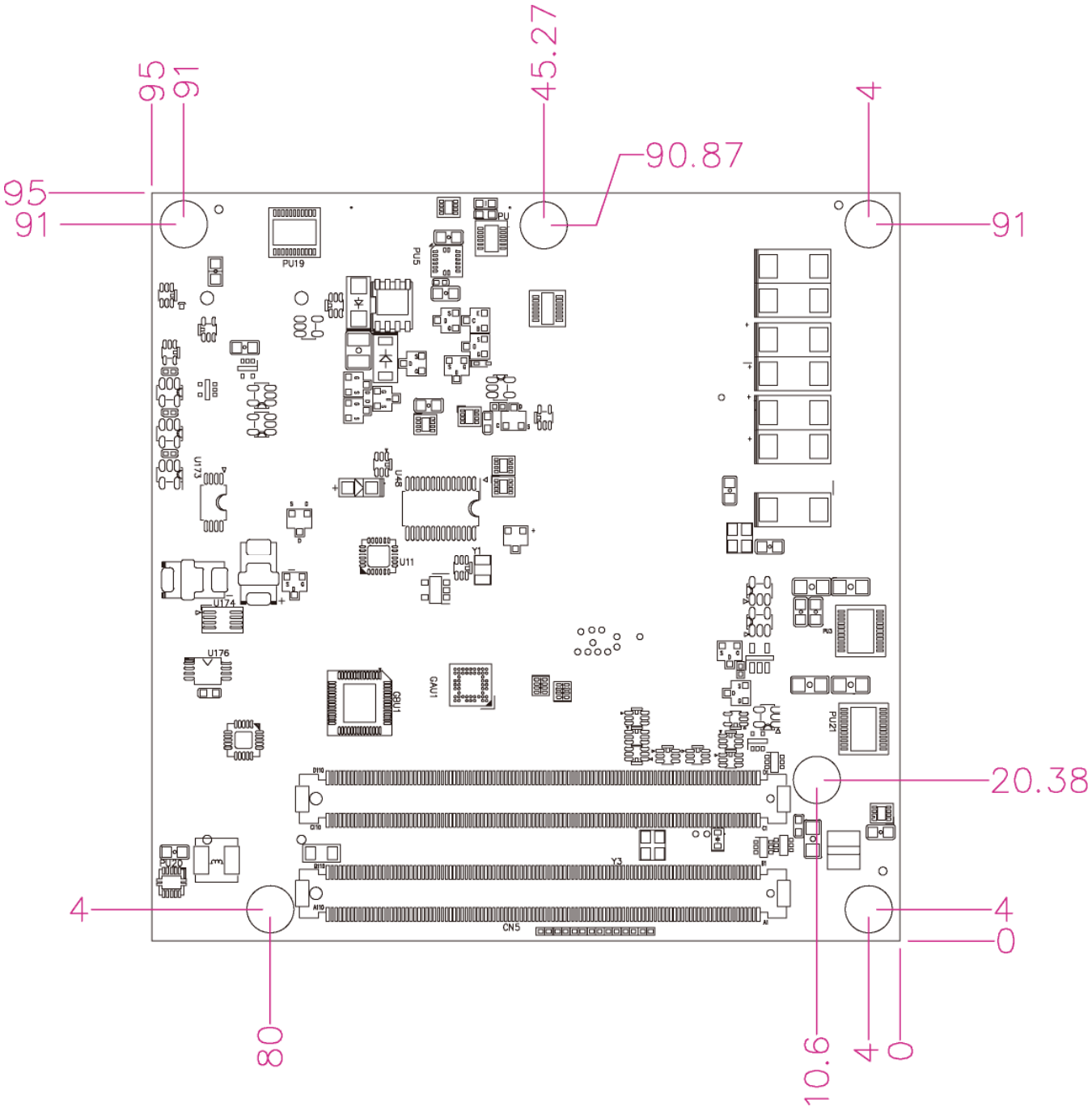


3. Mechanical Information

3.1 Mechanical Dimensions



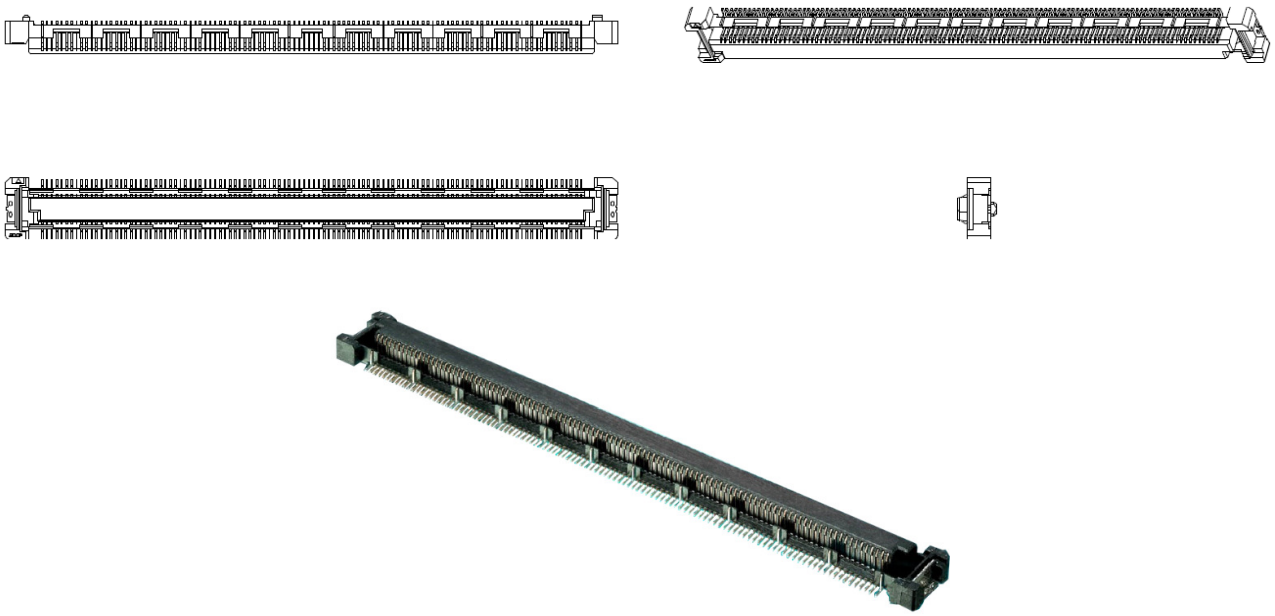
Unit: mm



Unit: mm

3.2. Module Connector

The board-to-board connectors are 440-pin receptacles that are composed of 2 pieces of a 220-pin, 0.5 mm pitch receptacle.



Tyco 3-6318490-6

- 220-pin board-to-board connector with 0.5mm for a stacking height of 8 mm.
- This connector can be used with 8 mm through-hole standoffs (SMT type).

Common Specifications

- Current capacity: 0.5A per pin
- Rated voltage: 50 VAC
- Insulation resistance: 100M or greater @ 500 VDC
- Temperature rating: -40˚C ~ 85˚C
- UL certification (ECBT2.E28476)
- Copper alloy (contacts)
- Housing: thermo-plastic molded compound (L.C.P.)

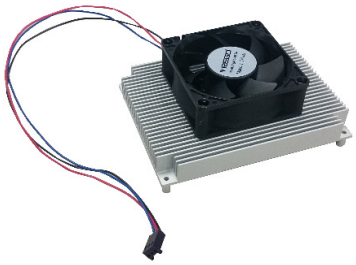
3.3. Thermal Solution (for reference only)

3.3.1. Heat Sink

It is recommended to use a heat sink or thermal fan as the thermal solution according to the actual application. Steps below are based on heat sink as an example.

3.3.2. Installation

Prepare parts below:

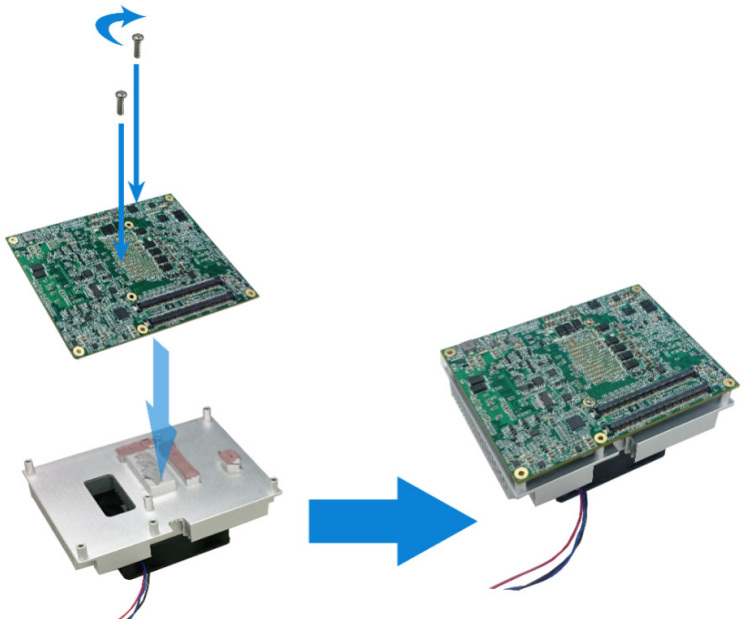


Heatsink assembly X 1

COM Express Carrier board X 1
MB-COMe-EVAL

Fastening screws (M2.5, L = 8 mm) X 2
Fastening screws (M2.5, L = 16 mm) X 5

Step 1: Remove the protective film from the thermal pads.
Step 2: Align the mounting holes of the module, fit the module onto the heat thing by securing the two fastening screws (M2.5, L = 8 mm) as shown below.

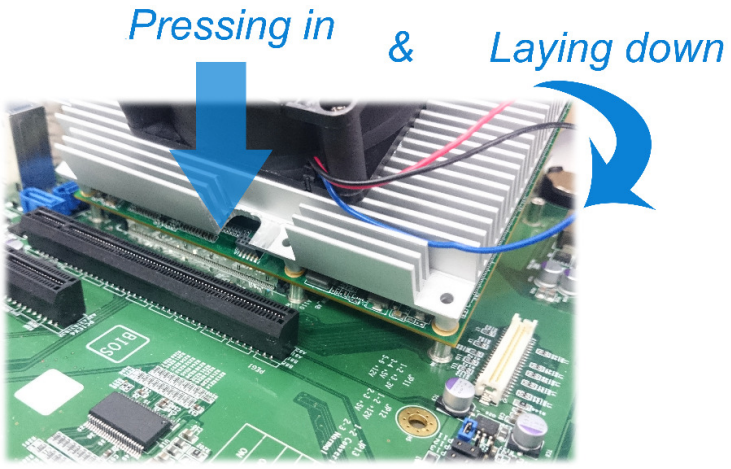


Step 3:

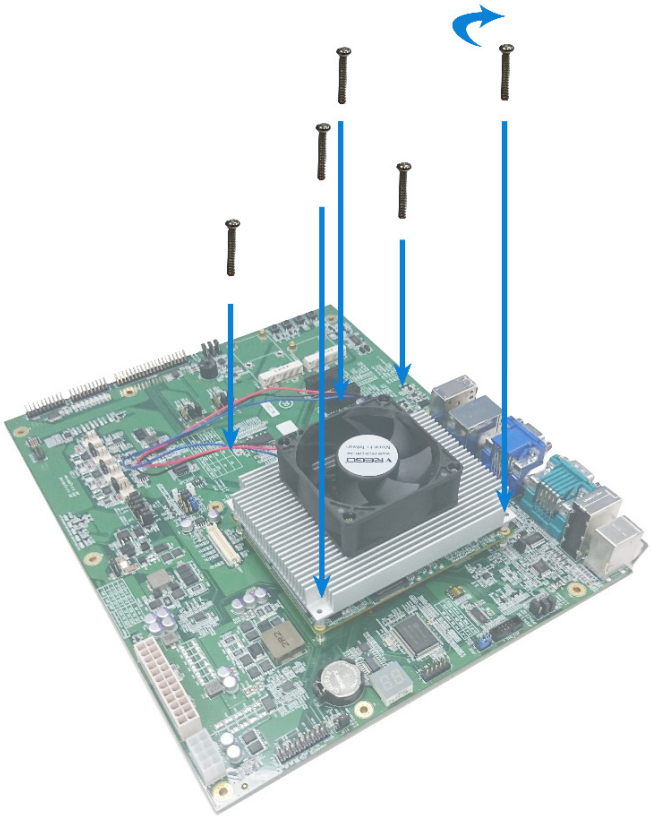
a. Tilt the heat sink assembly with the module and align the three studs of the module to the three studs of the carrier board.

b. Fit the heat sink assembly with the module by pressing where the arrow indicates.

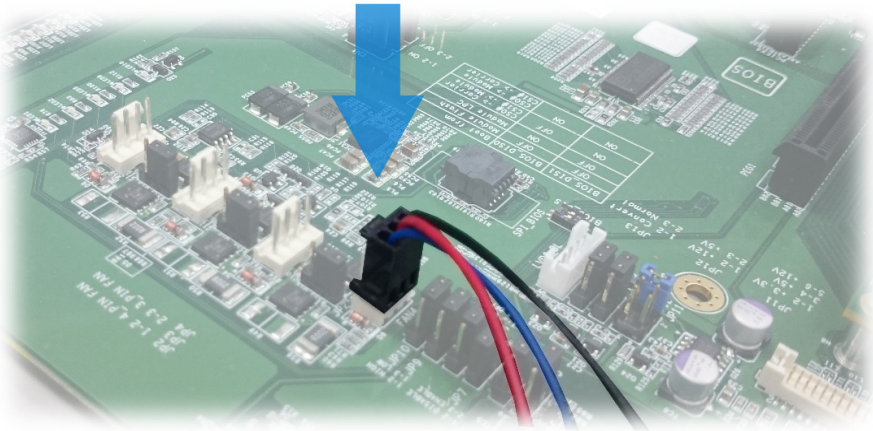
c. Lay down the heat sink assembly with the module.

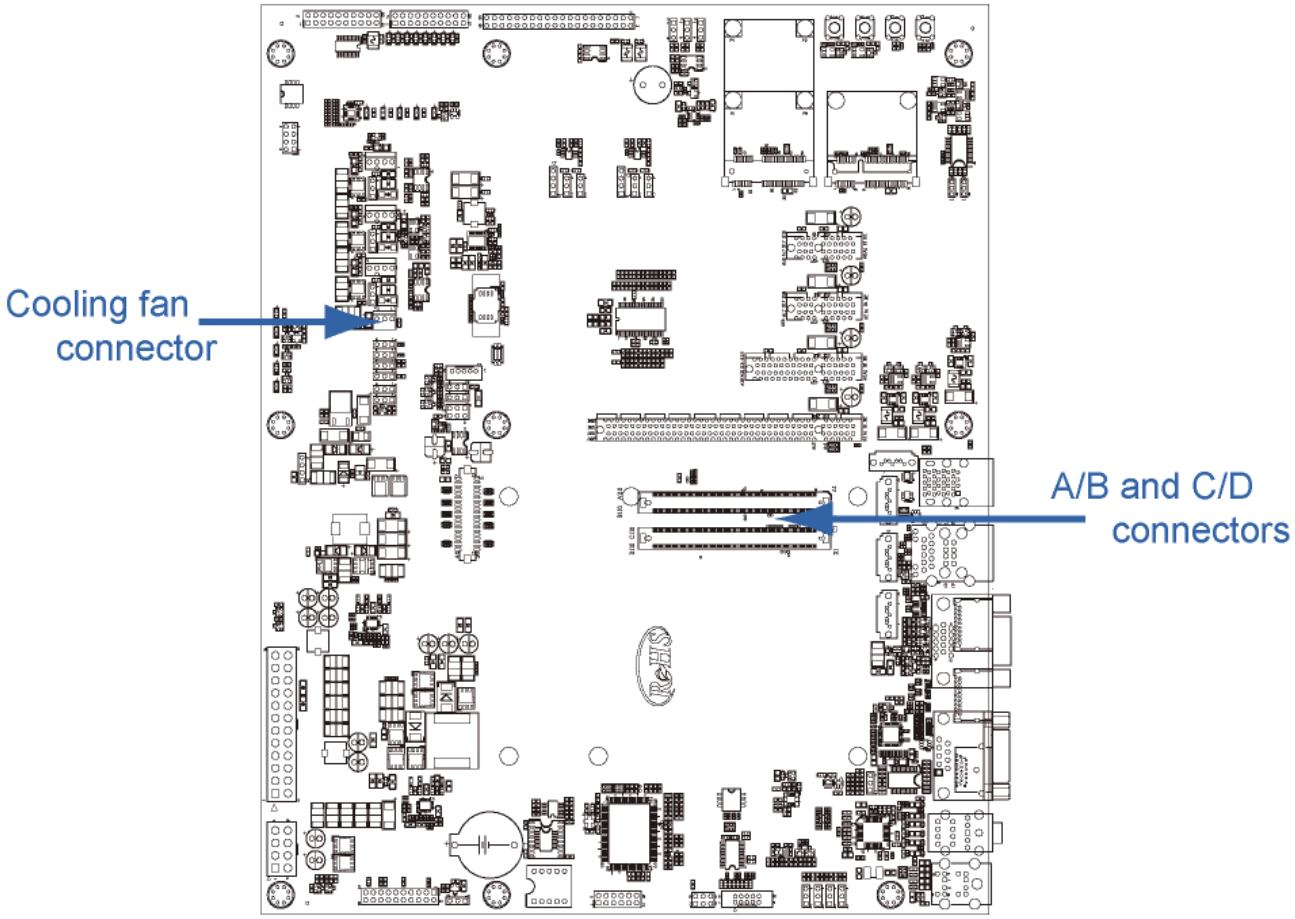


Step 4: Tighten the shipped five fastening screws (M2.5, L = 16 mm) to secure the module.



Step 5: Connect the power plug of the heat sink assembly..





3.4. Mounting Methods

3.4.1. Mechanical Specifications

Dimensions

95.0 mm x 95.0 mm (3.75” x 3.75”)

Height

If a Module is equipped with a heat-spreader, the heat-spreader by itself does not constitute the complete thermal solution for a Module but provides a common interface between Modules and implementation-specific thermal solutions.

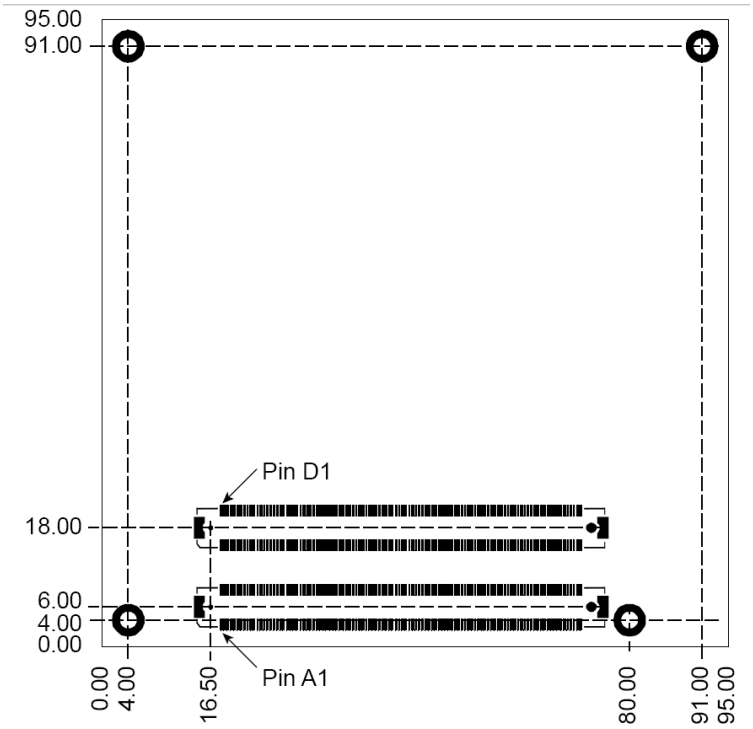
If implemented, a heat-spreader for the Basic form factor shall use an implementation specific set of holes and spacers to attach the heat-spreader to the Module. These implementation specific holes are

in addition to the Module mounting holes specified in below.

Module Size - Compact Module

The PCB size for the Compact Module shall be 95mm x 95mm. The PCB thickness should be 2mm to allow high layer count stack-ups and facilitate a standard “z” dimension between the Carrier Board and the top of the heat-spreader.

The holes shown in this drawing are intended for mounting the Module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers shall be used to attach the heat-spreader to the Module.



Unit: mm

Tolerances shall be ± 0.25mm [±0.010"], unless noted otherwise.

The 440 pin connector pair shall be mounted on the backside of the PCB and is seen “through” the board in this view.

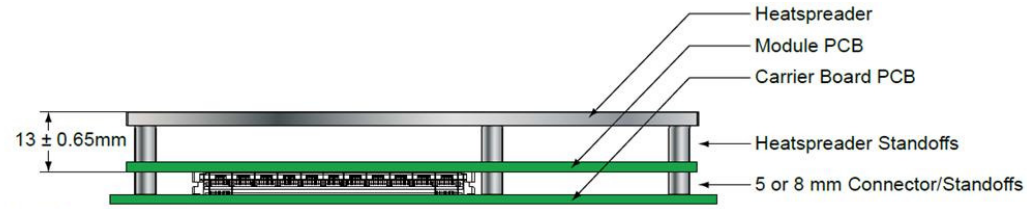
The four mounting holes shown shall use 6mm diameter pads and shall have 2.7mm plated holes, for use with 2.5mm hardware. The pads shall be tied to the PCB ground plane.

Modules shall include the 5 mounting holes as shown in Figure above. These holes are primarily used to attach the Module to the Carrier.

For the Compact form factor a heat-spreader should not use the Module mounting holes as the only attachment points to a Module. The intent is to be able to provide a Module and heat-spreader as an assembly that can then be mounted to a Carrier without having to break the thermal interface between the Module components and the heat-spreader.

The standoffs should be mounted on the Carrier Board. The height of the standoff is dependent on the stack height of the Carrier Board connector (5 mm or 8mm).
The overall Module height from the bottom surface of the Module board to the heat-spreader top surface shall be 13 mm for the Mini, the Compact, the Basic and the Extended Modules.

The Module PCB and heat-spreader plate thickness are vendor implementation specific, however, a 2 mm PCB with a 3 mm heat-spreader may be used which allows use of readily available standoffs.



All dimensions in mm.

Tolerances (unless otherwise specified):

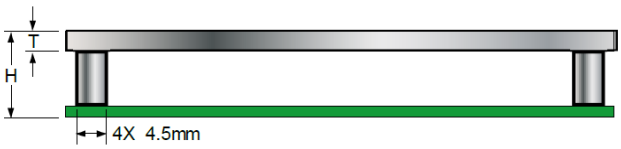
Z (height) dimensions should be ± 0.8mm [±0.031”] from top of Carrier Board to top of heatspreader.

Heat-spreader surface should be flat within 0.2mm [.008"] after assembly.

Interface surface finish should have a maximum roughness average (Ra) of 1.6μm [63μin].

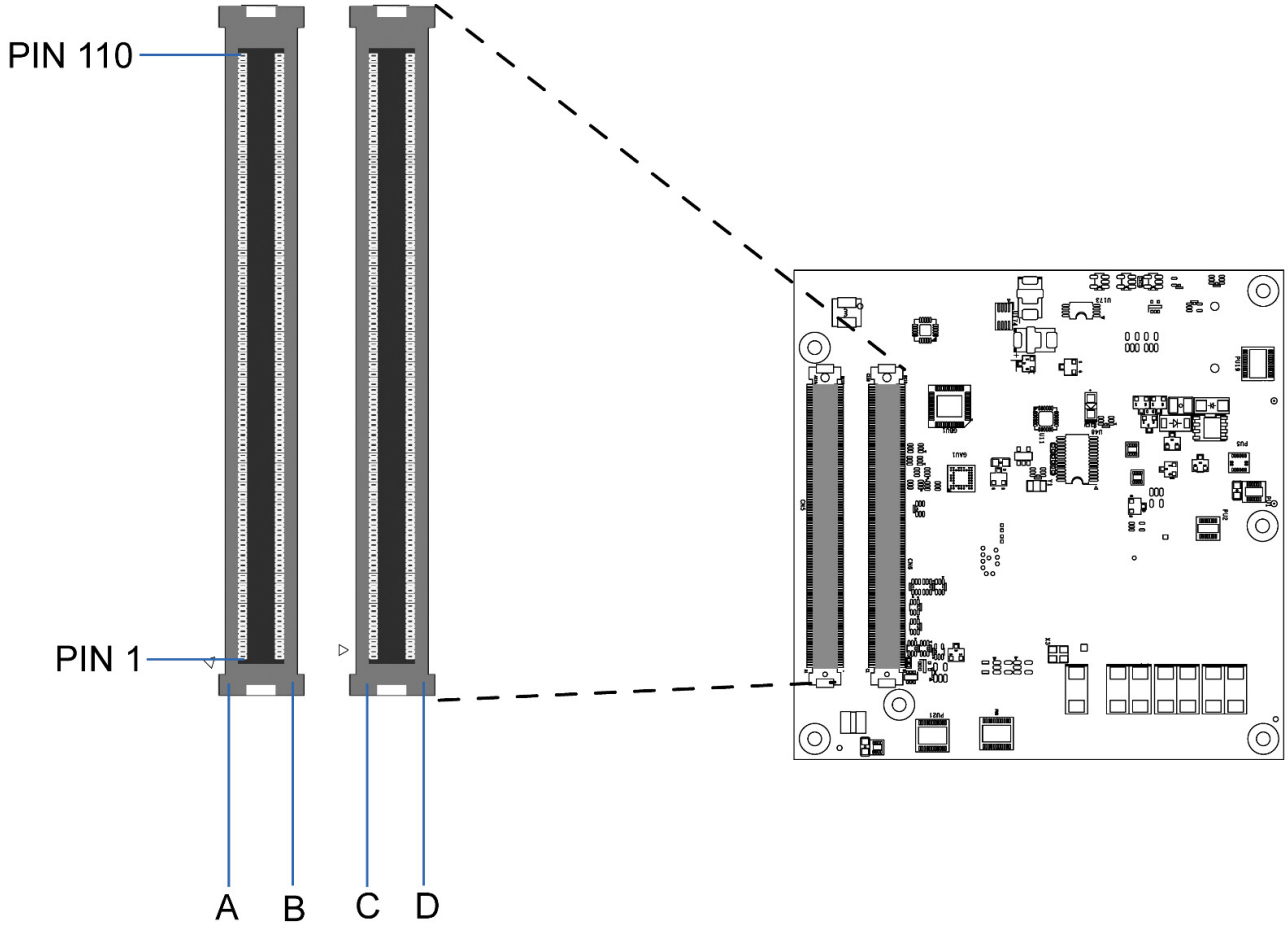
The critical dimension in Figure 6-10 is the Module PCB bottom side to heat-spreader topside. This dimension shall be 13.00mm ± 0.65mm [±0.026”].

Figure below shows a cross section of a Module and heat-spreader assembled to a Carrier Board using the 5mm stack height option. If 8mm Carrier Board connectors are used, the overall assembly height increases from 18.00mm to 21.00mm.



Thickness ´T´ is implemantation specific and may be 3mm.
Height 'H' (which includes PCB thickness) shall be 13.00mm

4. Pinout Definitions



4.1. Connector A/B

PIN	Row A	PIN	Row B
A1	**GND (FIXED)**	B1	**GND (FIXED)**
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK#	B8	LPC_DRQ0#
A9	GBE0_MDI1-	B9	LPC_DRQ1#

PIN	Row A	PIN	Row B
A10	GBE0_MDI1+	B10	LPC_CLK
A11	**GND (FIXED)**	B11	**GND (FIXED)**
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	GBE0_CTREF	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	SUS_STAT#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	**GND (FIXED)**	B21	**GND (FIXED)**
A22	SATA2_TX+	B22	SATA3_TX+
A23	SATA2_TX-	B23	SATA3_TX-
A24	SUS_S5#	B24	PWR_OK
A25	SATA2_RX+	B25	SATA3_RX+
A26	SATA2_RX-	B26	SATA3_RX-
A27	BATLOW#	B27	WDT
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1
A30	AC/HDA_RST	B30	AC/HDA_SDIN0
A31	**GND (FIXED)**	B31	**GND (FIXED)**
A32	AC/HDA_BITCLK	B32	SPKR
A33	AC/HDA_SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	**GND (FIXED)**	**B41**	**GND (FIXED)**
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#

PIN	Row A	PIN	Row B
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	EXCD1_PERST#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#
A49	EXCD0_CPPE#	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	**GND (FIXED)**	B51	**GND (FIXED)**
A52	PCIE_TX5+	B52	PCIE_RX5+
A53	PCIE_TX5-	B53	PCIE_RX5-
A54	GPI0/SD_DATA0	B54	GPO1/SD_CMD
A55	PCIE_TX4+	B55	PCIE_RX4+
A56	PCIE_TX4-	B56	PCIE_RX4-
A57	GND	B57	GPO2/SD_WP
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	**GND (FIXED)**	B60	**GND (FIXED)**
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1/SD_DATA1	B63	GPO3/SD_CD#
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	**GND**	B66	WAKE0#
A67	GPI2/SD_DATA2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	**GND (FIXED)**	B70	**GND (FIXED)**
A71	LVDS_A0+ /eDP_TX2+	B71	LVDS_B0+
A72	LVDS_A0- / eDP_TX2-	B72	LVDS_B0-
A73	LVDS_A1+ / eDP_TX1+	B73	LVDS_B1+
A74	LVDS_A1- / eDP_TX1-	B74	LVDS_B1-
A75	LVDS_A2+ / eDP_TX0+	B75	LVDS_B2+
A76	LVDS_A2- / eDP_TX0-	B76	LVDS_B2-
A77	LVDS_VDD_EN / eDP_VDD_EN	B77	LVDS_B3+
A78	LVDS_A3+	B78	LVDS_B3-
A79	LVDS_A3-	B79	LVDS_BKLT_EN / eDP_BKLT_EN

PIN	Row A	PIN	Row B
A80	**GND (FIXED)**	B80	**GND (FIXED)**
A81	LVDS_A_CK+ / eDP_TX3+	B81	LVDS_B_CK+
A82	LVDS_A_CK- / eDP_TX3-	B82	LVDS_B_CK-
A83	LVDS_I2C_CK / eDP_AUX+	B83	LVDS_BKLT_CTRL / eDP_BKLT_CTRL
A84	LVDS_I2C_DAT / eDP_AUX-	B84	VCC_5V_SBY
A85	GPI3/SD_DATA3	B85	VCC_5V_SBY
A86	RSVD	B86	VCC_5V_SBY
A87	eDP_HPD	B87	VCC_5V_SBY
A88	PCIE_CLK_REF+	B88	BIOS_DIS1#
A89	PCIE_CLK_REF-	B89	VGA_RED
A90	**GND (FIXED)**	B90	**GND (FIXED)**
A91	SPI_POWER	B91	VGA_GRN
A92	SPI_MISO	B92	VGA_BLU
A93	GPO0/SD_CLK	B93	VGA_HSYNC
A94	SPI_CLK	B94	VGA_VSYNC
A95	SPI_MOSI	B95	VGA_I2C_CK
A96	TPM_PP	B96	VGA_I2C_DAT
A97	TYPE10#	B97	SPI_CS#
A98	SER0_TX	B98	RSVD
A99	SER0_RX	B99	RSVD
A100	**GND (FIXED)**	B100	**GND (FIXED)**
A101	SER1_TX / CAN_TX	B101	FAN_PWMOUT
A102	SER1_RX / CAN_RX	B102	FAN_TACHIN
A103	LID#	B103	SLEEP#
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	**GND (FIXED)**	B110	**GND (FIXED)**

4.2. Connector C/D

PIN	Row C	PIN	Row D

PIN	Row C	PIN	Row D
C1	**GND (FIXED)**	D1	**GND (FIXED)**
C2	GND	D2	GND
C3	USB_SSRX0-	D3	USB_SSTX0-
C4	USB_SSRX0+	D4	USB_SSTX0+
C5	GND	D5	GND
C6	USB_SSRX1-	D6	USB_SSTX1-
C7	USB_SSRX1+	D7	USB_SSTX1+
C8	GND	D8	GND
C9	USB_SSRX2-	D9	USB_SSTX2-
C10	USB_SSRX2+	D10	USB_SSTX2+
C11	**GND (FIXED)**	D11	**GND (FIXED)**
C12	USB_SSRX3-	D12	USB_SSTX3-
C13	USB_SSRX3+	D13	USB_SSTX3+
C14	**GND (FIXED)**	D14	**GND (FIXED)**
C15	DDI1_PAIR6+	D15	DDI1_CTRLCLK_AUX+
C16	DDI1_PAIR6-	D16	DDI1_CTRLDATA_AUX-
C17	RSVD	D17	RSVD
C18	RSVD	D18	RSVD
C19	PCIE_RX6+	D19	PCIE_TX6+
C20	PCIE_RX6-	D20	PCIE_TX6-
C21	**GND (FIXED)**	D21	**GND (FIXED)**
C22	PCIE_RX7+	D22	PCIE_TX7+
C23	PCIE_RX7-	D23	PCIE_TX7-
C24	DDI1_HPD	D24	RSVD
C25	DDI1_PAIR4+	D25	RSVD
C26	DDI1_PAIR4-	D26	DDI1_PAIR0+
C27	RSVD	D27	DDI1_PAIR0-
C28	RSVD	D28	RSVD
C29	DDI1_PAIR5+	D29	DDI1_PAIR1+
C30	DDI1_PAIR5-	D30	DDI1_PAIR1-
C31	**GND (FIXED)**	D31	**GND (FIXED)**
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL
C35	RSVD	D35	RSVD

PIN	Row C	PIN	Row D
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+
C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-
C38	DDI3_DDC_AUX_SEL	D38	RSVD
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+
C40	DDI3_PAIR0-	D40	DDI2_PAIR0-
C41	**GND (FIXED)**	D41	**GND (FIXED)**
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+
C43	DDI3_PAIR1-	D43	DDI2_PAIR1-
C44	DDI3_HPD	D44	DDI2_HPD
C45	RSVD	D45	RSVD
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-
C48	RSVD	D48	RSVD
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+
C50	DDI3_PAIR3-	D50	DDI2_PAIR3-
C51	**GND (FIXED)**	D51	**GND (FIXED)**
C52	PEG_RX0+	D52	PEG_TX0+
C53	PEG_RX0-	D53	PEG_TX0-
C54	TYPE0#	D54	PEG_LANE_RV#
C55	PEG_RX1+	D55	PEG_TX1+
C56	PEG_RX1-	D56	PEG_TX1-
C57	TYPE1#	D57	TYPE2#
C58	PEG_RX2+	D58	PEG_TX2+
C59	PEG_RX2-	D59	PEG_TX2-
C60	**GND (FIXED)**	D60	**GND (FIXED)**
C61	PEG_RX3+	D61	PEG_TX3+
C62	PEG_RX3-	D62	PEG_TX3-
C63	RSVD	D63	RSVD
C64	RSVD	D64	RSVD
C65	PEG_RX4+	D65	PEG_TX4+
C66	PEG_RX4-	D66	PEG_TX4-
C67	RSVD	D67	GND
C68	PEG_RX5+	D68	PEG_TX5+
C69	PEG_RX5-	D69	PEG_TX5-
C70	GND (FIXED)	D70	GND (FIXED)

PIN	Row C	PIN	Row D
C71	PEG_RX6+	D71	PEG_TX6+
C72	PEG_RX6-	D72	PEG_TX6-
C73	**GND (FIXED)**	D73	**GND (FIXED)**
C74	PEG_RX7+	D74	PEG_TX7+
C75	PEG_RX7-	D75	PEG_TX7-
C76	GND	D76	GND
C77	RSVD	D77	RSVD
C78	PEG_RX8+	D78	PEG_TX8+
C79	PEG_RX8-	D79	PEG_TX8-
C80	**GND (FIXED)**	D80	**GND (FIXED)**
C81	PEG_RX9+	D81	PEG_TX9+
C82	PEG_RX9-	D82	PEG_TX9-
C83	RSVD	D83	RSVD
C84	GND	D84	GND
C85	PEG_RX10+	D85	PEG_TX10+
C86	PEG_RX10-	D86	PEG_TX10-
C87	GND	D87	GND
C88	PEG_RX11+	D88	PEG_TX11+
C89	PEG_RX11-	D89	PEG_TX11-
C90	**GND (FIXED)**	D90	**GND (FIXED)**
C91	PEG_RX12+	D91	PEG_TX12+
C92	PEG_RX12-	D92	PEG_TX12-
C93	**GND (FIXED)**	D93	**GND (FIXED)**
C94	PEG_RX13+	D94	PEG_TX13+
C95	PEG_RX13-	D95	PEG_TX13-
C96	**GND (FIXED)**	D96	**GND (FIXED)**
C97	RSVD	D97	RSVD
C98	PEG_RX14+	D98	PEG_TX14+
C99	PEG_RX14-	D99	PEG_TX14-
C100	GND (FIXED)	D100	GND (FIXED)
C101	PEG_RX15+	D101	PEG_TX15+
C102	PEG_RX15-	D102	PEG_TX15-
C103	**GND (FIXED)**	D103	**GND (FIXED)**
C104	VCC_12V	D104	VCC_12V
C105	VCC_12V	D105	VCC_12V

PIN	Row C	PIN	Row D
C106	VCC_12V	D106	VCC_12V
C107	VCC_12V	D107	VCC_12V
C108	VCC_12V	D108	VCC_12V
C109	VCC_12V	D109	VCC_12V
C110	**GND (FIXED)**	D110	**GND (FIXED)**

4.3. Signal Definition

Followings are definition for signal on connectors A/B and C/D.

I	Input signal to the module
O	Output signal from the module
I/O	Bi-directional input/output signal
OD	Open drain output
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	3.3V output signal
O 5V	5V output signal
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O 3.3Vsb	Input 3.3V tolerant active in standby state
P	Power Input/Output
REF	Reference voltage output that may be sourced from a module power plane.
PDS	Pull-down strap. This is an output pin on the module that is either tied to GND or not connected. The signal is used to indicate the PICMG module type to the Carrier Board.
PU	pull-up resistor on module
PD	pull-down resistor on module

4.4. Signal Descriptions – Connector A/B

4.4.1. Audio Signals

Signal	Pin	Description	I/O	PU/PD	Comment
AC/HDA_SYNC	A29	Sample-synchronization signal to the CODEC (s).	O 3.3V		
AC/HDA_RST#	A30	Reset output to CODEC, active low.	O 3.3V		
AC/HDA_BITCLK	A32	Serial data clock generated by the external CODEC(s).	O 3.3V		
AC/HDA_SDOUT	A33	Serial TDM data output to the CODEC.	O 3.3V		
AC/HDA_SDIN2	B28	Serial TDM data inputs from up to 3 CODECs.	I 3.3V		not connected
AC/HDA_SDIN1	B29		I 3.3V		
AC/HDA_SDIN0	B30		I 3.3V		

4.4.2. Analog VGA

Note: No VGA support on this product.

Signal	Pin	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	O Analog		not supported
VGA_GRN	B91	Green for monitor Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		not supported
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		not supported
VGA_HSYNC	B93	Horizontal sync output to VGA monitor.	O 3.3V		not supported
VGA_VSYNC	B94	Vertical sync output to VGA monitor.	O 3.3V		not supported
VGA_I2C_CK	B95	DDC clock line (I2C port dedicated to identify VGA monitor capabilities).	O 3.3V		not supported
VGA_I2C_DAT	B96	DDC data line.	I/O 3.3V		not supported

4.4.3. LVDS/eDP

Signal	Pin	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- -	A71 A72 A73 A74 A75 A76	LVDS Channel A differential pairs	O LVDS		LVDS is default. (through eDP to LVDS bridge)

Signal	Pin	Description	I/O	PU/PD	Comment
LVDS_A3+	A78				
LVDS_A3-	A79				
LVDS_A_CK+	A81	LVDS Channel A differential clock	O LVDS		
LVDS_A_CK					
LVDS_B0+	B71	LVDS Channel B differential pairs	O LVDS		**Note**: eDP support is a BOM option
LVDS_B0-	B72				
LVDS_B1+	B73				
LVDS_B1-	B74				
LVDS_B2+	B75				
LVDS_B2-	B76				
LVDS_B3+	B77				
LVDS_B3-	B78				
LVDS_B_CK+	B81	LVDS Channel B differential clock	O LVDS		
LVDS_B_CK	B82				
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10K	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10K	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V	PD 100K	ePD to LVDS requirement
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control	I/O 3.3V	PU 2k2 3.3V	

eDP BOM Optional Signal Descriptions

Signal	Pin	Description	I/O	PU/PD	Comment
eDP_TX2+	A71	eDP differential pairs	O PCIE		AC coupled off module
eDP_TX2-	A72				
eDP_TX1+	A73				
eDP_TX1-	A74				
eDP_TX0+	A75				
eDP_TX0--	A76				
eDP_TX3+	A81	eDP differential pairs	O PCIE		AC coupled off

Signal	Pin	Description	I/O	PU/PD	Comment
eDP_TX3--	A82				module
eDP_VDD_EN	A77	eDP power enable	O 3.3V	PD 10K	
eDP_BKLT_EN	B79	eDP backlight enable	O 3.3V	PD 10K	
eDP_BKLT_CTRL	B83	eDP backlight brightness control	O 3.3V	PD 100K	
eDP_AUX+	A83	eDP AUX+	I/O PCIE		AC coupled off module
eDP_AUX-	A84	eDP AUX-	I/O PCIE		AC coupled off module
eDP_HPD	A87	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	

4.4.5. Gigabit Ethernet

Signal	Pin	Description	I/O	PU/PD	Comment
GBE0_MDI0-	A12	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T / 100BASE-TX / 10BASE-T MDI[0]+/- / B1_DA+/- / TX+/- / TX+/- MDI[1]+/- / B1_DB+/ / RX+/- / RX+/- This set of differential pairs, in conjunction with the GBE1_MDI[0:3] pairs, may also be used to implement a 10 Gigabit / sec interface.	I/O Analog		Twisted pairsignals forexternaltransformer.
GBE0_MDI0+	A13				
GBE0_MDI1-	A9				
GBE0_MDI1+	A10				
GBE0_MDI2-	A6				
GBE0_MDI2+	A7				
GBE0_MDI3-	A2				
GBE0_MDI3+	A3				
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		

Signal	Pin	Description	I/O	PU/PD	Comment
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.			not connected

4.4.6. SATA

Signal	Pin	Description	I/O	PU/PD	Comment
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports SATA 3.0
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports SATA 3.0
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Receive Input differential pair.	O SATA		Supports SATA 3.0
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports SATA 3.0
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Receive Input differential pair.	O SATA		Supports SATA 3.0
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Supports SATA 3.0
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Receive Input differential pair.	O SATA		Supports SATA 3.0
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Supports SATA 3.0
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activityindicator, active low.	O 3.3V	PU 10K 3.3V	Supports SATA 3.0

Note: Core i7/i5/i3 support three SATA ports

4.4.7. PCI Express

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		PCIe port 5 is used by LAN by default. BOM option supports PCIe port5
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		PCIe port 5 is used by LAN by default. BOM option supports PCIe port5
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		

4.4.8. LPC Bus

Signal	Pin	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3VSB		Skylake platform uses standby power for LPC bus
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3VSB		Skylake platform uses standby power for LPC bus
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC serial DMA request	I 3.3V		NC. No support on Skylake-U platform
LPC_SERIRQ	A50	LPC serial interrupt	I/O OD 3.3VSB	PU 8k2 3.3V	Skylake platform uses standby power for LPC bus
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC serial DMA request	I 3.3V		NC. No support on Skylake-U platform

4.4.9. USB

Signal	Pin	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB differential data pairs for Port 0	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB1+ USB1-	B46 B45	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB2+ USB2-	A43 A42	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB3+ USB3-	B43 B42	USB differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB4+ USB4-	A40 A39	USB differential data pairs for Port 3	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB5+ USB5-	B40 B39	USB differential data pairs for Port 4	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB6+ USB6-	A37 A36	USB differential data pairs for Port 5	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB7+ USB7-	B37 B37	USB differential data pairs for Port 6	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and	I 3.3VSB	PU 10k 3.3VSB	Do not pull

Signal	Pin	Description	I/O	PU/PD	Comment
		1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.			high on carrier
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier

4.4.11. SPI (BIOS only)

Signal	Pin	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10K 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER.	O P 3.3VSB		

Signal	Pin	Description	I/O	PU/PD	Comment
		SPI_POWER shall only be used to power SPI devices on the Carrier			
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave no-connect

4.4.12. Miscellaneous

Signal	Pin	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V	PU 10K 3.3V	
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V		
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V		
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V		
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM.	O OD 3.3V	PU 2.2K 3.3V	PD shall be on the carrier board
FAN_TACHIN11	B102	Fan tachometer input for a fan with a two pulse output.	I OD 3.3V	PU 10k 3.3V	
TPM_PP	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 1k 3.3V	PD is only placed when TPM is installed on module

4.4.13. SMBus

Signal	Pin	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.	I/O OD 3.3VSB	PU 8k2 3.3VSB	

SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	I/O OD 3.3VSB	PU 8k2 3.3VSB
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	I 3.3VSB	PU 10k 3.3VSB

4.4.14. I2C Bus

Signal	Pin	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O OD 3.3VSB	PU 2k2 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O OD 3.3VSB	PU 2k2 3.3VSB	

4.4.15. General Purpose I/O (GPIO)

Signal	Pin	Description	I/O	PU/PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V	PU 10K 3.3V	After hardware RESET output low
GPO[1]	B54	General purpose output pins.	O 3.3V	PU 10K 3.3V	After hardware RESET output low
GPO[2]	B57	General purpose output pins.	O 3.3V	PU 10K 3.3V	After hardware RESET output low
GPO[3]	B63	General purpose output pins.	O 3.3V	PU 10K 3.3V	After hardware RESET output low
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the	I 3.3V	PU 10K 3.3V	

Signal	Pin	Description	I/O	PU/PD	Comment
		module.			
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	

4.4.16. Serial Interface Signals

Signal	Pin	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter (TTL level output)	O CMOS		Power rail tolerance 5V/12V PD shall be on the carrier board
SER0_RX	A99	General purpose serial port receiver (TTL level input) I CMOS	I CMOS		Power rail tolerance 5V/12V
SER1_TX / CAN_TX	A101	General purpose serial port transmitter (TTL level output)	O CMOS		Power rail tolerance 5V/12V PD shall be on the carrier board
SER1_RX / CAN_RX	A102	General purpose serial port receiver (TTL level input)	I CMOS		Power rail tolerance 5V/12V

4.4.17. Power and System Management

Signal	Pin	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power	I 3.3VSB	PU 10k 3.3VSB	

Signal	Pin	Description	I/O	PU/PD	Comment
		cycle may be used.			
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3VSB		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or other configurable devices time to be programmed.	I 3.3V	PU 100k 3.3VSB	
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as “PS_ON”) may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10k 3.3VSB	Not supported. Connected to WAKE0#
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10k 3.3VSB	

Signal	Pin	Description	I/O	PU/PD	Comment
LID#	A103	LID button. Low active signal used by the ACPI operating system for a LID switch.	I OD 3.3VSB	PU 10k 3.3VSB	Emulated on GPIO (BIOS)
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3VSB	PU 10K 3.3VSB	Emulated on GPIO (BIOS)

4.4.18. Power and Ground

Signal	Pin	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal (5 ~ 20V wide input). All available VCC_12V pins on the connector(s) shall be used.	P		5~20 V
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		5Vsb ±5%
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A66, A80, A90, A96, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path.	P		

4.5. Signal Descriptions – Connector C/D

4.5.1. USB 3.0 Extension

Signal	Pin	Description	I/O	PU/PD	Comment
USB_SSRX0-USB_SSRX0+	C3 C4	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0	I PCIE		
USB_SSTX0-USB_SSTX0+	D3 D4	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0	O PCIE		AC coupled on Module
USB_SSRX1-USB_SSRX1+	C6 C7	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1	I PCIE		
USB_SSTX1-USB_SSTX1+	D6 D7	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1	O PCIE		AC coupled on Module
USB_SSRX2-USB_SSRX2+	C9 C10	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2	I PCIE		
USB_SSTX2-USB_SSTX2+	D9 D10	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB2	O PCIE		AC coupled on Module
USB_SSRX3-USB_SSRX3+	C12 C13	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3	I PCIE		
USB_SSTX3-USB_SSTX3+	D12 D13	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB3	O PCIE		AC coupled on Module

4.5.2. PCI Express x1

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		Not supported

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		Not supported

4.5.3. DDI Channels

DDI 1

Signal	Pin	Description	I/O	PU/PD	Comment
DDI1_PAIR0+	D26				
DDI1_PAIR0-	D27				
DDI1_PAIR1+	D29				
DDI1_PAIR1-	D30				
DDI1_PAIR2+	D32				
DDI1_PAIR2-	D33				
DDI1_PAIR3+	D36	Digital Display Interface1 differential	O PCIE		Pair 4 to Pair 6
DDI1_PAIR3-	D37	pairs			Not supported
DDI1_PAIR4+	C25				
DDI1_PAIR4-	C26				
DDI1_PAIR5+	C29				
DDI1_PAIR5-	C30				
DDI1_PAIR6+	C15				
DDI1_PAIR6-	C16				
DDI1_HPD	C24	Digital Display Interface Hot-Plug Detect	I PCIE	PD 100K	
DDI1_CTRLCLK_AUX+	D15	IF DDI1_DDC_AUX_SEL is floating	I/O PCIe		DP1_AUX+
		IF DDI1_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI1_CTRLCLK
DDI1_CTRLDATA_AUX-	D16	IF DDI1_DDC_AUX_SEL is floating	I/O PCIe		DP1_AUX+
		IF DDI1_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI1_CTRLDATA
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA	I/O OD 3.3V	PD 1M	

Signal	Pin	Description	I/O	PU/PD	Comment
		signals.			

DDI 2

Signal	Pin	Description	I/O	PU/PD	Comment
DDI2_PAIR0+	D39				
DDI2_PAIR0-	D40				
DDI2_PAIR1+	D42				
DDI2_PAIR1-	D43	Digital Display Interface2 differential			
DDI2_PAIR2+	D46	pairs			
DDI2_PAIR2-	D47				
DDI2_PAIR3+	D49				
DDI2_PAIR3-	D50				
DDI2_HPD	D44			PD 100K	
DDI2_CTRLCLK_AUX+	C32	IF DDI2_DDC_AUX_SEL is floating	I/O PCIe		DP2_AUX+
		IF DDI2_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI2_CTRLCLK
DDI2_CTRLDATA_AUX-	C33	IF DDI2_DDC_AUX_SEL is floating	I/O PCIe		DP2_AUX+
		IF DDI2_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI2_CTRLDATA
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.		PD 1M	

DDI 3

Signal	Pin	Description	I/O	PU/PD	Comment
DDI3_PAIR0+	C39				
DDI3_PAIR0-	C40				
DDI3_PAIR1+	C42	Digital Display Interface3 differential			Not supported
DDI3_PAIR1-	C43	pairs			
DDI3_PAIR2+	C46				
DDI3_PAIR2-	C47				

Signal	Pin	Description	I/O	PU/PD	Comment
DDI3_PAIR3+	C49				
DDI3_PAIR3-	C50				
DDI3_HPD	C44			PD	Not supported
DDI3_CTRLCLK_AUX+	C36	IF DDI3_DDC_AUX_SEL is floating	I/O PCIe		Not supported
		IF DDI3_DDC_AUX_SEL pulled high	I/O OD 3.3V		Not supported
DDI3_CTRLDATA_AUX-	C37	IF DDI3_DDC_AUX_SEL is floating	I/O PCIe		Not supported
		IF DDI3_DDC_AUX_SEL pulled high	I/O OD 3.3V		Not supported
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.		PD 1M	Not supported

4.5.4. DDI to DP/HDMI/SDVO Mapping

Pin	Pin Name	DP	HDMI\DVI
D26	DDI1_PAIR0+	DP1_LANE0+	TMDS1_DATA2+
D27	DDI1_PAIR0-	DP1_LANE0-	TMDS1_DATA2-
D29	DDI1_PAIR1+	DP1_LANE1+	TMDS1_DATA1+
D30	DDI1_PAIR1-	DP1_LANE1-	TMDS1_DATA1-
D32	DDI1_PAIR2+	DP1_LANE2+	TMDS1_DATA0+
D33	DDI1_PAIR2-	DP1_LANE2-	TMDS1_DATA0-
D36	DDI1_PAIR3+	DP1_LANE3+	TMDS1_CLK+
D37	DDI1_PAIR3-	DP1_LANE3-	TMDS1_CLK
C25	DDI1_PAIR4+	Not supported	Not supported
C26	DDI1_PAIR4-	Not supported	Not supported
C29	DDI1_PAIR5+	Not supported	Not supported
C30	DDI1_PAIR5-	Not supported	Not supported
C15	DDI1_PAIR6+	Not supported	Not supported
C16	DDI1_PAIR6-	Not supported	Not supported
C24	DDI1_HPD	DP1_HPD	HDMI1_HPD
D15	DDI1_CTRLCLK_AUX+	DP1_AUX+	HMDI1_CTRLCLK

D16	DDI1_CTRLDATA_AUX-	DP1_AUX	HMDI1_CTRLDATA
D34	DDI1_DDC_AUX_SEL	DP1_LANE0+	TMDS1_DATA2+
D39	DDI2_PAIR0+	DP2_LANE0+	TMDS2_DATA2+
D40	DDI2_PAIR0-	DP2_LANE0-	TMDS2_DATA2-
D42	DDI2_PAIR1+	DP2_LANE1+	TMDS2_DATA1+
D43	DDI2_PAIR1-	DP2_LANE1-	TMDS2_DATA1-
D46	DDI2_PAIR2+	DP2_LANE2+	TMDS2_DATA0+
D47	DDI2_PAIR2-	DP2_LANE2-	TMDS2_DATA0-
D49	DDI2_PAIR3+	DP2_LANE3+	TMDS2_CLK+
D50	DDI2_PAIR3-	DP2_LANE3-	TMDS2_CLK-
D44	DDI2_HPD	DP2_HPD	HDMI2_HPD
C32	DDI2_CTRLCLK_AUX+	DP2_AUX+	HDMI2_CTRLCLK
C33	DDI2_CTRLDATA_AUX-	DP2_AUX-	HDMI2_CTRLDATA
C34	DDI2_DDC_AUX_SEL		

4.5.5. Module Type Definition

<table>
<tr><th>Signal</th><th>Pin</th><th colspan="5">Description</th><th>I/O</th><th>PU/PD</th><th>Comment</th></tr>
<tr><td rowspan="2">TYPE0#</td><td rowspan="2">C54</td><td colspan="5" rowspan="2">The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10, these pins are not present (X).</td><td rowspan="2">PDS</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr></tr>
<tr><td rowspan="7">TYPE1#</td><td rowspan="7">C57</td><td>TYPE2#</td><td>TYPE1#</td><td>TYPE0#</td><td colspan="2"></td><td rowspan="7">PDS</td><td rowspan="7"></td><td rowspan="7"></td></tr>
<tr><td>X</td><td>X</td><td>X</td><td colspan="2">Pin-out Type1</td></tr>
<tr><td>NC</td><td>NC</td><td>NC</td><td colspan="2">Pin-out Type2</td></tr>
<tr><td>NC</td><td>NC</td><td>GND</td><td colspan="2">Pin-out Type3 (no IDE)</td></tr>
<tr><td>NC</td><td>GND</td><td>NC</td><td colspan="2">Pin-out Type4 (no PCI)</td></tr>
<tr><td>NC</td><td>GND</td><td>GND</td><td colspan="2">Pin-out Type5 (no IDE, no PCI)</td></tr>
<tr><td>GND</td><td>NC</td><td>NC</td><td colspan="2">Pin-out Type6 (no IDE, no PCI)</td></tr>
<tr><td>TYPE2#</td><td>D57</td><td colspan="5">The Carrier Board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible Module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.</td><td>PDS</td><td>PD, 0 ohm</td><td></td></tr>
</table>

4.5.6. Power and Ground

Signal	Pin	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal (5 ~ 20V wide input). All available VCC_12V pins on the connector(s) shall be used.	P		5~20 V
GND	C1, C11, C21, C31, C41, C51, C60, C70, C76, C80,C84, C87, C90, C93, C96,C100, C103, C110, D1,D11, D21, D31, D41, D51,D60, D67, D70, D76, D80,D84, D87, D90, D93, D96,D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrierboard GND plane.			

5. System Resources

5.1. System Memory Map

Address Range(decimal)	Address Range(hex)	Size	Description
(4GB-16MB)	FF000000 – FFFFFFFF	16 MB	High BIOS Area
(4GB-18MB) – (4GB-17MB-1)	FEE00000 – FEEFFFFF	1 MB	MSI Interrupts
(4GB-20MB) – (4GB-19MB-1)	FEC00000 – FECFFFFF	1 MB	APIC Configuration Space
15MB – 16MB	F00000 – FFFFFF	1 MB	ISA Hole
1MB -15MB	100000 -EFFFFF	14 MB	Main Memory
0K –1MB	00000 – FFFFFF	1 MB	DOS Compatibility Memory

5.2. I/O Map

Hex Range	Device
000-01F	N/A
020-02D and 030-03F	Interrupt controller 1, 8259 equivalent
02E-02F	LPC SIO () configuration index/data registers
040-043	Timer, 8254-2 equivalent
04e-04f	LPC SIO () configuration index/data registers
050-053	Timer, 8254-2 equivalent
060, 064,	8742 equivalent (keyboard)
061	NMI control and status
070-077	Real Time Clock Controller(bit 7 -NMI mask)
80	Port 80 debugger
081-090	N/A
092	Reset (Bit 0)/ Fast Gate A20 (Bit 1)
091 ， 93-9F	N/A
0A0-0B1 and 0B4-0BD	Interrupt controller 2, 8259 equivalent
0B2 and 0B3	APM control and status port respectively
0C0-0DF	N/A
0E0-0EF	N/A
0F0	Co-processor error register
0F1-0FF	N/A

Hex Range	Device
100-169	N/A
170-177	N/A
178-1EF	N/A
1F0-1F7	N/A
1F8-2DF	N/A
2E0-2E7	Available
2E8 -2EF	Serial Port 4
2F0-2F7	Available
2F8-2FF	Serial Port 2
300-36F	Available
376	Available
378-37F	Available
380-3AF	Available
3B0-3BB and 3BF	Mono/VGA mode video
3BC-3BE	Reserved for parallel port
3C0-3DF	VGA registers
3E0-3E7	Available
3E8-3Ef	Serial Port 3
3F0-3F7	Available
3F8-3FF	Serial port 1
400	Alias for ICH TCO base address.
4D0,4D1	Interrupt controller
CF8-CFB	PCI configuration address register (32 bit I/O only)
CF9	Reset Control register (8 bit I/O)
CFC-CFF	PCI configuration data register
F040	Smbus base address for SB.
1800	PM (ACPI) Base Address for SB
0A00~0AFF	Reserved for SIO functions base address (ex: PME /GPIO etc)

5.3. Interrupt Request (IRQ) Lines

5.3.1. PIC Mode

IRQ#	Typical interrupt Resources	Connected to Pin	Available
0	Counter 0	N/A	No

1	Keyboard controller	IRQ1 via SERIRQ	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2)	IRQ3 via SERIRQ / PIRQ	Note (1)
4	Serial Port 1 (COM1)	IRQ4 via SERIRQ / PIRQ	Note (1)
5	Serial Port 4 (COM4)	IRQ5 via SERIRQ / PIRQ	Note (1)
6	Generic	IRQ6 via SERIRQ / PIRQ	No
7	Generic	IRQ7 via SERIRQ / PIRQ	Note (1)
8	Real-time clock	N/A	No
9	Generic	N/A	Note (1)
10	Serial Port 3 (COM3)	IRQ10 via SERIRQ / PIRQ	Note (1)
11	Generic	IRQ11 via SERIRQ / PIRQ	Note (1)
12	PS/2 Mouse	IRQ12 via SERIRQ / PIRQ	Note (1)
13	FERR# logic	N/A	No
14	Generic	IRQ14 via SERIRQ / PIRQ	Note (1)
15	Generic	IRQ15 via SERIRQ / PIRQ	Note (1)

Note (1): These IRQs can be used for PCI devices when onboard device is disabled.

5.3.2. APIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	IRQ1 via SERIRQ	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2)	IRQ3 via SERIRQ	Note (1)
4	Serial Port 1 (COM1	IRQ4 via SERIRQ	Note (1)
5	Serial Port 4 (COM4)	IRQ5 via SERIRQ	Note (1)
6	N/A	N/A	Note (1)
7	N/A	N/A	Note (1)
8	Real-time clock	N/A	No
9	N/A	IRQ9 via SERIRQ	Note (1)
10	Serial Port 3 (COM3)	IRQ10 via SERIRQ	Note (1)
11	N/A	N/A	Note (1)
12	PS/2 Mouse	IRQ12 via SERIRQ	Note (1)
13	FERR# logic	N/A	Note (1)

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
14	N/A	N/A	Note (1)
15	N/A	N/A	Note (1)
16	N/A	P.E.G Root Port, Intel HDA, PCIE Port 0/1/2/3/4/5/6, I.G.D, XHCI Controller, Gbe Controller, SMBus Controller	Note (1)
17	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)
18	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port	Note (1)
19	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)
20	N/A	N/A	Note (1)
21	N/A	N/A	Note (1)
22	N/A	N/A	Note (1)
23	N/A	XHCI Controller	Note (1)

Note (1): These IRQs can be used for PCI devices when onboard device is disabled.

5.4. PCI Configuration Space Map

Bus Number	Device Number	Function Number	Routing	Description
00h	00h	00h	N/A	Intel host Bridge
00h	01h	00h	Internal	Intel PCI Express Graphics port
00h	02h	00h	Internal	Intel I.G.D
00h	08h	00h	Internal	Gaussian Mixture Model
00h	14h	00h	Internal	xHCI Controller
00h	16h	00h	Internal	Intel Management Engine Interface
00h	17h	00h	Internal	Intel AHCI controller
00h	1Ch	00h	Internal	Intel PCI Express Root port 1
00h	1Dh	00h	Internal	Intel PCI Express Root port 9
00h	1Dh	01h	Internal	Intel PCI Express Root port 10
00h	1Dh	02h	Internal	Intel PCI Express Root port 11
00h	1Dh	03h	Internal	Intel PCI Express Root port 12
00h	1Fh	00h	N/A	Intel LPC Interface Bridge

Bus Number	Device Number	Function Number	Routing	Description
00h	1Fh	02h	Internal	Memory Controller
00h	1Fh	03h	Internal	HDA Controller
00h	1Fh	04h	Internal	SMBUS Controller
00h	1Fh	06h	Internal	Ethernet Controller

5.5. PCI Interrupt Routing Map

INT Line	P.E.G Root Port	xHCI Controller	ME Controller #1	GbE Controller	HD Audio Controller
Int0	N/A	INTA:16	INTA:16	INTA:16	INTA:16
Int1	N/A		INTD:19		
Int2	N/A		INTC:18		
Int3	N/A	INTD:19	INTB:17		
INT Line	**PCIE Port1**	**PCIE Port9**	**PCIE Port10**	**PCIE Port11**	**PCIE Port12**
Int0	INTA:16	INTB:17	INTC:18	INTD:19	INTA:16
Int1	INTB:17	INTC:18	INTD:19	INTA:16	INTB:17
Int2	INTC:18	INTD:19	INTA:16	INTB:17	INTC:18
Int3	INTD:19	INTA:16	INTB:17	INTC:18	INTD:19
INT Line	**LPC Controller**	**SATA Controller**	**SMBus Controller**	**Thermal Subsystem**	
Int0	INTA:16	INTA:16	INTA:16		
Int1	INTB:17				
Int2	INTC:18			INTC:18	
Int3	INTD:19				

5.6. SMBus Address Table

Device	Address
DIMMA	A0h
DIMMB	A4h
Extend GPIO	E8h

6. BIOS Setup

The following sections describe the BIOS setup. BIOS settings of this module can be viewed and set via BIOS settings. It is strongly recommended that only users with profound experience are allowed to change the default BIOS settings.

►Main	BIOS Information
	Memory Information
	► System Date and Time
►Advanced	► Trusted Computing
	► CPU Configuration
	► ACPI Settings
	► AMT Configuration
	► PCH-FW Configuration
	► SMART Settings
	► W83627DHG Super IO Configuration
	► NCT5104DSEC Super IO Configuration
	► NCT7802Y HW Monitor
	► CSM Configuration
	► NVMe Configuration
	► USB Configuration
	► SATA Configuration
	► Trusted Computing
►Chipset	► System Agent (SA) Configuration
	► PCH-IO Configuration
Boot	Boot Configuration
Security	Password Description
►Save & Exit	Save Options
	Default Options

6.1. Main

6.1.1. BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	BIOS source code provider.
Core Version	Info only	AMI BIOS core version.
Compliancy	Info only	Compliance with UEFI version.
Project Version	Info only	WIN BIOS version.
Build Date and Time	Info only	WIN date the BIOS was build.

6.1.2. Memory Information

Feature	Options	Description
Total Memory	Info only	Display installed memory size.

6.1.3. Date and Time

Feature	Options	Description
System Date	Week-day, MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds

6.2. Advanced

6.2.1. Trusted Computing

Feature	Options	Description
Security Device Support	**Enabled** Disabled	Enables or Disables BIOS support for security device. When disabled OS will not show Security Device. TCG EFI protocol and INT1A interface will not be available
TPM State	**Enabled**	Enable/Disable Security Device. NOTE: Your Computer will

	Disabled	reboot during restart in order to change State of the Device.
Pending operation	**None** TPM Clear	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.
Select Device Type	TPM 1.2 TPM 2.0 **Auto**	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

6.2.2. CPU Configuration

Feature	Options	Description
CPU	Info only	Manufacturer, model, speed
CPU Signature	Info only	Display CPU Signature.
Microcode Patch	Info only	Display Microcode Patch.
Max CPU speed	Info only	Display Max CPU speed.
Min CPU speed	Info only	Display Min CPU speed.
CPU Speed	Info only	Display CPU Speed.
Processor Cores	Info only	Display Processor Cores.
Hyper Threading Technology	Info only	Display Intel HT Technology support or not.
Intel VT-x Technology	Info only	Display Intel VT-x Technology support or not.
Intel SMX Technology	Info only	Display Intel SMX Technology support or not.
64-bit	Info only	Display 64-bit support or not.
EIST Technology	Info only	Display EIST Technology support or not
CPU C3 state	Info only	Display CPU C3 state support or not
CPU C6 state	Info only	Display CPU C6 state support or not
CPU C7 state	Info only	Display CPU C7 state support or not
CPU C8 state	Info only	Display CPU C8 state support or not
CPU C9 state	Info only	Display CPU C9 state support or not
CPU C10 state	Info only	Display CPU C10 state support or not
L1 Data Cache	Info only	Display cache info.

Feature	Options	Description
L1 Code Cache	Info only	Display cache info.
L2 Cache	Info only	Display cache info.
L3 Cache	Inf o only	Display cache info.
L4 Cache	Inf o only	Display cache info.
Hyper-threading	Disabled **Enabled**	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.
Active Processor Cores	**All** 1 2 3	Number of cores to enable in each processor package.
Intel Virtualization Technology	Disabled **Enabled**	Enable/Disable support for the Intel virtualization technology.
Hardware Prefetcher	Disabled **Enabled**	Enable the Mid Level Cache (L2) streamer prefetcher.
Adjacent Cache Line Prefetch	Disabled **Enabled**	Enable the Mid Level Cache (L2) prefetching of adjacent cache lines.
CPU AES	Disabled **Enabled**	Enable/Disable CPU Advanced Encryption Standard instructions
Boot performance mode	Max Battery **Max Non-Turbo Performance** Turbo Performance	Select the performance state that the BIOS will set before OS handoff.
Intel(R) Speed Shift Technology	Disabled **Enabled**	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.
Intel(R) SpeedStep(TM)	Disabled **Enabled**	Allows more than two frequency ranges to be supported.
Turbo Mode	Disabled **Enabled**	Enable/Disable turbo mode.
CPU C state	Disabled **Enabled**	Enable or disable CPU C states
Enhanced C-states	Disabled **Enabled**	Enable/Disable C1E. When enabled, CPU will switch to minimum speed when all cores enter C-State.

6.2.3. ACPI Settings

Feature	Options	Description
Enable Hibernation	Disabled **Enabled**	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select ACPI sleep state the system will enter when the SUSPEND button is pressed.

6.2.4. AMT Configuration

Feature	Options	Description
Intel AMT	Disabled **Enabled**	Enable/Disable Intel (R) Active Management Technology BIOS Extension. Note : iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device
BIOS Hotkey Pressed	**Disabled** Enabled	Enable/Disable BIOS hotkey press.
MEBx Selection Screen	**Disabled** Enabled	Enable/Disable MEBx selection screen.
Hide Un-Configure ME Confirmation Prompt	**Disabled** Enabled	Hide Un-Configure ME without password Confirmation Prompt
MEBx Debug Message Output	**Disabled** Enabled	Enable MEBx debug message output.
Un-Configure ME	**Disabled** Enabled	Un-Configure ME without password.
Amt Wait Timer	0 - 65535	Set timer to wait before sending ASF_GET_BOOT_OPTIONS.
ASF	Disabled **Enabled**	Enable/Disable Alert Specification Format.
Activate Remote Assistance Process	**Disabled** Enabled	Trigger CIRA boot.
USB Provisioning of AMT	Disabled **Enabled**	Enable/Disable of AMT USB Provisioning.
PET Progress	Disabled **Enabled**	User can Enable/Disable PET Events progress to recieve PET events or not.

Feature	Options	Description
AMT CIRA Timeout	0	OEM defined timeout for MPS connection to be established. * 0 - use the default timeout value of 60 seconds. * - MEBX waits until the connection succeeds
WatchDog	**Disabled** Enabled	Enable/Disable WatchDog Timer.
OS Timer		Set OS watchdog timer.
BIOS Timer		Set BIOS watchdog timer.

6.2.5. PCH-FW Configuration

Feature	Options	Description
ME Unconfig on RTC Clear State	**Enabled** Disabled	Disabling this option will cause ME not to unconfigure on RTC clear

6.2.6. W83627DHG Super IO Configuration

Feature	Options	Description
W83627DHG Super IO Configuration	Info only	
Super IO Chip	Info only	

Feature	Options	Description
Serial Port 1 Configuration Serial Port	Submenu	
Serial Port	**Enabled** Disabled	Enable or Disable Serial Port (COM)
Device Settings	IO=3F8h; IRQ=4	Fixed configuration of serial port.
Change Settings	**Auto** IO=3F8h; IRQ=4 IO=3F8h;IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h;IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h;IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h;IRQ=3,4,5,6,7,9,10,11,12	Select an optimal settings for Super IO device.
Serial Port 2 Configuration Serial Port	Submenu	
Serial Port	**Enabled** Disabled	Enable or Disable Serial Port (COM)
Disabled"	IO=2F8h; IRQ=3	Fixed configuration of serial port.
Device Settings	**Auto** IO=2F8h; IRQ=3	Select an optimal settings for Super IO

			IO=3F8h;IRQ=3,4,5,6,7,9,10,11,12 device. IO=2F8h;IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h;IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h;IRQ=3,4,5,6,7,9,10,11,12
		Change Settings	**Standard Serial Port Mode** IrDA Active pulse 1.6 uS IrDA Active pulse 3/16 bit time ASKIR Mode
Watchdog Function	Info only		
Watchdog Mode	**Sec.** Min.	Watchdog Mode (Second / Minute)	
Watchdog Timer	0	Watchdog count timer. 00 is disable, 01 occurs after 1 minute only.	
Watchdog count	Info only	Watchdog countdown value.	

6.2.7. NCT7802Y HW Monitor

Feature	Options	Description		
Pc Health Status	Info only			
Smart Fan Function	Disabled **Enabled**	Enable or Disable Smart Fan		
Smart Fan Mode Configuration	Submenu	Feature	Options	Description
		CPU Fan Control	**Smart Duty-Cycle Mode** Manual Duty Mode	Smart Fan Mode Select
		Temperature 1	35	Specifies the temperature threshold at which the H/W monitor turns on CPU fan with specific PWM duty cycle 1.
		Temperature 2	45	Specifies the temperature threshold at which the H/W monitor turns on CPU fan with specific PWM duty cycle 2.
		Temperature 3	55	Specifies the temperature threshold at which the H/W monitor turns on CPU fan with specific PWM duty cycle 3.
		Temperature 4	65	Specifies the temperature threshold at which the H/W monitor turns on CPU fan with specific PWM duty cycle 4.
		~~Duty Cycle 1~~	~~45~~	~~Select the PWM percentage of duty~~

				cycle 1.
		Duty Cycle 2	55	Select the PWM percentage of duty cycle 2.
		Duty Cycle 3	65	Select the PWM percentage of duty cycle 3.
		Duty Cycle 4	80	Select the PWM percentage of duty cycle 4.
CPU temperature	Read only	Display CPU current temperature.		
CPU Fan Speed	Read only	Display CPU fan speed.		
VCC	Read only	Display actual voltage of the V3.30.		
+5V	Read only	Display actual voltage of the V5.00.		
Vcore	Read only	Display actual voltage of the Vcore.		
+1.2V	Read only	Display actual voltage of the V1.2.		
+1.05V	Read only	Display actual voltage of the V1.05.		

6.2.8. NVMe Configuration

Feature	Options	Description
NVME controller and Drive information	Info Only	

6.2.9.USB Configuration

Feature	Options	Description
USB Configuration	Info only	
USB Module Version	Info only	
USB Controllers	Info only	X XHCI
USB Devices	Info only	X Drive, X Keyboards, X Mouse, X Hubs
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by

		the XHCI OS driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable/Disable USB Mass Storage Driver Support.
USB hardware delays and time-outs:	Info only	
USB transfer time-out	1 sec 5 sec 10 sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
Mass Storage Devices	Info only	List current USB max stroge device.

6.2.10. SATA Configuration

Feature	Options	Description
SATA Controller(s)	**Enabled** Disabled	Enable or disable SATA Device.
SATA Mode Selection	**AHCI** RAID	Determines how SATA controller(s) operate.
Software Feature Mask Configuration	Submenu	

Feature	Options	Description
RAID0	Disabled **Enabled**	Enable or Disable RAID0 feature.
RAID1	Disabled **Enabled**	Enable or Disable RAID1 feature.
RAID10	Disabled **Enabled**	Enable or Disable RAID10 feature.
RAID5	Disabled **Enabled**	Enable or Disable RAID5 feature.
OROM UI Normal	**2 Seconds**	Select the delay time of the

		Delay	4 Seconds 6 Seconds 8 Seconds	OROM UI Splash Screen in a normal status.

Aggressive LPM Support	**Enabled** Disabled	Enable PCH to aggressively enter link power state.
Serial ATA Port 0	Info only	
Software Preserve	Info only	
Port 0	Disabled **Enabled**	Enable or Disable SATA Port
Serial ATA Port 1	Info only	
Software Preserve	Info only	
Port 1	Disabled **Enabled**	Enable or Disable SATA Port
Serial ATA Port 2	Info only	
Software Preserve	Info only	
Port 2	Disabled **Enabled**	Enable or Disable SATA Port

6.2.11. System Agent (SA) Configuration

Feature	Options	Description
System Agent Bridge Name	Info only	Display System Agent Bridge name.
SA PCIe Code Version	Info only	
VT-d	Info only	Check VT-d function on System Agent.
VT-d	Disabled **Enabled**	VT-d capability.

Graphics Configuration — Submenu

Feature	Options	Description
Graphics Configuration	Info only	
IGFX VBIOS Version	Info only	Display VBIOS Version.
Skip Scaning of External Gfx Card	**Disabled** Enabled	If Enable, it will not scan for External Gfx Card on PEG and PCH PCIE Ports
Primary Display	**Auto** IGFX PEG PCIE	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.

Internal Graphics	**Auto** Disabled Enable	Keep IGFX enabled based on the setup options.
GTT Size	2MB 4MB **8MB**	Select the GTT Size.
Aperture Size	128MB **256MB** 512MB 1024MB 2048MB 4096MB	Select the Aperture Size Note : Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM Support.
DVMT Pre-Allocated	**XXM**	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
DVMT Total Gfx Mem	**XXXM**	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.

LCD Control	Submenu	**Feature**	**Options**	**Description**
		LCD Control	**Info only**	
		LCD Panel Type	**VBIOS Default** 640X480 LVDS 800X600 LVDS 1024X768 LVDS 1280X1024 LVDS 1400X1050 LVDS1 1400X1050 LVDS2 1600X1200 LVDS 1366X768 LVDS 1680X1050 LVDS 1920X1200 LVDS 1440X900 LVDS 1600X900 LVDS 1280X800 LVDS 1920X1080 LVDS 2048X1536 LVDS	Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.
		~~Panel~~	~~**Auto**~~	~~Select the LCD~~

	Scaling	Off Force Scaling	panel scaling option used by the Internal Graphics Device.
	Backlight Control	PWM Inverted PWM Normal	Back Light Control Setting.
	Active LFP	**Disabled** Enabled	Configuring LFP usage
	Panel Color Depth	**18 Bit** 24 Bit	Select the LFP Panel Color Depth

PEG Port Configuration Submenu	**Feature**	**Options**	**Description**
	PEG Port Configuration	Info only	
	PEG 0:1:0	**Not Present**	Display PEG0 present or not.
	Enable Root Port	Disabled Enabled **Auto**	Enable or Disable the Root Port.
	Max Link Speed	**Auto** Gen1 Gen2 Gen3	Configure PEG 0:1:0 Max Speed
	PEG 0:1:1	**Not Present**	Display PEG1 present or not.
	Enable Root Port	Disabled Enabled **Auto**	Enable or Disable the Root Port.
	Max Link Speed	**Auto** Gen1 Gen2 Gen3	Configure PEG 0:1:1 Max Speed
	PEG 0:1:2	**Not Present**	Display PEG2 present or not.
	Enable Root Port	Disabled Enabled **Auto**	Enable or Disable the Root Port.

		Max Link Speed	**Auto** Gen1 Gen2 Gen3	Configure PEG 0:1:2 Max Speed

		Feature	Options	Description
GT - Power Management Control	Submenu	GT - Power Management Control	Info only	
		GT Info	Info only	Display Processor Graphics Technology (GT) Info.
		RC6(Render Standby)	Disabled **Enabled**	Check to enable render standby support.

6.2.12. PCH-IO Configuration

Feature	Options	Description
Intel PCH RC Version	Info only	Display Intel PCH RC Version.
Intel PCH SKU Name	Info only	Display Intel PCH Name.
Intel PCH Rev ID	Info only	Display Intel PCH Revision ID.

		Feature	Options	Description		
PCI Express Configuration	Submenu	PCI Express Configuration	Info only			
		PCI Express Clock gating	Disable **Enable**	Enable or disable PCI Express Clock Gating for each root port.		
		DMI Link ASPM Control	Disable **Enable**	Enable/Disable the control of Active State Power Management on SA side of the DMI link.		
		PCI Express Root Port 1	Submenu	PCI Express Root Port X	Disabled **Enabled**	Control the PCI Express Root Port.
				PCIe Speed	**Auto** Gen1 Gen2 Gen3	Select PCI Express port speed.
		PCI Express Root Port 2	Submenu	PCI Express Root Port X	Disabled **Enabled**	Control the PCI Express Root Port.
				PCIe Speed	**Auto** Gen1 Gen2 Gen3	Select PCI Express port speed.

		PCI Express Root Port 3	Submenu	PCI Express Root Port X	Disabled **Enabled**	Control the PCI Express Root Port.
				PCIe Speed	**Auto** Gen1 Gen2 Gen3	Select PCI Express port speed.
		PCI Express Root Port 4	Submenu	PCI Express Root Port X	Disabled **Enabled**	Control the PCI Express Root Port.
				PCIe Speed	**Auto** Gen1 Gen2 Gen3	Select PCI Express port speed.
		PCIE Port 5 is assigned to LAN	Info only			
		PCI Express Root Port 6	Submenu	PCI Express Root Port X	Disabled **Enabled**	Control the PCI Express Root Port.
				PCIe Speed	**Auto** Gen1 Gen2 Gen3	Select PCI Express port speed.

		Feature	**Options**	**Description**
USB Configuration	Submenu	USB Configuration	Info only	
		USB Precondition	Enabled **Disabled**	Precondition work on USB host controller and root ports for faster enumeration.
		XHCI Disable Compliance Mode	**FALSE** TRUE	Options to disable Compliance Mode. Default is FALSE to not disable Compliance Mode. Set TRUE to disable Compliance Mode.
		USB Port Disable Override	**Disabled** Select Pre-Pin	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.

		Feature	**Options**	**Description**
HD Audio Configuration	Submenu	HD Audio Configuration	Info only	
		HD Audio	Disabled Enabled **Auto**	Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled

		Auto = HDA will be enabled if present, disabled otherwise.
PCH LAN Controller	**Enabled** Disabled	Enable or disable onboard NIC.
Wake On LAN	**Enabled** Disabled	Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)
State After G3	**S0 State** S5 State	Specify what state to go to when power is re-applied after a power failure (G3 state).

6.3. Boot

Boot Configuration

Feature	Options	Description
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the keyboard NumLock state
Quiet Boot	**Disabled** Enabled	Enables or disables Quiet Boot option
Boot Option filter	**UEFI and Legacy** Legacy only UEFI only	This option controls Legacy/YEFI ROMs priority
Boot Option Priorities	Info only	
Boot Option #**X**	Selection	Sets the system boot orde

6.4. Security

Password Description

Feature	Options	Description
Password Description	Info only	Info only
Administrator Password	Enter password	Set Administrator Password
User Password	Enter password	Set User Password

6.5. Save & Exit

Save Options

Feature	Options	Description

Save Changes and Reset	Reset the system after saving the changes.
Discard Changes and Reset	Reset system setup without saving any changes.

Default Options

Feature	Options	Description
Restore Defaults		Restore/Load Default values for all the setup options.

Boot Override

Feature	Options	Description
Boot Override	Info only	

7. BIOS Checkpoints, Beep Codes

7.1. Status Code Ranges

Status Code Range	Description
0x01-0x0F	SEC Status Codes & Errors
0x10-0x2F	PEI execution up to and including memory detection
0x30-0x4F	PEI execution after memory detection
0x50-0x5F	PEI errors
0x60-0xCF	DXE execution up to BDS
0xD0-0xDF	DXE errors
0xE0-0xE8	S3 Resume (PEI)
0xE9-0xEF	S3 Resume errors (PEI)
0xF0-0xF8	Recovery (PEI)
0xF9-0xFF	Recovery errors (PEI)

7.2. Standard Status Codes

7.2.1. SEC Status Codes

Status Code Range	Description
	Not used
Progress Codes	
0x1	Power on. Reset type detection (soft/hard).
0x2	AP initialization before microcode loading
0x3	North Bridge initialization before microcode loading
0x4	South Bridge initialization before microcode loading
0x5	OEM initialization before microcode loading
0x6	Microcode loading
0x7	AP initialization after microcode loading
0x8	North Bridge initialization after microcode loading
0x9	South Bridge initialization after microcode loading
0xA	OEM initialization after microcode loading
0xB	Cache initialization
SEC Error Codes	

0xC – 0xD	Reserved for future AMI SEC error codes
0xE	Microcode not found
0xF	Microcode not loaded

7.2.2. SEC Beep Codes

N/A

7.2.3. PEI Status Codes

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization

Status Code	Description
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

Status Code	Description
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
S3 Resume Error Codes	
0xE8	S3 Resume Failed in PEI
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

7.2.4. PEI Beep Codes

Number of Beeps	Description
1	Memory not Installed
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

7.2.5. DXE Status Codes

Status Code	Description
0x60	DXE Core is started

0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect

0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error

0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

7.2.6. DXE Beep Codes

Number of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Input or Output Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

7.2.7. ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

7.3. OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

Contact Information

North Andover, Mass. (Headquarters)

WIN Enterprises, Inc., 300 Willow Street, North Andover, Mass. 01845

+1 (978) 688-2000

sales@win-ent.com

+1 (978) 688-4884

www.win-ent.com