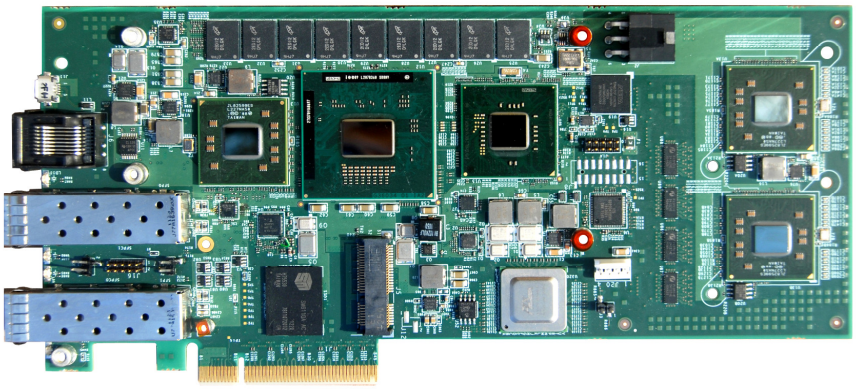


User's Manual

Version 1.0

Networking Preprocessing Board

Model Number IP-90830

(SoNIC) System on NIC with Intel® Dual Xeon® Preprocessor

e-Mail: sales@win-ent.com PH: (978) 688-2000

1.0 SoNIC Component Information*

CPU (Codename: Gladden)	SoNIC is initially offered in two varieties: • IP-9083A: Xeon E3-1125C, Quad-Core 2GHz, HT, 40W • IP-9083B: Core i3-2115C, Dual-Core, 2GHz, HT, 25W
RAM	The following dual-channel configurations, memory pre-installed, and non-removable on top/bottom sides: IP-9083A & IP-9083B: • 4GB (2x2GB) DDR3-1333 ECC, Registered
STORAGE	IP-9083A & IP-9083B: • 16GB (15.8 Avail) OnBoard (non removable) SATA SSD, 1x mSATA Slot
LAN (External or I/O Plate NICs)	IP-9083A & IP-9083B: • Dual 10GbE SFP+ i82599ES
USB & Serial	IP-9083A & IP-9083B: • 1x USB 2.0 micro connector on I/O plate • 1x RJ45 Serial Port on I/O plate • 2x USB 2.0 port on 2mm pitch 10-pin header
Additional Components	Both the IP-9083A & B Accelerators include two additional options to interface with a host system, see **5.0 Host System Communication** sections for more on these.

*WIN Enterprises can customize many features of the standard SoNIC offerings for your OEM needs. Some examples: Support for additional processors in the "Gladden" family, more or less memory support, larger or smaller, on-board SSD and more. Speak with a WIN representative for more information.

2.0 IP-90830 Component Layout

Figure 2A and **Figure 2B** show main component layout reference for IP-90830 SoNIC

Figure 2A IP-90830 "Top" (CPU Side)

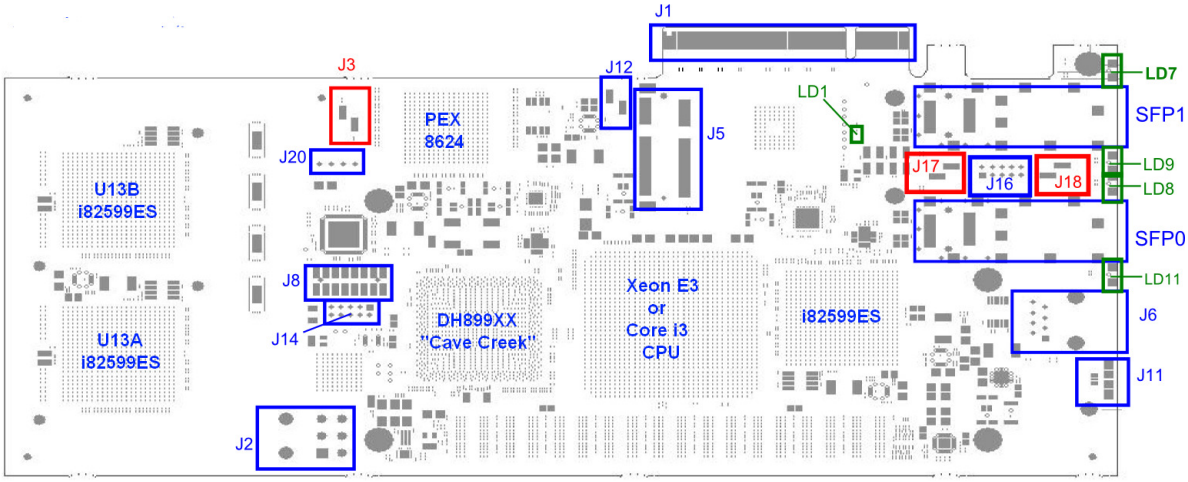
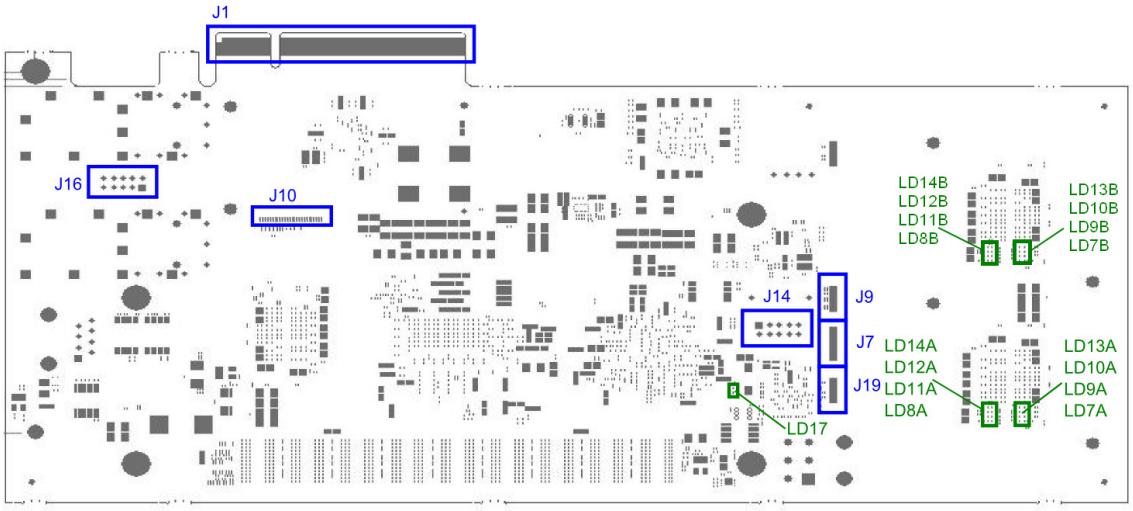


Figure 2B IP-90830 “Bottom”



2.1 Table: IP-9083A/B Pinout Definitions

J1	Standard PCIe x8 Gen 2.0 slot.
J2	12V Input Connector, use of this connector is required to boot SoNIC as it needs additional power than what is available through the PCIe pins. For this connector you can use industry standard 6-pin power adapters used for high-end video cards (“Dual LP4 to 6 Pin PCIe”), also found on many modern PSUs, with a 6-Pin plug usually labeled “PCIe”. One example of an off-the-shelf from StarTech LP4PCIEXADAP The board requires a PSU with ample power available on a +12V Rail **Power Requirements: +12VDC @8 Amps.** Adapter pinout: TOP ROW | PIN 4: GND | PIN 5: GND | PIN 6: GND BOTTOM ROW | PIN 1: +12VDC | PIN 2: +12VDC | PIN 3: +12VDC
J3	Host System Communication Configuration Jumper: Jumper ON: Slot (J1) <-> PEX8624 <-> CPU Jumper OFF (Default): PCIe Slot (J1) <-> i82559ES (U13B) <-> i82599ES (U13A) <-> CPU “Bump In the Wire” See **5.0 Host System Communication section** for more information.
J5	mSATA Connector: Standard mSATA (MiniCard-type) connector, for use only with mSATA modules. This connector is not for USB or PCIe devices.
J6	COM Port (Com 0 / ttyS0) Header (RS232, for Terminal Serial Redirection) **P1: RS232-CTS | P2: NoConnect | P3: RS232-TXD | P4: GND | P5: GND** **P6: RS232-RXD | P7: NoConnect | P8: RS232-RTS | P9: NoConnect | P10: NoConnect**
J7	GPIO Header for PCH CPLD Functions (DEBUG ONLY) (Rev AB Only) P1: VCC 3.3VDC | P2: CPLD_GPIO0_PCH_GP9 | P3: CPLD_GPIO1_PCH_GP10 | P4: CPLD_GPIO2_PCH_GP12

	P5: CPLD_GPIO3_PCH_GP13	P6: CPLD_GPIO4_PCH_GP14	P7: NoConnect	P8: GND	

J8 Header for LPC Access (DEBUG ONLY)

P1: VCC 3.3VDC	P2: LPC_LAD0
P3: LPC_LAD1	P4: LPC_LAD2
P5: LPC_LAD3	P6: LPC_LFRAME_#
P7: NoConnect	P8: VCC 5.0 VDC
P9: NoConnect	P10: NoConnect
P11: GND	P12: GND
P13: LPC_DRQ_#	P14: GND
P15: NoConnect	P16: GND

J9 JTAG Header for CPLD (DEBUG ONLY) (Rev AB Only)

P1: VCC 3.3VDC	P2: CPLD_TMS	P3: CPLD_TDO	P4: CPLD_TCK	P5: CPLD_TDI
P6: GND				

J10 XDP Debug Header

J11 MicroUSB Connector

P1: VCCUSB	P2: DATA-	P3: DATA+	P4: USB_ID	P5: GND
P6: EARTH	P7: EARTH	P8: EARTH	P9: EARTH	

J12 16GB OnBoard SSD Write Protect
Jumper ON: Write Protect ENABLE
Jumper OFF: Write Protect DISABLE

J14 USB 2.0 Header (2 Ports) 2MM Pitch

P1: VCCUSB	P3: DATA1-	P5: DATA1+	P7: GND	P9: NC
P2: VCCUSB	P4: DATA2-	P6: DATA2+	P8: NC	P10: GND

J16 SPI Header for BIOS

P1: VCC 3.3VDC_SPI	P3: SPI_CS_#	P5: SPI_FLH_MISO	P7: NC	P9: NC
P2: GND	P4: SPI_FLH_CLK	P6: SPI_FLH_MOSI	P8: SPI_ISOLATE_#	P10: GND

J17 & J18 BIOS chip boot select
J17: JUMPER ON (Selects boot from SPI1 BIOS)
J18: JUMPER ON (Selects boot from SPI0 BIOS)

J19 MAIN JTAG LOOP CONNECTOR

P1: VCC 3.3VDC	P2: NIA_TMS	P3: NIAB_TDO	P4: NIA_TCK	P5: CONN19_TDO
P6: GND				

J20 FAN Power (PWM Enabled)

P1: GND	P2: VCC +12VDC	P3: NC	P4: PWM

J21 PEX8624 Switch JTAG

P1: VCC 3.3VDC	P2: PEX_TMS	P3: PEX_TDI	P4: PEX_TCK	P5: U13B (82599ES)_TDO
P6: GND				

2.2 Table: IP-9083A/B LED Definitions

LD1	Read/Write Activity OnBoard SSD
LD7 & LD9	Link, Activity, Mode LEDs for SFP1
LD8 & LD11	Link, Activity, Mode LEDs for SFP0
LD7B, LD8B, LD9B, LD10B, LD11B, LD12B, LD13B, LD14B	Link, Activity, Mode LEDs for U13B (i82599ES)
LD7A, LD8A, LD9A, LD10A, LD11A, LD12A, LD13A, LD14A	Link, Acticity, Mode LEDs for U13A (i82599ES)

LD17	SATA_HD_LED

2.3 Table: Additional Pin Definition

SW3	The revision AB boards have a 0.100" bridge pin-pair that needs to be shorted briefly (i.e. momentary switch) to turn on. Once on, SoNIC will remain on until powered off.

3.0 Installation and Bootup of the IP-90830 SoNIC

3.1 Power off all power to host board, including standby.

3.2 Install the IP-90830 in an available PCIe x8 (or x16) slot.

3.3 Plug 6-pin "PCIe AUX" power connector into J1 (top row GND, bottom row +12VDC, see Table 2.1, J1)
NOTE: Take great care when removing this 6-pin connector as the small "0201" resistors behind U13A can be scraped or damaged when removing this connector.

3.4 For communication to SoNIC, you can now plug in a Console Redirection Cable (RJ45 end) to J11, and/or communicate via external network (SFP0, or SFP1) via "SSH", finally you can simply use the "Bump in the Wire" method (see **5.0 Host System Communication**) via SSH. The pre-installed Fedora 16 x86_64 OS is a multi-user OS that can connect simultaneously via all 3 input methods. Finally, there is an advanced communication method possible via direct access from PCIe slot to the CPU requiring additional programming support to enable, which at the time of this writing, and AB revision, is not functional.

3.5 Power on Host Board (to power SoNIC outside of a Host Board, see **Working with SoNIC from the Bench**)

3.6 Access SoNIC via SSH or Terminal (see **4.0 Accessing SoNIC**) It will boot by default automatically to the pre-installed Fedora 16 x86_64 image on the IP-90830 (Designated SILICONIMAGE 15.8) device in BIOS. The login credentials for SoNIC are:

Login: **intel** (all lowercase, this is NOT part of the admininstrator group, for this login as: **root**)

Password: **password** (all lowercase, this is also the password for **root** & **sudo**

4.0 Accessing SoNIC

4.1 SoNIC can be accessed via console redirection (J11) with the following settings:
Speed: 115200
Data: 8
Parity: n (or null)
Stop: 1
(for example, in Linux, you might use the "screen" command for your terminal program:

screen /dev/ttyS(com port) 115200

(Since **8, null, 1** are common settings you may not have to specify these)

4.2 SoNIC can be accessed via SSH as well, via either the external IP (from SFP0 or 1) or from the internal IP (from U13A + U13B interconnect). The login credentials are the same, but this requires you to know the IP address of the SoNIC board.
The U13A is set to ip: 10.10.1.1 and 10.10.2.1

From the host system, you'll want to set your brand new 10GbE 82599 interface (U13B) to 10.10.1.2 and 10.10.2.2 or something similarly appropriate. After this, with SSH software you can:

ssh root@10.10.1.1 or
ssh root@10.10.2.1
Into the SoNIC board via the U13A XAUI if.
NOTE: If you'd like to increase performance, you can "bond" these devices on both ends as well.
If neither works, there may be a problem with the XAUI (U13A or B) interface. If so, you can ssh through whatever the SFP+ ports leased from your router:
(e.g.: # ssh root@192.168.1.111)

Then login with the same password credentials described above.

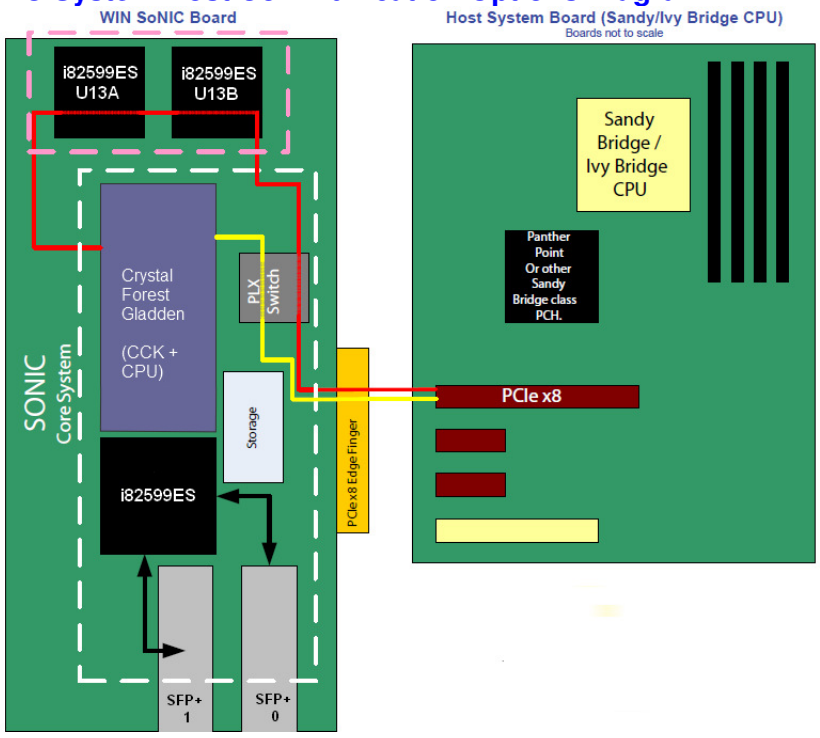
4.3 To access the SoNIC BIOS, you will either have to boot the board independent of an System Host Board power source (See **6.0 Working With SoNIC from the Bench**) or simply issue a "reboot" command to the onboard image.
In either event the BIOS is an only visible/available to manipulate via console redirection methods.
As the system posts, press the F2 key when the POST screen appears, this command, and the internal BIOS options should be similar and familiar to any standard commercial motherboard with an AMI EFI BIOS. BIOS Commands are explained later in this document. (See **7.0 SoNIC BIOS**)

5.0 System Host Communication

5.1 Communication with the system host board can be achieved in two ways:

1.) The IP-90830, by default, is preconfigured a straightforward and simple implementation nicknamed "bump in the wire". This configuration uses two additional Intel® 8299ES 10 Gigabit Ethernet Controllers which provides for fast and easy implementation by most OEMs. In this configuration (see red line in **Figure 5A**), SoNIC presents to the host systems' OS as a Dual 10GbE network card connecting through the PLX bridge to U13B. Simultaneously, SoNIC, boots via its own storage device, into its own OS and detects U13A. U13A & B connect together via XAUI interface and present Sonic to the host system as a **networked system**. The PLX PCIe bridge is operating in **transparent** mode, and the yellow path (see figure below) is *not* active. This configuration provides an off-the-shelf, and well-known standard solution to communicate back and forth with SoNIC with currently available i82599 drivers that support virtualization in a variety of Operating Systems.

Figure 5A SoNIC System Host Communication Options Diagram.



(Drawings not to scale)

2.) In the secondary configuration, the PLX PCIe switch is operating in **non-transparent** mode, and the yellow line is followed, while the red line is not functional. Special device code can be written to communicate directly to SoNIC (removing U13A & B) over the now non-transparent PLX switch. The PLX 8624 PCIe switch was chosen for its non-transparent capability allowing clients with sufficient development resources to customize their own programming methods for use with SoNIC in their own operating system of choice, and communicate directly with the Xeon Gladden PCIe interface.

6.0 Working with SoNIC from the Bench

Sonic can be POSTED and Operated independent of a system main board. Simply build a stable and ESD-safe environment with which to rest the IP-90830, and supply a suitable 12V power source (12VDC @ 8 Amps) into J2 6-pin PCIe Aux power adapter.
NOTE: Take great care when removing this 6-pin connector as the small "0201" resistors behind U13A can be scraped or damaged when removing this connector
Apply power, and short SW3 briefly and SoNIC will power up as normal. The interaction with SoNIC from this point will be limited to Console Redirection (J11) or SSH (SFP1 / SFP0).

7.0 SoNIC BIOS

7.1 Accessing the BIOS:

SoNIC is preconfigured to display a large dump of preboot information before you can access BIOS.

If this is your first time using SoNIC as an evaluation product, entering the BIOS should not be necessary except for experimentation or troubleshooting. SoNIC is preconfigured to automatically boot to the on-board SATA SSD chip and enter its' own OS. Some of these fields may no longer be valid, or be slightly different from when this was written as it is based off of a similar design with the same BIOS.

Press F2 when the following screen appears.

```
|Version 2.11.1210. Copyright (C) 2010 American Megatrends, Inc.       |
|BIOS Date: 9/8/2011 11:22:14 Ver: 0ABXQ626                           |
|EVALUATION COPY.                                                     |
|Press <DEL> or <F2> to enter setup.                                  |
```

7.2 BIOS Main Screen

```
Aptio Setup Utility – Copyright (C) 2011 American Megatrends, Inc.
    Main  Advanced  Chipset  Boot  Security  Save & Exit
/-----------------------------------------------------+-------------------------\
|  BIOS Information                                   |Choose the system        |
|  BIOS Vendor             American Megatrends        |default language         |
|  Core Version            4.6.4.1                    |                         |
|  Compliancy              UEFI 2.1                   |                         |
|  Project Version         0ABXQ 6.26 x64             |                         |
|  Build Date and Time     9/8/2011 11:22:14          |                         |
|                                                     |                         |
|  Memory Information                                 |                         |
|  Total Memory            4096 MB (DDR3 1333)        |                         |
|                                                     |-------------------------|
|  System Language         [English]                  |><: Select Screen        |
|                                                     |^v: Select Item          |
|  System Date             [Sat 01/01/2011]           |Enter: Select            |
|  System Time             [00:00:16]                 |+/-: Change Opt.         |
|                                                     |F1: General Help         |
|  Access Level            Administrator              |F2: Previous Values      |
|                                                     |F3: Optimized Defaults   |
|                                                     |F4: Save & Exit          |
|                                                     |ESC: Exit                |
\-----------------------------------------------------+-------------------------/
```

The first screen you will see when entering SoNIC BIOS the main screen which contains basic information about the BIOS code, date & vendor.

IP-9083A & B units will contain 4GB of DDR3 PC-1333 RAM, which can be verified here.

Finally, in the upper-right-hand corner of your display, you'll see help prompts which will display information about the various fields that you are highlighting.

Note: Because the IP-90830 contains no battery backup for Real Time Clocks, setting the Date & Time is not necessary as power-cycling the board will erase Date & Time data.

7.2 Advanced BIOS Options

Under the Advanced tab, are several options with HELP

```
    Main  Advanced  Chipset  Boot  Security  Save & Exit
/-----------------------------------------------------+-------------------------\
|                                                     |Enable or Disable Boot   |
|  Legacy OpROM Support                               |Option for Legacy        |
|  Launch PXE OpROM        [Disabled]                 |Network Devices.         |
|  Launch Storage OpROM    [Enabled]                  |                         |
|                                                     |                         |
|> PCI Subsystem Settings                             |                         |
|> ACPI Settings                                      |                         |
|> CPU Configuration                                  |                         |
|> SATA Configuration                                 |                         |
|> USB Configuration                                  |-------------------------|
|> Cave Creek SIW Configuration                       |><: Select Screen        |
|> Clock Generator                                    |^v: Select Item          |
```

```
|> Serial Port Console Redirection                    |Enter: Select            |
|                                                      |+/-: Change Opt.         |
|                                                      |F1: General Help         |
|                                                      |F2: Previous Values      |
|                                                      |F3: Optimized Defaults   |
|                                                      |F4: Save & Exit          |
|                                                      |ESC: Exit                |
\------------------------------------------------------+-------------------------/
```

- `Legacy OpROM` and its subheadings can be ignored in revision AB as they have no function. There is currently no PXE ROM Support, Also, there are no storage OpROMs to be concerned with.

- `PCI Subsystem Settings` displays information regarding devices connected via legacy PCI bus which are remains of the core BIOS code and should be ignored.

- `PCI Express Settings` and `PCI Express GEN 2` settings contain features that are preset for the default board configuration. It is not recommended to change these settings unless you are advised to by the manufacturer.

- `ACPI Settings` subsection should not be modified from its default settings, to allow IP-90830 to function normally.

- `CPU Configuration` and its subdirectory contain hardware information about your installed CPU. You can use this heading to verify the CPU type on the IP-90830 version you purchased.

    - `Hyper-Threading, Active Processor Core, Execute Disable Bit, Intel Virtualization`, and `Power Technology` are preconfigured for maximum performance & power efficiency. If you are installing your own custom OS distribution for SoNIC, these options may not be supported and can be disabled either here at the BIOS level, or with kernel arguments on your bootloader. They are all set to `Enabled/ALL` by default.

- `SATA Configuration` contains only one useful field of note:
    - `SATA Mode`, which is by default set to `AHCI`, which is recommended for the current version of the DH89XX (Cave Creek) sample code, it is not recommended to change to `IDE` mode, however depending on your custom OS requirements, this may need to be changed.
      The `Staggered Spin-Up` and `Hot-Plug` settings are not relevant to this configuration and can be ignored.
      Note: The mSATA port does not support hot-plug.

- `USB Configuration` should be left unchanged, as it is preconfigured for success with for modern operating systems (e.g. Linux 2.6+), however depending on the specifics of your custom kernel, the EHCI and Legacy Handoff functions may provide an easier effort of reading your USB devices. Some devices (e.g. a specific brand of Transcend USB key) can cause the system to hang. In some cases modifying the `Power Up Delay` can help fix this. The `Mass Storage Device` field gives you the opportunity to power up your USB storage to appear as a different type of device (CD, Floppy, etc) though `AUTO` setting is recommended and most extensively tested.
- `Cave Creek SIW Configuration` is where you will find your COM Port settings to control the Console Redirection Interface (see also **4.0 Accessing SoNIC**) settings. The IP-90830, and its OS are preconfigured to the following settings:

    - `Serial Port 0 Configuration`
        - `Enabled, IO=38fh, IRQ=4`

  The COM Port speed & Redirection variables are changed in a different location: `Serial Port Console Redirection`

  NOTE: Serial Port 0 (known as ttyS0 to most Linux OS's, and COM1 to others)

  NOTE: Serial Port 1 is not connected and these fields can be ignored.

- `Clock Generator` the field under this directory can enable or disable Spread Spectrum clocking. **Note: On IP-90830 revision AB, this should be left DISABLED, as it will cause the IP-90830 to not function, later revisions (BA and on) will fix this issue.**
- `Serial Port Console Redirection` this section controls the speed and protocols of Serial Port 0 (ttyS0 / COM1).
    - `COM 0 > Serial Port Console Redirection` is defaulted to `ENABLED` and should be left at this setting.
    - `COM 0 > Console Redirection Settings` is defaulted to the following:
        - `Terminal Type [VT-UTF8]`
        - `Bits Per Second [115200]`
        - `Data Bits [8]`
        - `Parity [None]`
        - `Stop Bits [1]`
        - `Flow Control [None]`
        - `Recorder Mode [Disabled]`
        - `Resolution 100x31 [Disabled]`
        - `Legacy OS Redirection [80x24]`

      These settings are set for maximum compatibility with the preconfigured operating system on the IP-90830. Terminal Type can be safely changed to whatever output (VT100 or VT102 are common choices) display better in your terminal redirection software, however `VT-UTF8` is usually a compatible standard with both.
      The `Bits per Second` and additional field changes will cause an incompatibility with the on-board OS (`/boot/grub2/grub.cfg`) and the correlated changes should be made before changing these by another method (for example: SSH). `Recorder` and `Resolution` modes have not been tested.

      NOTE: The fields for `COM1` and `Serial Port for Out Of Band Management` should be left `Disabled` as they have no function on the IP-90830 and are remnants of the core BIOS code.

7.3 Chipset Options.

Under chipset are two fields, one for `North Bridge` (the CPU), the other for `South Bridge` (the DH89 Cave Creek chipset).

7.3A `North Bridge`:

```
/-------------------------------------------------+-------------------------\
|  Memory Information                             ^|Low MMIO resources       |
|                                                 *|align at 64MB/1024MB     |
|  Total Memory            4096 MB (DDR3 1333)    *|                         |
|                                                 *|                         |
|  Memory Slot0            2048 MB (DDR3 1333)    *|                         |
|  Memory Slot1               0 MB (DDR3 1333)    *|                         |
|  Memory Slot2            2048 MB (DDR3 1333)    *|                         |
|  Memory Slot3               0 MB (DDR3 1333)    *|                         |
|                                                 *|                         |
|  Low MMIO Align          [64M]                  *|-------------------------|
|                                                 *|><: Select Screen        |
|  VT-d                    [Disabled]             +|^v: Select Item          |
```

```
|  Memory ECC Support      [Enabled]                +|Enter: Select             |
|  Root Port 1             [Enabled]                +|+/-: Change Opt.          |
|  Root Port 2             [Enabled]                +|F1: General Help          |
|                                                   +|F2: Previous Values       |
|  Initate Graphic Adapt   [PEG/IGD]                +|F3: Optimized Defaults    |
|  IGD Memory              [64M]                    +|F4: Save & Exit           |
|  Render Standby          [Enabled]                v|ESC: Exit                 |
\--------------------------------------------------+-------------------------/
```

Page down

```
|  Memory Slot3               0 MB (DDR3 1333)      *|                          |
|                                                   *|                          |
|  Low MMIO Align          [64M]                    *|-------------------------|
|                                                   *|><: Select Screen         |
|  VT-d                    [Disabled]               +|^v: Select Item           |
|  Memory ECC Support      [Enabled]                +|Enter: Select             |
|  Root Port 1             [Enabled]                +|+/-: Change Opt.          |
|  Root Port 2             [Enabled]                +|F1: General Help          |
|                                                   +|F2: Previous Values       |
|  Imitate Graphic Adapt   [PEG/IGD]                +|F3: Optimized Defaults    |
|  IGD Memory              [64M]                    +|F4: Save & Exit           |
|  Render Standby          [Enabled]                v|ESC: Exit                 |
|  IGD Multi-Monitor       [Disabled]               +|                          |
|                                                   +|                          |
|  PCI Express Port        [Auto]                   +|                          |
|  PEG Force Gen1          [Disabled]               +|                          |
|  Detect Non-Compliance   [Disabled]               +|                          |
|  MRC Message Print       [Disabled]               +|                          |
\--------------------------------------------------------------------------------/
```

This page will show useful information about the exact memory alignment of the on-board memory. Standard IP-9083A and B systems will have the same memory configuration pictured, 2 Offset (Slot 0 & 2) arrays of 2048MB DDR3 PC1333 memory in a Dual-Channel Alignment.

- `Low MMIO Align [1024M]` This field should be set to 1024M for 64-bit OS, and 64M for 32-bit OS.
- `VT-d [Disabled]` This field should be set to `Enable` or `Disable` depending on your use of virtualization. In GRUB, you can set the following kernel argument: iommu=off to disable virtualization support at the kernel. **NOTE: The VT-d function has <u>not</u> been tested and will crash the Fedora 16 image pre-installed, do note enable it. It may function with a fresh OS install with this flag enabled.**
- `Memory ECC Support [Enabled]` This field enables or disables the ECC function of the on-board ECC Registered DDR3 PC3-1333 Ram chips.
- Leave both PCIe `Root Ports 1( and 2) [Enabled]`
- Leave the following settings at their Default as they have either no effect (with regard to graphics, or expansion slot compatibility.)

  ```
  IGD Memory              [64M]
  Render Standby          [Enabled]
  IGD Multi-Monitor       [Disabled]
  PCI Express Port        [Auto]
  PEG Force Gen1          [Disabled]
  Detect Non-Compliance   [Disabled]
  ```

- `MRC Message Print [Disabled]` This field can be used to display Memory MRC information (Memory Reference Code) visible during console redirection.

7.3B `South Bridge`

```
/--------------------------------------------------+-------------------------\
|                                                  |Enable or disable SMBus  |
|  SB Chipset Configuration                        |Controller.              |
|  SMBus Controller        [Enable]                |                         |
|                                                  |                         |
|  Restore AC Power Loss   [Always ON]             |                         |
|  SLP_S4 Assertion Stre   [Enable]                |                         |
```

```
|   SLP_S4 Assertion Wid   [4-5 Seconds]              |                          |
|                                                     |                          |
|  High Precision Event Timer Configuration           |                          |
|  High Precision Timer    [Enabled]                  |--------------------------|
|                                                     |><: Select Screen         |
|> PCI Express Ports Configuration                    |^v: Select Item           |
|> USB Configuration                                  |Enter: Select             |
|                                                     |+/-: Change Opt.          |
|                                                     |F1: General Help          |
|                                                     |F2: Previous Values       |
|                                                     |F3: Optimized Defaults    |
|                                                     |F4: Save & Exit           |
|                                                     |ESC: Exit                 |
\-----------------------------------------------------+--------------------------/
```

This page shows information about configurable aspects of the DH89XX Cave Creek PCH. All items here, as well as in the PCI Express Ports Configuration submenu, and USB Configuration submenu, should be left at their defaults. Changing them can cause unpredictable results and are generally used to debug compatibility issues with peripheral add-on cards for standard motherboards. These features are installed by default with the BIOS code and should be ignored.

- `SMBus Controller [Enable]` Leave enabled unless your kernel has specific issues with reading the SMBus that you cannot work around.

- `Restore AC Power Loss [Always ON]` This will automatically startup the IP-90830 when power is applied to the host system. The default configuration is the only power mode the IP-90830 is configured for.
  NOTE: We recommend you do NOT issue a shutdown command to the SoNIC OS until you are ready to shut down the entire system, this is due to the fact that you will need to power-cycle your entire system in order to power the IP-90830 back on. If you need to perform SoNIC OS maintenance, it is recommended you use the reboot command instead.

7.4 Boot Menu

```
                                                    Boot
/-----------------------------------------------------+--------------------------\
|  Boot Configuration                                 |Number of seconds to      |
|  Setup Prompt Timeout    3                          |wait for setup            |
|  Bootup NumLock State    [On]                       |activation key.           |
|                                                     |65535(0xFFFF) means       |
|  Quiet Boot              [Disabled]                 |indefinite waiting.       |
|                                                     |                          |
|  CSM16 Module Version    07.64                      |                          |
|                                                     |                          |
|  GateA20 Active          [Upon Request]             |                          |
|  Option ROM Messages     [Force BIOS]               |--------------------------|
|  Interrupt 19 Capture    [Disabled]                 |><: Select Screen         |
|                                                     |^v: Select Item           |
|  Boot Option Priorities                             |Enter: Select             |
|  Boot Option #1          [P4: SILICONMOTION ...]    |+/-: Change Opt.          |
|  Boot Option #2          [UEFI: Built-in EFI...]    |F1: General Help          |
|  Boot Option #3          [UEFI: USB USB Hard...]    |F2: Previous Values       |
|                                                     |F3: Optimized Defaults    |
|  Hard Drive BBS Priorities                          |F4: Save & Exit           |
|                                                     |ESC: Exit                 |
\-----------------------------------------------------+--------------------------/
```

- `Setup Prompt Timeout 3` This setting changes the wait time for the setup key (F2) to be pressed before the unit continues on to boot from `Boot Option #1`
- `Bootup NumLock State [On]` This setting changes whether or not the NUMLOCK Key will be activated at boot.
- `Quiet Boot [Disabled]` Enable to remove display of some preboot information, has no effect on boot-time.

- `GateA20 Active [Upon Request]` Leave as default, unless you are running RealTime code above 1MB.
- `Option Rom Messages [Force BIOS]`, `Interrupt 19 Capture [Disabled]` have no necessary application on the IP-90830.
- `Boot Option Priorities` has important subheadings where you can select up to 3 Devices to boot from. The platform will try to boot from each device listed, in order, until it can successfully boot. If no devices are bootable, the IP-90830 will boot to a prompt which reads: No Boot Devices Available.
  Note: this boot failure message will only be available to be seen from Console Redirection method, as SSH will only work from a valid OS.
- `Boot Option #1 (or #2, or #3) [P4: SILICONMOTION ...]` default setting to boot from the onboard SSD NAND Flash module, it will be listed as `[P4: SILICONMOTION…]` and is preset to boot first.
  To change the boot order, you can either highlight an option and press the + or – keys, or press ENTER and change the option with the arrow keys.
- `Hard Drive BBS Priorities` Entering this submenu will allow you to change the priority of devices listed as "Hard Drives." Such devices are usually:
  - Specially formatted USB Keys, which are formatted in Hard Drive partitions (NTFS, or some Linux partitions)
  - mSATA devices installed at J5 (mSATA socket)
  - USB Hard Drives plugged in externally

  The limitation of this BIOS is that you can only have one Hard Drive listed in any of the 3 boot options listed in `Boot Option Priorities` at one time, boot devices must be floppy disks, USB Keys (not formatted as HDDs), or USB Optical Devices for example.

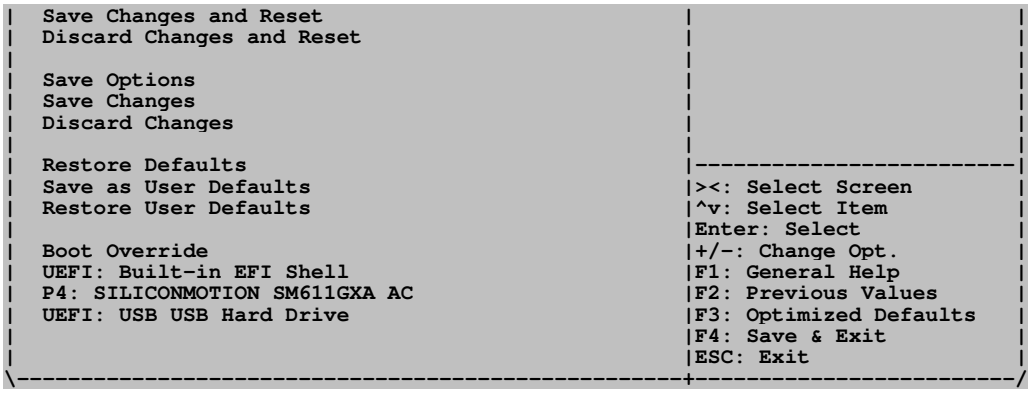
7.5 Security

```
                                                    Security
/-------------------------------------------------+-------------------------\
|  Password Description                           |Set Administrator        |
|                                                 |Password                 |
|  If ONLY the Administrator's password is set,   |                         |
|  then this only limits access to Setup and is   |                         |
|  only asked for when entering Setup.            |                         |
|  If ONLY the User's password is set, then this  |                         |
|  is a power on password and must be entered to  |                         |
|  boot or enter Setup. In Setup the User will    |                         |
|  have Administrator rights.                     |                         |
|  The password must be 3 to 20 characters long.  |-------------------------|
|                                                 |><: Select Screen        |
|                                                 |^v: Select Item          |
|  Administrator Password                         |Enter: Select            |
|  User Password                                  |+/-: Change Opt.         |
|                                                 |F1: General Help         |
|                                                 |F2: Previous Values      |
|                                                 |F3: Optimized Defaults   |
|                                                 |F4: Save & Exit          |
|                                                 |ESC: Exit                |
\-------------------------------------------------+-------------------------/
```

This screen allows you to set passwords to continue booting, or entering setup to the IP-90830 BIOS, this is only recommended for use if you access the IP-90830 via Console Redirection as you will not see this BIOS screen otherwise.

7.6 Save & Exit

```
                                          Save & Exit
/-------------------------------------------------+-------------------------\
|  Save Changes and Exit                          |Exit system setup after  |
|  Discard Changes and Exit                       |saving the changes.      |
```



Save & Exit menu is mostly self-explanatory. You can also choose to save your currently set settings as “new” defaults though this is only recommended if you have a clean BIOS backup on the second SPI BIOS chip.

NOTE: IP-90830 revision AB has only one functional SPI BIOS chip, saving custom settings as defaults are not recommended unless you are equipped to manually program the BIOS via SPI header J16.

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