Custom x86 Embedded Solutions

PL-80930

Networking Appliance

User's Manual

Version 1.0

1U Rack-Mount Intel® Haswell-EP Xeon E5-2600V3 Series Processor and Intel® C612 PCH Network System, support DDR4 up to 256GB, 4 PCIe x8 slot for expansion NIC module, 2 x 2.5" or 1 x 2.5" & 1 x 3.5" SATA HDD, 2 USB, 2 GbE, 1 Console, CF, SATA DOM, 1 PCIe x8 slot, Redundant PSU

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Revision History			
Date	Version	Modification	Editor
2015/12/24	1.0	First Release	Jason Fan

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Chapter 1. General Information

1.1 Introduction

The PL-80930 is 1U Rack-Mount high-performance networking system that fulfills most networking solutions. It uses the New Intel® Microarchitecture Haswell EP platform with efficient performance processor Xeon E5-2600 V3 family and the Intel® C612 series chipset (codenamed Wellsburg). This new generation platform provides high performance, CPU cores of up to 18 cores, and supports 45MB of cache and a total of 40 PCIe lanes.

The PL-80930 is an enhancement in computing performance, system responsiveness with Intel® E5-2600 V3 processor, supporting eight DDR4 ECC RDIMM/ LRDIMM(up to 2133 MHz) and maximum memory capacity of up to 256 GB. With 40 PCIe Express lanes, the PL-80930 can support up to 8 NIC modules, and support multiple Ethernet module bays for flexible port configuration; such as 10 Gigabit SFP+, Gigabit copper with BYPASS function (or not) and Gigabit fiber ports. Maximum capable Ethernet ports is 64 GbE.

The strong IO elements of PL-80930 include two management Ethernet ports (one for management, another for optional IPM function), a console port, two USB ports, a LCD module with keypad (5 keys), LEDs for power/ HDD/ 2x GPO. In addition, the PL-80930 also supports two 2.5" SATA or one 2.5" and one 3.5" HDDs/SSDs and onboard CompactFlash™ and SATA DOM for basic network storage applications.

1.2 Specifications

Processor System	CPU	Supports Single Intel® Haswell-EP E5-2600V3 Series, LGA 2011-3
	Chipset	Intel® Wellsburg C612 PCH
	BIOS	AMI® UEFI BIOS
Memory	Technology	Total 8 DIMMs (Four channels per CPU, 2 DIMMs per channel) 1. ECC/ Registered DDR4 2133 MHz memory, up to 32GB per DIMM 2. LRDIMM: DDR4 2133 MHz, up to 32GB per

		DIMM	
	Capacity	ECC UDIMM/ RDIMM: up to 256GB LRDIMM: up to 256GB	
Expansion	Expansion Slots	1. One SO-DIMM slot for IPMI card with VGA support 2. One Gen. 3 PCIe x4 in PCIe x8 slot	
Ethernet	Ethernet Modules for Option	IP-384A	Expansion module with 8 SFP GbE ports, Intel 82580EB
		IP-384B	Expansion module with 8 SFP GbE ports, Intel I350-AM4
		IP-385A	Expansion module with 8 RJ45 GbE ports with two pairs Gen. 3 bypass, Intel 82580E
		IP-385B	Expansion module with 8 RJ45 GbE ports with two pairs Gen. 3 bypass, Intel I350-AM4
		IP-386A	Expansion module with 4 SFP+ 10 GbE ports, Intel XL710-BM1 w/o re-driver
		IP-387A	Expansion module with 2 QSFP+ 40 GbE ports, Intel XL710-BM2 w/o re-driver
		IP-405A	Expansion module with 4 SFP GbE ports, Intel i350-AM4
		IP-406A	Expansion module with 4 RJ45 GbE ports with two pairs Gen. 3 bypass, Intel i350-A
		IP-408A	Expansion module with 4 RJ45 10G ports, Intel X540-BT2
		IP-408B	Expansion module with 2 RJ45 10G ports, Intel X540-BT2
Hardware Acceleration Module	Cryptographic	NA	
Storage	SATA HDD	Supports two 2.5" SATA HDD or Supports one 2.5" & one 3.5" SATA HDD	

	Compact Flash™ Socket	One CompactFlash™ Type I/II One SATA DOM
Front Accessible I/O	USB Port	Two external USB 2.0
	Console Port	One RJ45 Console port (COM1)
	Management Port	One MGMT port in RJ45, Intel® i210 One IPMI port support (option) in RJ45, Intel i210
	Display Port	One VGA pin header (R303D need plug in main board)
Power Supply	Watts	1U 500W ATX redundant power supply
Mechanical and Environmental	Form Factor	1U rack-mount
	LCD Module	One 16x2 LCM
	Keypad	R383A with five key buttons
	LED	4x GPO LEDs via R380A GP57 (Yellow) GP54 (Yellow) GP55 (Red) GP56 (Green)
	Dimensions (W x D x H)	440mm (W) x 570mm (D) x 44mm (H) (17.2"W x 22.44"D x 1.73"H)
	Operating Temperature	Operating: 0 ~ 40°C (32 ~ 104°F)
	Storage Temperature	-20 ~ 75°C (-4 ~ 167°F)
	Humidity	10 ~ 85% relative humidity, non-operating, non-condensing
Weight	1pc/CTN, 12 kgs	
Certification	CE/FCC	

1.3 Ordering Information

PL-80930	1U Rack-Mount, Single Intel Haswell-EP Processor with C612 PCH, DDR4, 4 PCIe x8 slots for Expansion Module , Console, USB, 2GbE, SATA, CF, SATA DOM, 1 PCIe x8
IP-303D	IPMI Card with VGA support for PL-80930
IP-384A	Expansion module with 8 SFP GbE ports, Intel 82580EB
IP-384B	Expansion module with 8 SFP GbE ports, Intel I350

IP-385A	Expansion module with 8 RJ45 GbE ports with two pairs Gen. 3 bypass, Intel 82580EB
IP-385B	Expansion module with 8 RJ45 GbE ports with two pairs Gen. 3 bypass, Intel I350-AM4
IP-386A	Expansion module with 4 SFP+ 10 GbE ports, Intel XL710-BM1 w/o re-driver
IP-387A	Expansion module with 2 QSFP+ 40 GbE ports, Intel XL710-BM2 w/o re-driver
IP-405A	Expansion module with 4 SFP GbE ports, Intel i350-AM4
IP-406A	Expansion module with 4 RJ45 GbE ports with two pairs Gen. 3 bypass, Intel i350-AM4
IP-408A	Expansion module with 4 RJ45 10G ports, Intel X540-BT2
IP-408B	Expansion module with 2 RJ45 10G ports, Intel X540-BT2
DK002	Cable development kit: CB-CO5204-00 Cross over 2M CB-DB9200-01 Null modem cable 2M CB-EC5200-00 Ethernet cat. 5 cable 2M CB-IPS200-00 KBMS cable, 15CM CB-IUSB2B-00 USB cable, 25CM CB-IVGA01-00 VGA cable, 20CM CB-RJDB91-00 RJ-45 to DB-9 cable 2M

1.4 Packaging

Please make sure that the following items have been included in the package before installation.

1. PL-80930 Appliance
2. Cables (Optional)
3. CD-ROM that contains the following folders:
   - 4.1 Manual
   - 4.2 System Driver
   - 4.3 Ethernet Driver
   - 4.4 Utility Tools

If any item above is missing or damaged, please contact your dealer or retailer from whom you purchased the PL-80930. Keep the box and carton when you

will probably ship or store PL-80930 in near future. After you unpack the goods, inspect and make sure the packaging is intact. Do not plug the power adapter to the appliance if you find it appears damaged.

Note: Keep the PL-80930 in the original packaging until you start installation.

1.5 Precautions

Please make sure you properly ground yourself before handling the PL-80930 appliance or other system components. Electrostatic discharge can be easily damage the appliance .

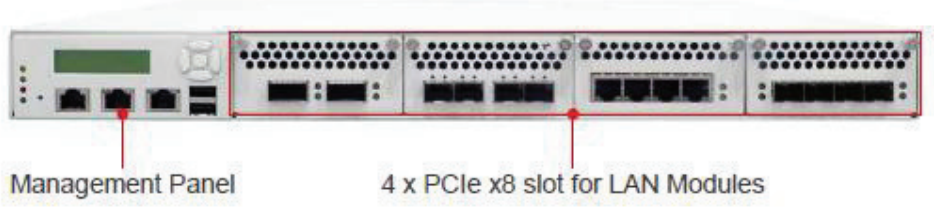
Do not remove the anti-static packing until you are ready to install the PL-80930 appliance.

Ground yourself before removing any system component from its protective anti-static packaging. To ground yourself, grasp the expansion slot covers or other unpainted parts of the computer chassis.

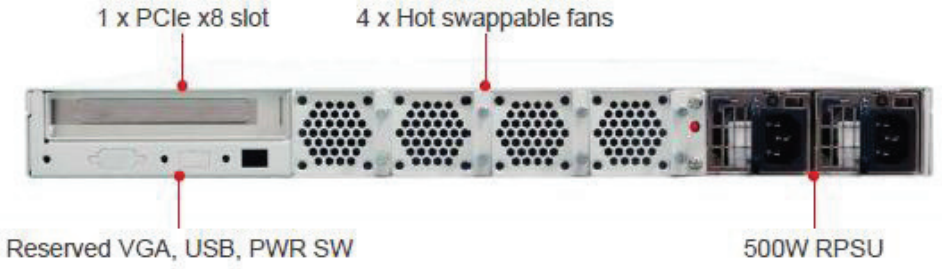
Handle the PL-80930 appliance by its edges and avoid touching the components.

1.6 System Layout

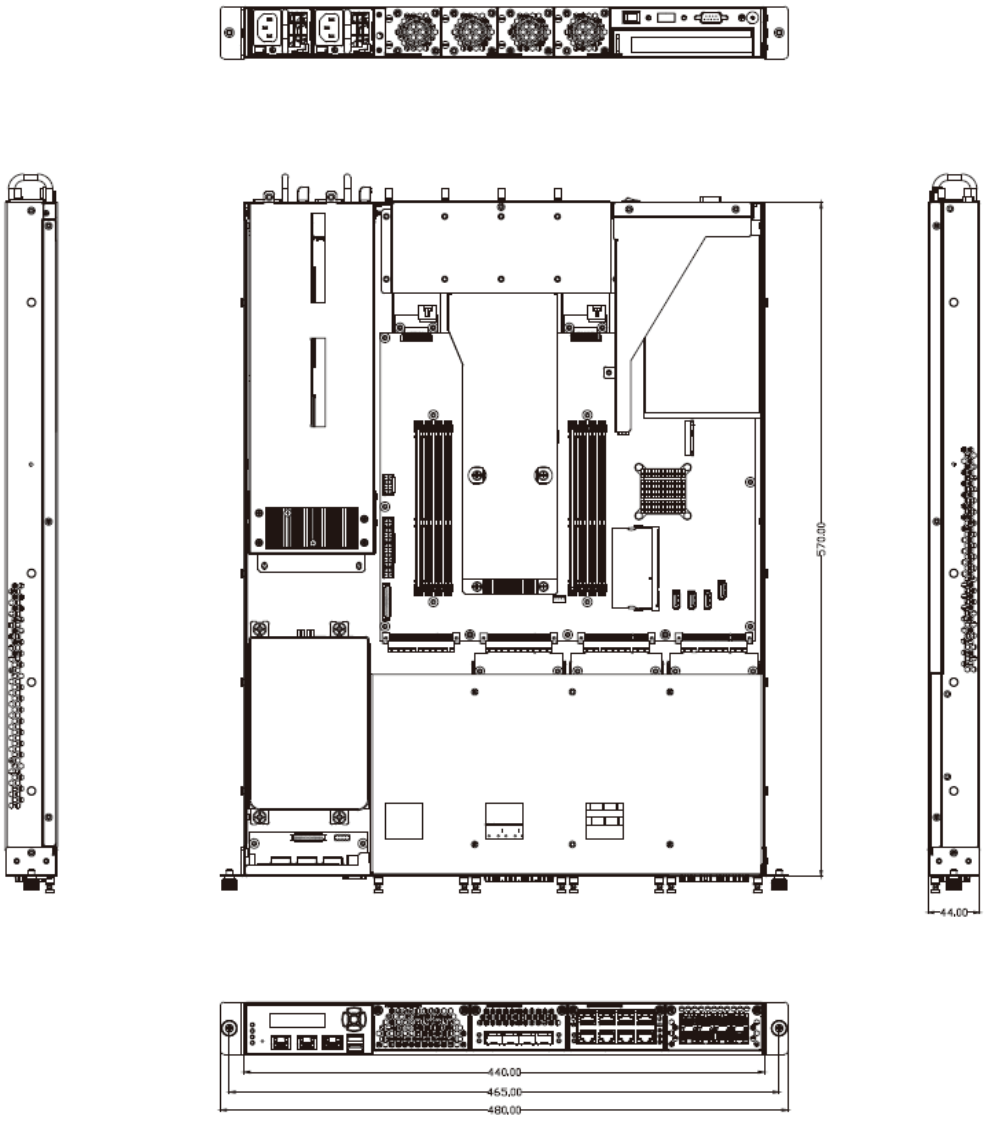
< Front panel features >



< Rear panel features >

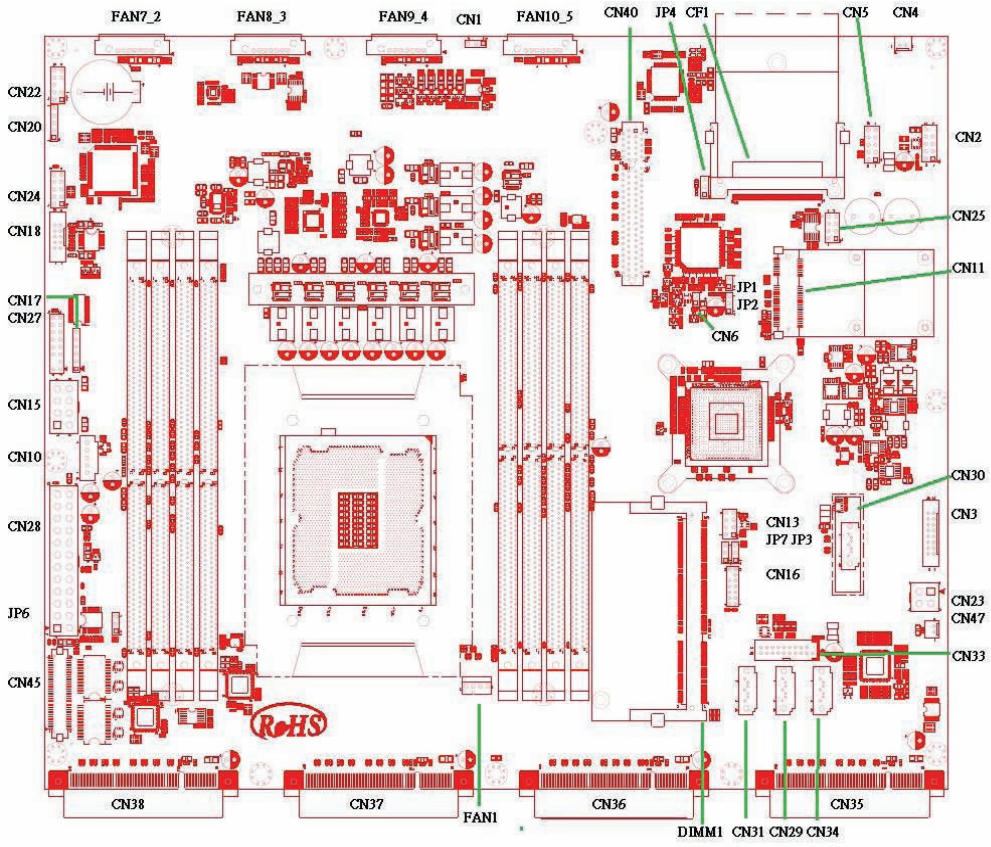


1.7 Dimensions



Chapter 2. Connector/Jumper Configuration

CB - 1911 A Rev.A1 Connector Pin Define and Jumper Setting



Connector List	
Connector	Define
CN1	VR12_I2C PIN HEADER
CN2	USB PIN HEADER
CN3	VGA BOX HEADER
CN4	ATX_SWITCH
CN5	CPLD JTAG
CN6	DEBUG GPIO
CN7	ATX I2C Connector
CN8	MINI-PCIE
CN9	FRONT PANEL PIN HEADER
CN10	ATX_8PIN

CN11	LPC PIN HEADER
CN12	KEY PAD PIN HEADER
CN13	COM2 BOX HEADER
CN14	GPI PIN HEADER
CN15	PS2 MS/KB PIN HEADER
CN16	PCIE +12V_ATX4PIN(RESERVED)
CN17	GPO PIN HEADER
CN18	SPI PIN HEADER
CN19	KEY PAD PIN HEADER
CN20	ATX 24PIN
CN21	SATA3# 2
CN22	SATA3# 1
CN23	SATA3# 3
CN24	USB3.0 PIN HEADER
CN25	SATA3# 4
CN26	PCIE X8 SLOT
CN27	PCIE X8 SLOT
CN28	PCIE X8 SLOT
CN29	PCIE X8 SLOT
CN30	PCIE X8 SLOT
CN31	I/O Connector
CN33	SATA DOM PWR
CN34	VR12_I2C PIN HEADER
CN35	USB PIN HEADER
CN36	VGA BOX HEADER
CN37	ATX_SWITCH
CN38	CPLD JTAG
CN39	DEBUG GPIO
CN40	ATX I2C Connector
CN41	MINI-PCIE
CN43	FRONT PANEL PIN HEADER
CN44	ATX_8PIN
CN45	LPC PIN HEADER
CN47	KEY PAD PIN HEADER

JP1	VCORE TEST PIN
JP2	ATX/AT SELECT
JP3	H/W OR S/W RESET
JP4	CLEAR CMOS
JP6	BYPASS LED OR GPIO LED
JP7	I210_PCIE RESET PIN
FAN1	CPU FAN (RESERVED)
FAN7_2	SYSTEM FAN*2 (1U)
FAN8_3	SYSTEM FAN*2 (1U)
FAN9_4	SYSTEM FAN*2 (1U)
FAN10_5	SYSTEM FAN*2 (1U)

CN1 : VR12_I2C

PIN	Description
1	GND
2	DATA
3	CLK

CN2 , CN48 : USB2.0 PIN HEADER

PIN	Description	PIN	Description
1	+ 5V	2	+ 5V
3	USB_CON_PN2	4	USB_CON_PN3
5	USB_CON_PP2	6	USB_CON_PP3
7	GND	8	GND
9	NC	10	GND

CN3 : VGA BOX HEADER

PIN	Description	PIN	Description
1	DACRO	2	DACGO
3	DACBO	4	NC
5	GND	6	GND
7	GND	8	GND
9	+ 5V	10	GND

11	NC	12	DDCDAT
13	HSYNC	14	VSYNC
15	DDCCLK	16	NC

CN4 : ATX_SWITCH

PIN	Description
1	GND
2	PANSWIN#_CONN

CN5 : CPLD JTAG

PIN	Description	PIN	Description
1	CPLD_TCK	2	GND
3	CPLD_TDO	4	3.3V_AUX
5	CPLD_TMS	6	NC
7	NC	8	NC
9	CPLD_TDI	10	GND

CN6 : DEBUG GPIO

PIN	Description
1	GPIO57#
2	GND

CN10: ATX I2C Connector

PIN	Description
1	CLK
2	DAT
3	GPI
4	GND
5	+3.3V

CN11: MINI - PCIE

CN13 : FRONT PANEL PIN HEADER

PIN	Description	PIN	Description
1	+3.3V_PU	2	GND
3	+3.3V_PU	4	HDD_LED_N

5	RESET_BTN_N	6	GND
7	GND	8	PANSWIN_N

CN15 : ATX_8PIN

PIN	Description	PIN	Description
1	GND	5	+12V
2	GND	6	+12V
3	GND	7	+12V
4	GND	8	+12V

CN16 : LPC PIN HEADER

PIN	Description	PIN	Description
1	+3.3V	2	LPC_AD0
3	LPC_AD1	4	LPC_AD2
5	LPC_AD3	6	FRAME_N
7	RST_LPC	8	+5V
9	CLK_33MHZ	10	PME_N
11	GND	12	NC
13	SERIRQ	14	LDRQ1

CN17 : KEY PAD PIN HEADER

PIN	Description
1	P_ACK
2	P_BUSY
3	P_PE
4	P_SLCT
5	GND
6	P_ERR#

CN18 : COM2 BOX HEADER

PIN	Description	PIN	Description
1	DCD	2	DSR
3	RXD	4	RTS
5	TXD	6	CTS
7	DTR	8	RI

9	GND	10	NC

CN20 : GPI PIN HEADER

PIN	Description
1	SIO_GPI4
2	SIO_GPI5
3	SIO_GPI6
4	SIO_GPI7
5	GND

CN22 : PS2 MS/KB PIN HEADER

PIN	Description	PIN	Description
1	L_KCLK	2	L_MCLK
3	L_KDAT	4	L_MDAT
5	NC	6	NC
7	GND	8	GND
9	+5V	10	+5V

CN23 : PCIE +12V_ATX4PIN(RESERVED)

PIN	Description	PIN	Description
1	GND	3	+12V
2	GND	4	+12V

CN24 : GPO PIN HEADER

PIN	Description	PIN	Description
1	SIO_GP70#	2	+3.3V_PU
3	SIO_GP71	4	+3.3V_PU
5	SIO_GP72	6	+3.3V_PU
7	SIO_GP73	8	+3.3V_PU
9	GND	10	+3.3V

CN25 : SPI PIN HEADER

PIN	Description	PIN	Description
1	VCC3_SPI	2	GND
3	SF_SPI_CS0_N	4	SF_SPI_CLK

5	SF_SPI_MISO	6	SF_SPI_MOSI
7	NC	8	FLASH_IO

CN27 : KEY PAD PIN HEADER

PIN	Description	PIN	Description
1	+ 5V	2	GND
3	AFD#	4	NC
5	INIT#	6	SLIN#
7	PD1	8	PD0
9	PD3	10	PD2
11	PD5	12	PD4
13	PD7	14	PD6
15	BK_CTRLN	16	BK_CTRLP

CN28 : ATX 24PIN

PIN	Description	PIN	Description
1	+ 3.3V	13	+ 3.3V
2	+ 3.3V	14	-12V
3	GND	15	GND
4	+ 5V	16	PS_ON
5	GND	17	GND
6	+ 5V	18	GND
7	GND	19	GND
8	POWER GOOD	20	RSVD
9	5VSB	21	+ 5V
10	+ 12V	22	+ 5V
11	+ 12V	23	+ 5V
12	+ 3.3V	24	GND

CN29 、CN31 、CN34 : SATA3

PIN	Description
1	GND
2	A+
3	A-
4	GND

5	B-
6	B+
7	GND

CN30: SATA DOM

PIN	Description
1	GND
2	A+
3	A-
4	GND
5	B-
6	B+
7	SATA_PWR

CN33 : USB3.0 PIN HEADER

PIN	Description	PIN	Description
1	+ 5V	11	USB2_PP1
2	USB3_RX0_N	12	USB2_PN1
3	USB3_RX0_P	13	GND
4	GND	14	USB3_TX1_P
5	USB3_TX0_N	15	USB3_TX1_N
6	USB3_TX0_P	16	GND
7	GND	17	USB3_RX1_P
8	USB2_PN0	18	USB3_RX1_N
9	USB2_PP0	19	+ 5V
10	NC	20	NC

CN35 、CN36 、CN37 、CN38 、CN40: PCIE X8 SLOT

CN45 : I/O Connector

PIN	Description	PIN	Description
1	LED_LAN1_LINK100#	2	LAN1_CON_0P
3	LED_LAN1_LINK1000#	4	LAN1_CON_0N
5	LED_LAN1_ACT#	6	LAN1_CON_1P
7	LED_LAN2_LINK100#	8	LAN1_CON_1N
9	LED_LAN2_LINK1000#	10	LAN1_CON_2P
11	LED_LAN2_ACT#	12	LAN1_CON_2N

13	+3.3V	14	LAN1_CON_3P
15	RTS_N1/CTS_N1	16	LAN1_CON_3N
17	DTR_N1	18	GND
19	TXD_N1	20	LAN2_CON_0P
21	RXD_N1	22	LAN2_CON_0N
23	DSR_N1	24	LAN2_CON_1P
25	GPIO_BYPASS	26	LAN2_CON_1N
27	SIO_GP55	28	LAN2_CON_2P
29	SIO_GP56	30	LAN2_CON_2N
31	SIO_GP57	32	LAN2_CON_3P
33	HDD_LED_N	34	LAN2_CON_3N
35	RIA_N2	36	3.3V_AUX
37	DTR_N2	38	P80_CTRL
39	GND	40	RESET_BTN#_NM#

CN47 : SATA DOM PWR

PIN	Description
1	+5V
2	GND

FAN1: FAN

PIN	Description
1	GND
2	12V
3	SENSE
4	Control

FAN7 -2、8-3、9-4、10-5 :FAN

PIN	Description
1	GND
2	FANIN1
3	+12V
4	NC
5	FANIN2

6	NC
7	FANCTL

Jumper List	
JP1	TEST VCORE PIN
NC	(DEFAULT)
1-2	TEST

JP2	ATX/AT SELECT
1-2	ATX (DEFAULT)
2-3	AT

JP3	H/W OR S/W RESET
1-2	H/W RESET (DEFAULT)
2-2	S/W RESET

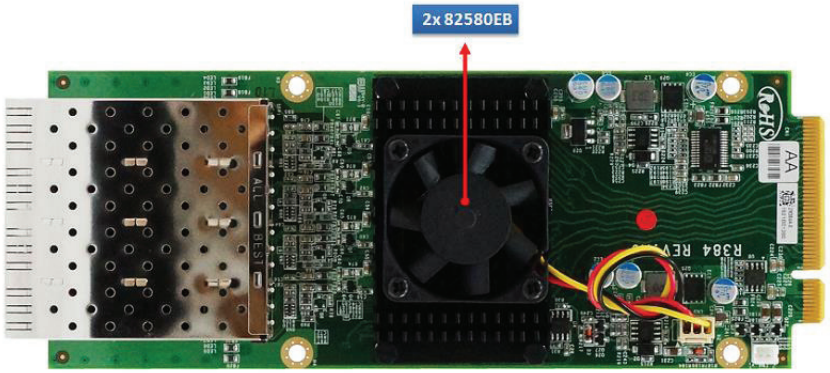
JP4	CLEAR CMOS
1-2	Normal (DEFAULT)
2-3	Clear CMOS

JP6	BYPASS LED OR GPIO LED
1-2	GPIO54# (DEFAULT)
2-3	ALL BYPASS#

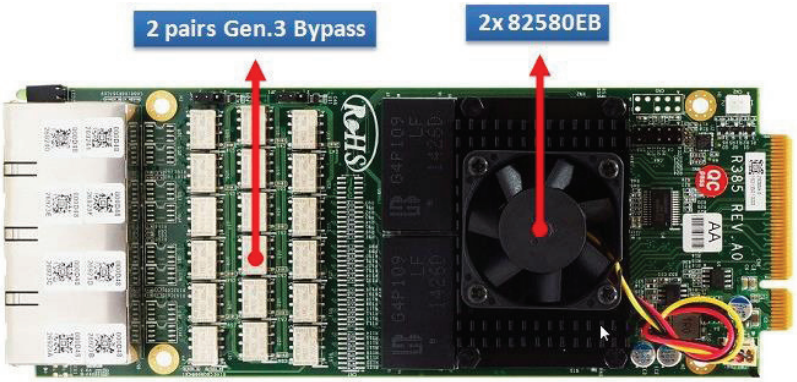
JP7	I210_PCIE RESET PIN
1-2	RESET (DEFAULT)
2-3	V3P3_AUX_PU

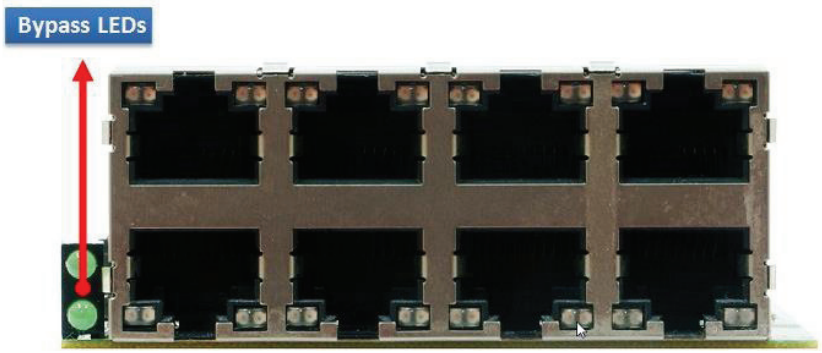
Chapter 3 Optional LAN Module & Add-on Card Settings

3. 1 IP-384A : Expansion module with 8 SFP GbE ports, Intel 82580EB

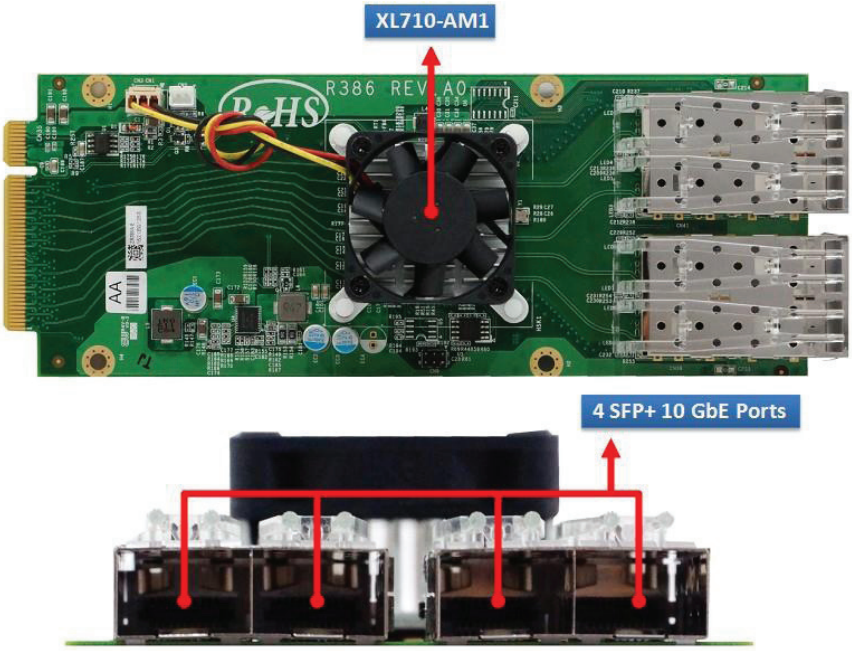


3. 2 IP- 385A : Expansion module with 8 RJ45 GbE ports with two pairs Gen.3 bypass, Intel 82580E B

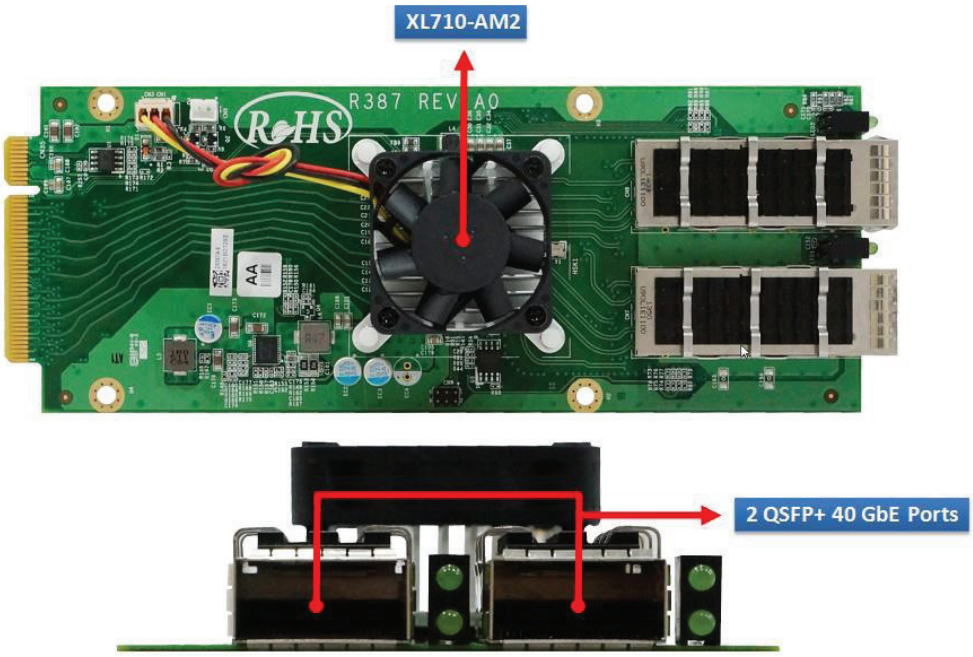




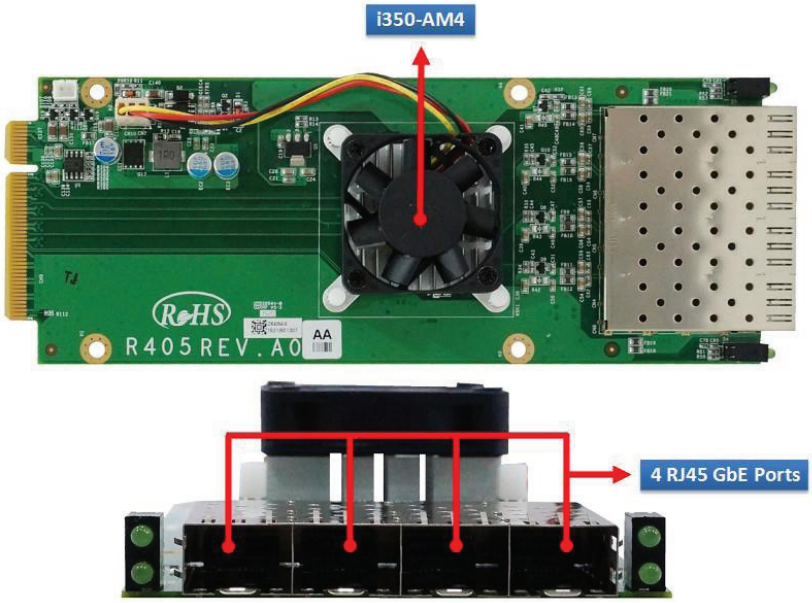
3. 3 IP- 386A : Expansion module with 4 SFP+ 10 GbE ports, Intel XL710 - B M1 w/o re - driver



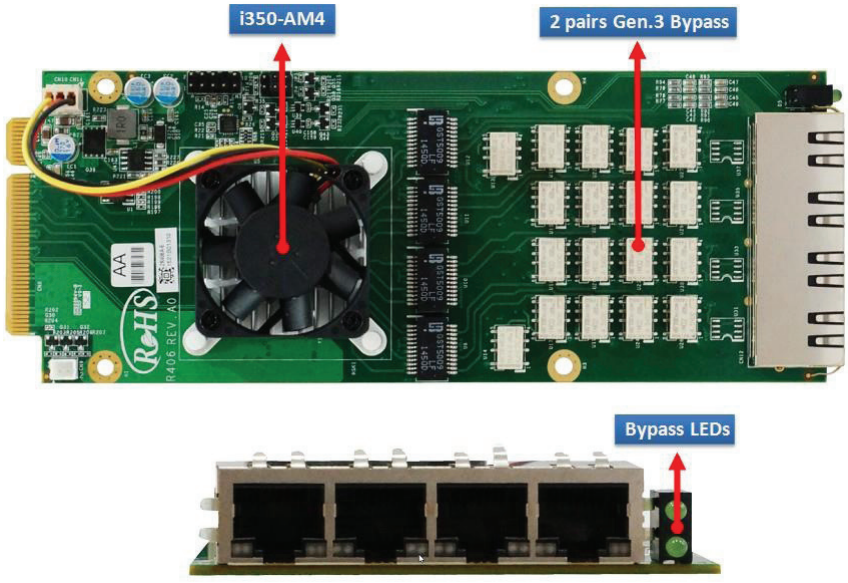
3.4 IP-387A: Expansion module with 2 Q SFP+ 40 GbE ports, Intel XL710 - B M2 w/o re - driver



3.5 IP-405A: Expansion module with 4 SFP GbE ports, Intel i350 - AM4

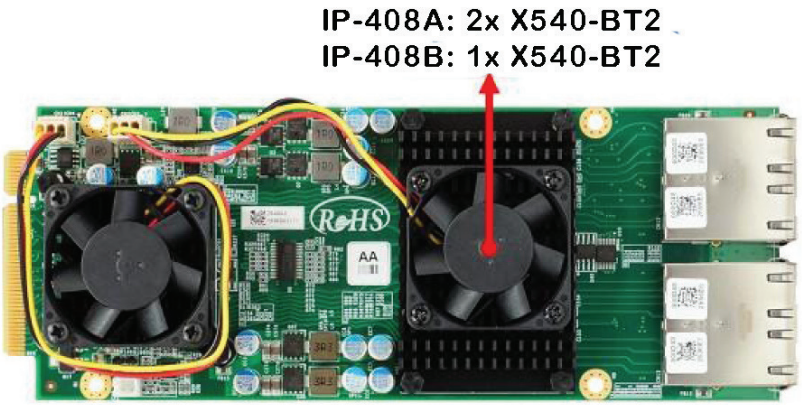


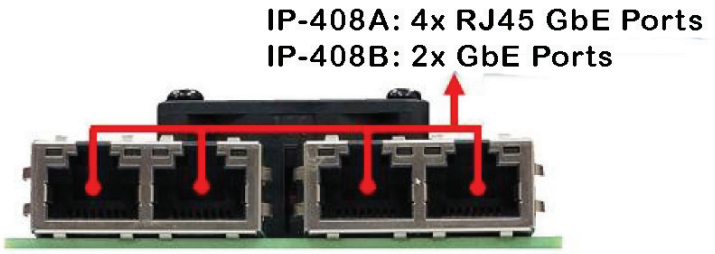
3.6 IP-406A: Expansion module with 4 RJ45 GbE ports with two pairs Gen.3 bypass, Intel i350- A M4



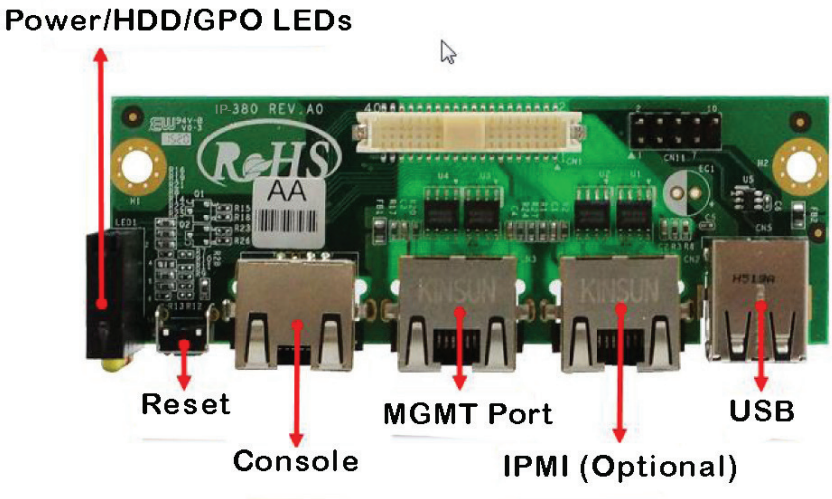
3.7 IP-408A: Expansion module with 4 RJ45 10G ports, Intel X540 - BT 2

3.8 IP-408B: Expansion module with 2 RJ45 10G ports, Intel X540 - BT2





3. 9 IP- 380A : Front I/O module



IP-380A is a front I/O module with GPO LEDs, two USB 2.0 port, one RJ45 console port (COM1), two GbE port.

Chapter 4. BIOS Setup

The ROM chip of your IP-80930 board is configured with a customized Basic Input/Output System (BIOS) from AMI BIOS. The BIOS is a set of permanently recorded program routines that give the system its fundamental operational characteristics. It also tests the computer and determines how the computer reacts to instructions that are part of programs.

The BIOS is made up of code and programs that provide the device-level control for the major I/O devices in the system. It contains a set of routines (called POST, for Power-On Self Test) that check out the system when you turn it on. The BIOS also includes BIOS setup program, so no disk-based setup program is required CMOS RAM stores information for:

- Date and time
- Memory capacity of the appliance
- Type of display adapter installed
- Number and type of disk drives

The CMOS memory is maintained by battery installed on the PL-80930 board. By using the battery, all memory in CMOS can be retained when the system power switch is turned off. The system BIOS also supports easy way to reload the CMOS data when you replace the battery of the battery power lose.

4.1 Quick Setup

In most cases, you can quickly configure the system by choosing the following main menu options:

1. Choose "Exit" > "Load Optimal Defaults" from the main menu. This loads the setup default values from the BIOS Features Setup and Chipset Features Setup screens.
2. Choose "Main" & "Advanced" from the main menu. This option lets you configure the date and time, hard disk type, floppy disk drive type, primary display and more.
3. In the main menu, press F4 ("Save and Exit") to save your changes and reboot the system.

4.2 Entering the BIOS Setup Utility

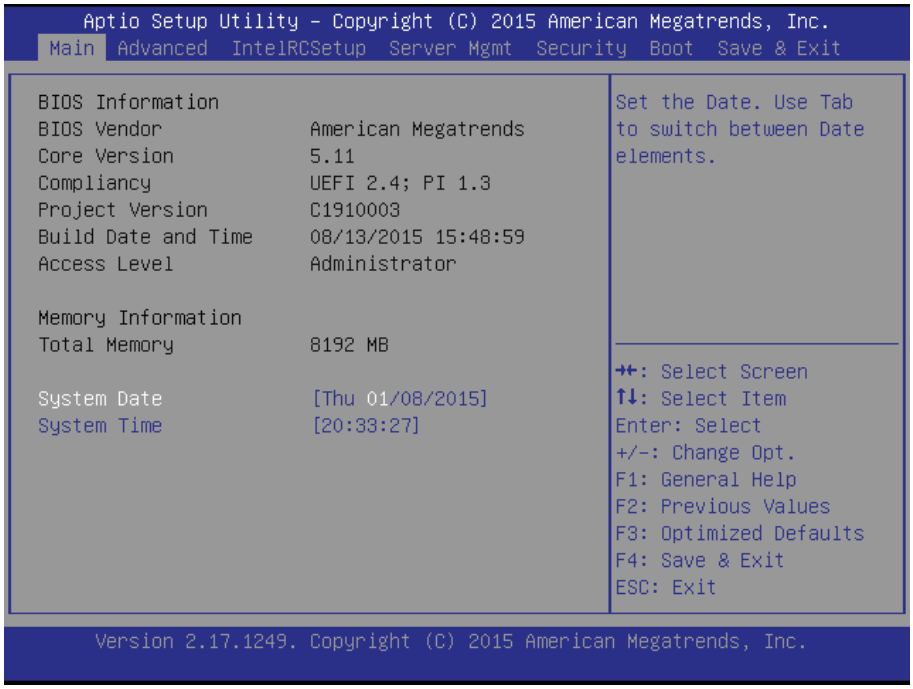
Use the BIOS setup program to modify the system parameters to reflect the options installed in your system and to customize your system. For example, you should run the Setup program after you:

- Received an error code at startup
- Install another disk drive
- Use your system after not having used it for a long time
- Find the original setup missing
- Replace the battery
- Change to a different type of CPU
- Run the AMI Flash program to update the system BIOS

Run the BIOS setup program after you turn on the system. On-screen instructions explain how to use the program.

⇩ Enter the BIOS setup program's main menu as follows:

1. Turn on or reboot the system. After the BIOS performs a series of diagnostic checks, the following message appears:
   "Press DEL to enter SETUP"
2. Press the <DEL> key to enter BIOS setup utility. The main menu appears:



3. Choose a setup option with the arrow keys and press <Enter>. See the following sections for a brief description of each setup option.

BIOS Information

Displays the BIOS related information.

Memory Information

Displays the total memory size.

System Language

Change the language display in BIOS setup utility.

System Date [Day mm/dd/yyyy]

This item allows you to set the system date.

SystemTime: [hour:min:sec]

This item allows you to set the system time.

In the main menu, press F4 ("Save and Exit") to save your changes and reboot the system. Press F3 ("Optimized Defaults") to load the Optimal default configuration values of the menu. Pressing <ESC> anywhere in the program returns you to the main menu.

4.3 Menu Options

The main menu options of the BIOS setup program are described in the following and the following sections of this chapter.

Main

For changing the basic system configurations.

Advanced

For changing the advanced system settings.

IntelRCSetup

To customize the Intel chipset functions

Server Mgmt

For changing the Server Mgmt settings

Security

For setting User and Supervisor Passwords.

Boot

For changing the system boot configurations.

Save & Exit

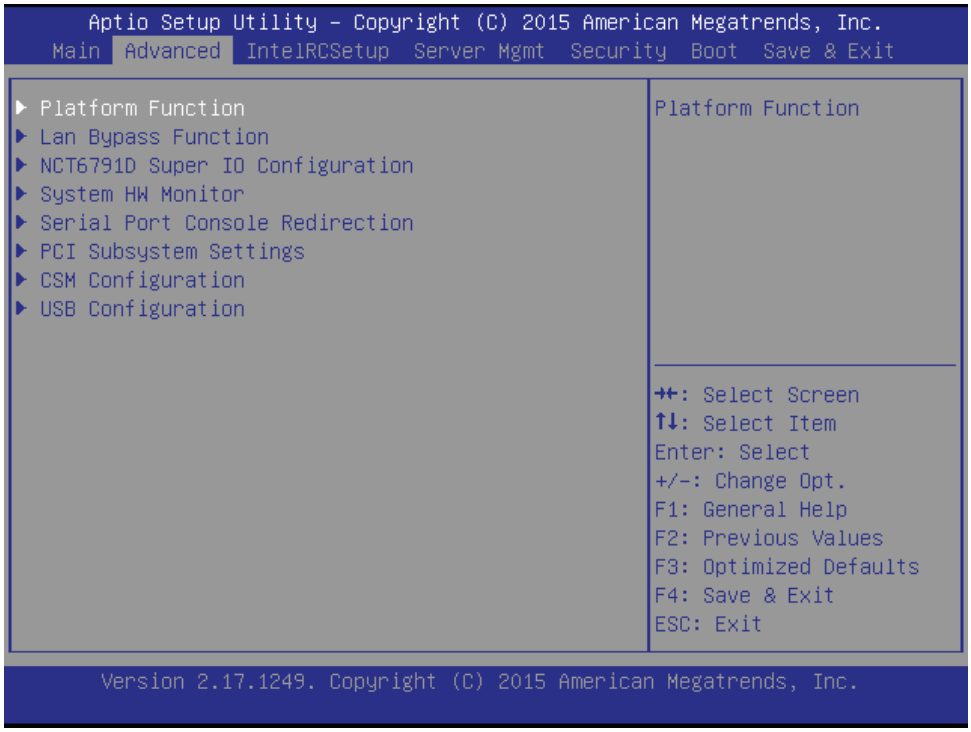
For selecting the exit options and loading default settings.

4.4 Advanced Menu

The Advanced menu items allow you to change the settings for the CPU and other system devices.

⇩Use the Advanced Setup option as follows:

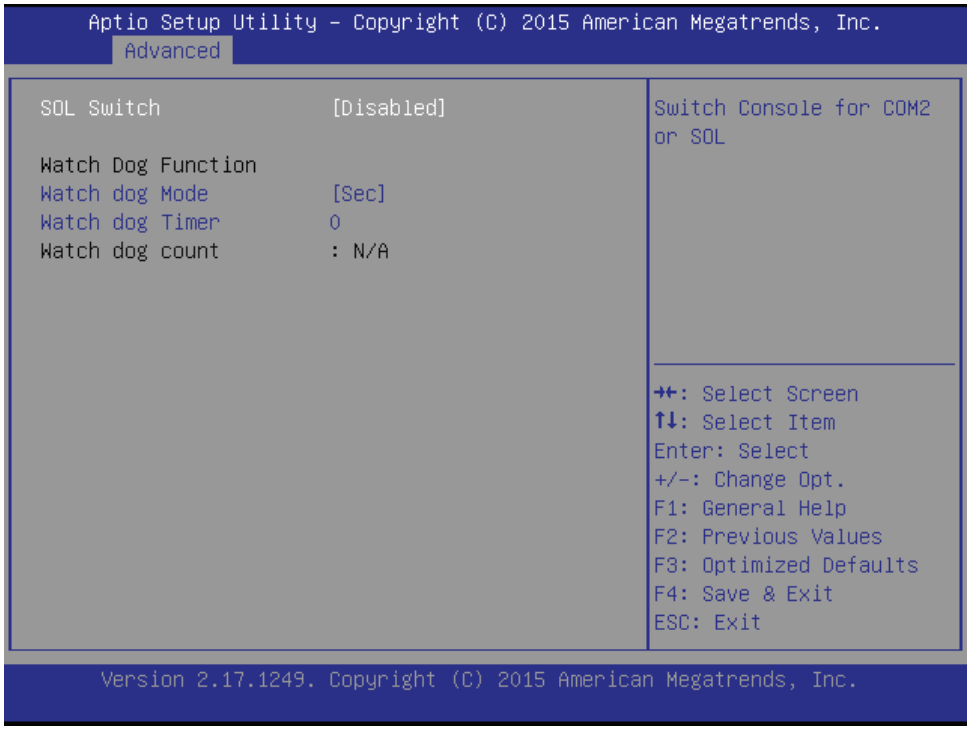
1. Choose "Advanced" from the main menu. The following screen appears:



2. Use the arrow keys to move between fields. Modify the selected field using the PgUP/PgDN/+ /- keys. Some fields let you enter numeric values directly.

3. After you have finished with the Advanced setup, press the < ? > or < ? > key to switch to other setup menu or press < F4> key to save setting.

4.4.1 Platform Function



SOL Switch

Switch Console for COM2 or SOL

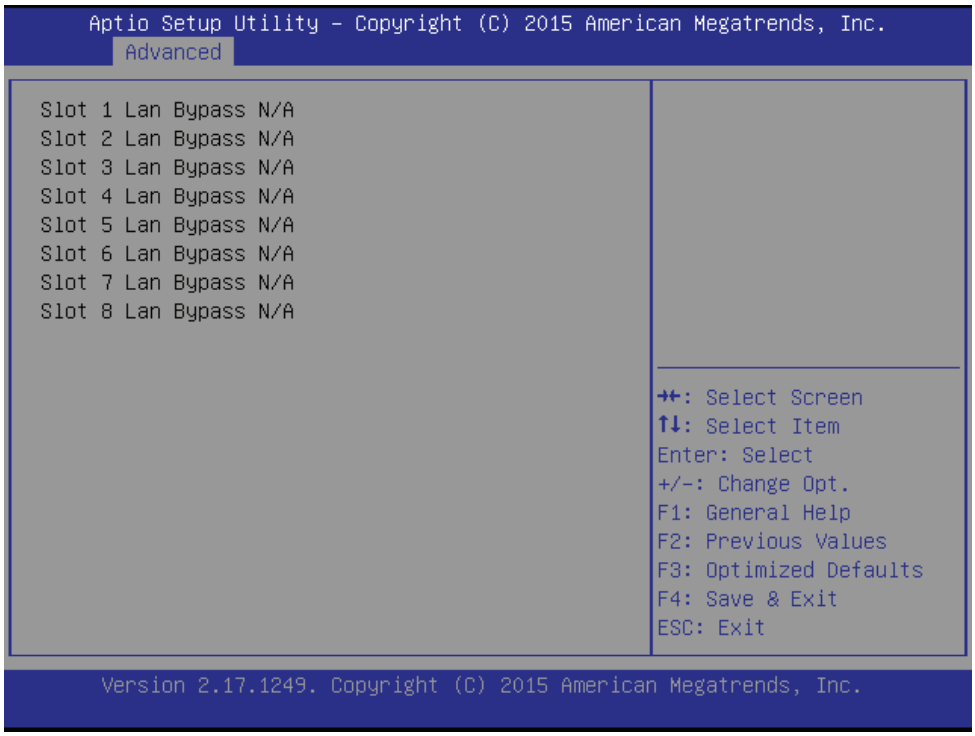
Watch dog Mode

Watch dog Mode（Sec/Min）.

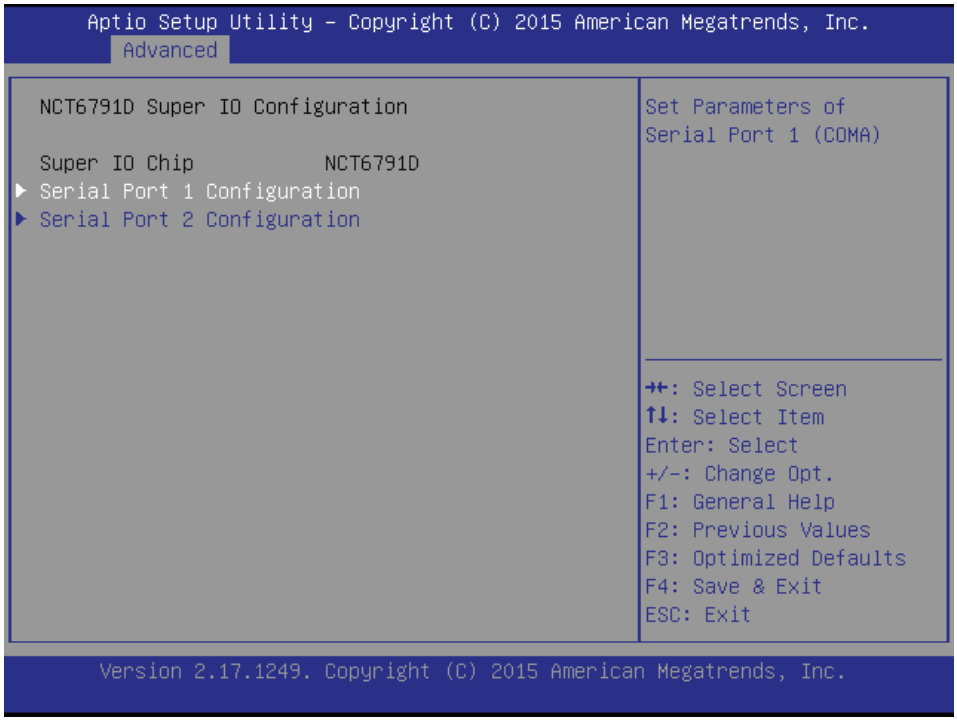
Watch dog Timer

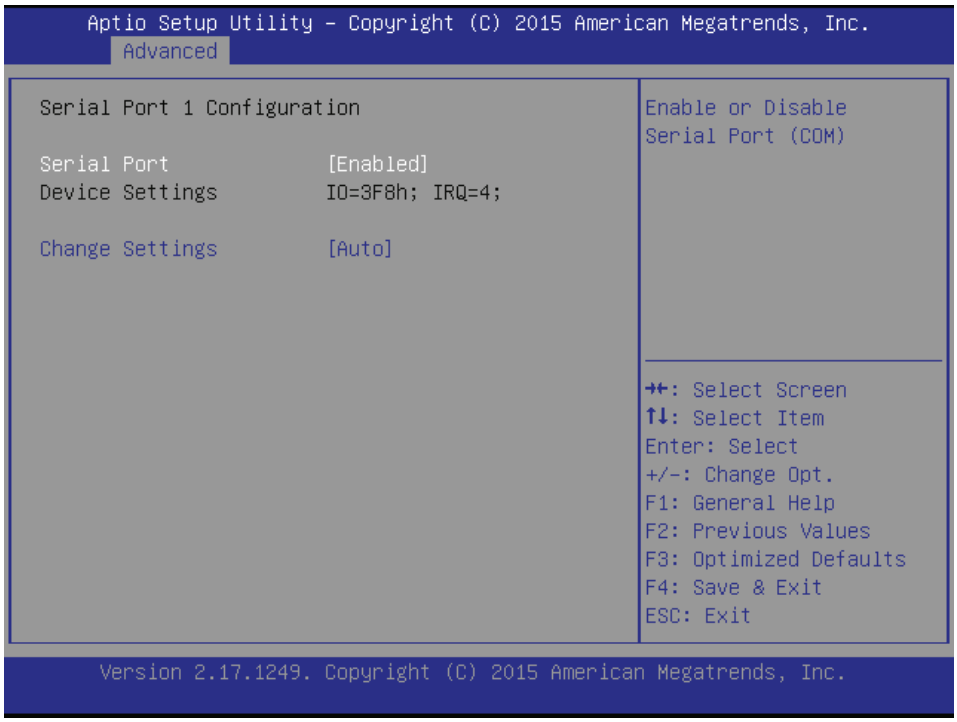
Watch dog Mode（Sec/Min）.

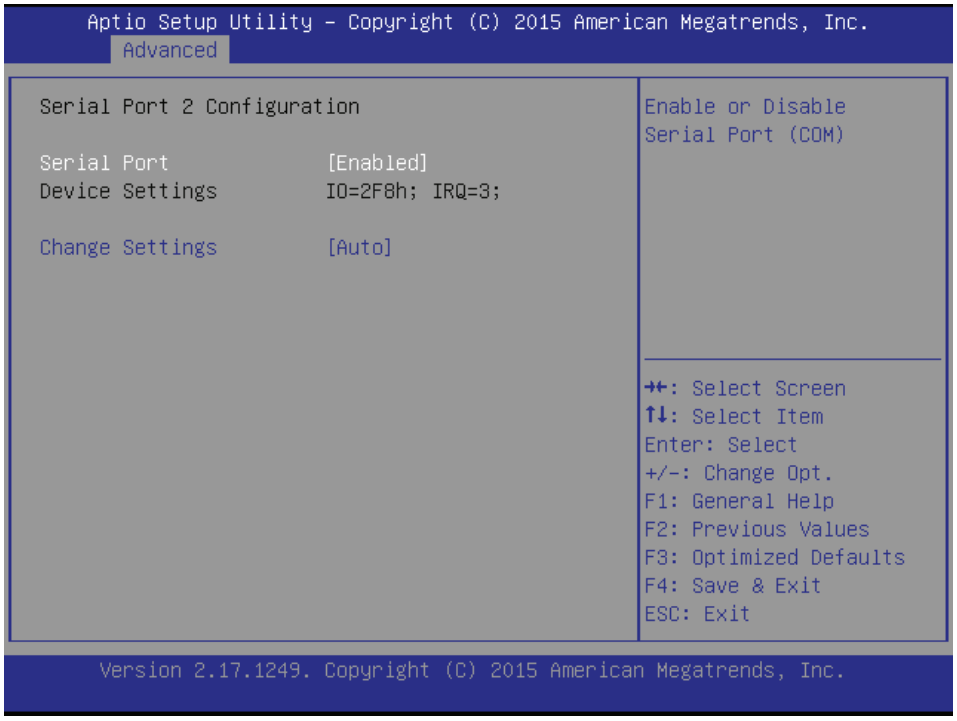
4.4.2 LAN Bypass Function



4.4.3 NCT6791D Super IO Configuration







Serial Port 1 Configuration

Set Parameters of Serial Port 1

Serial Port 2 Configuration

Set Parameters of Serial Port 2

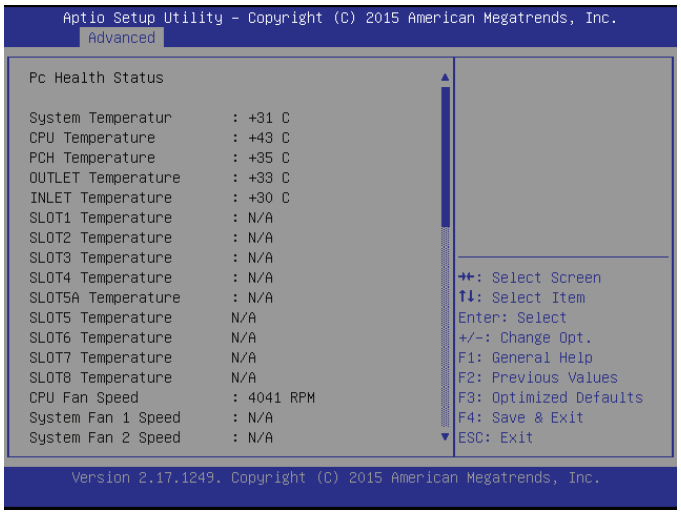
Serial Port

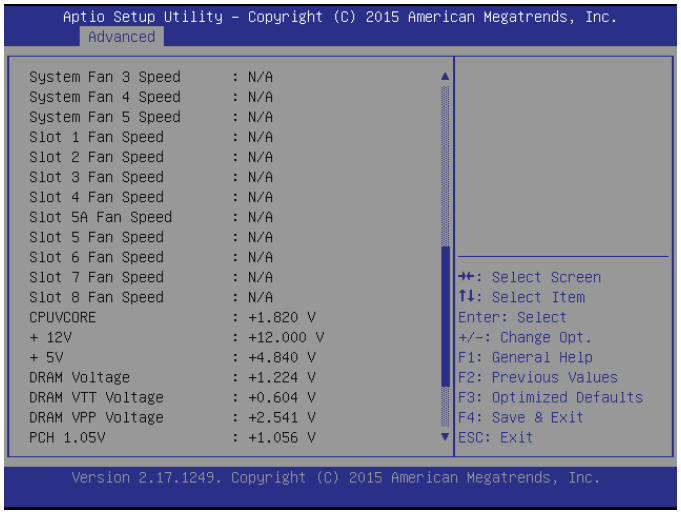
Enables or Disables Serial Port

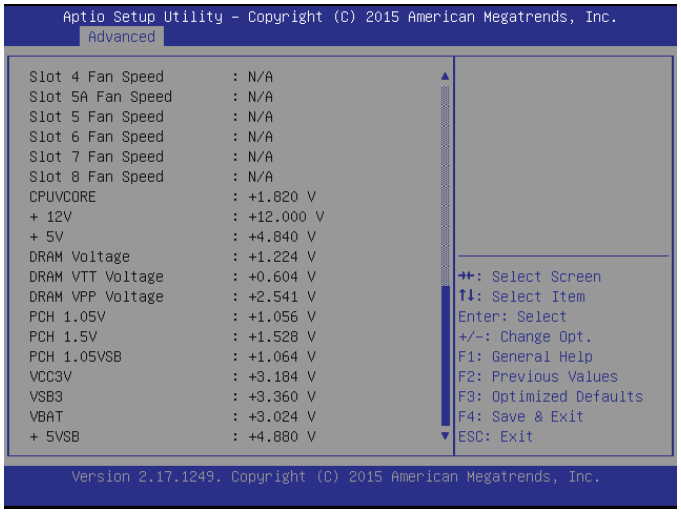
Change Setting

Device Settings

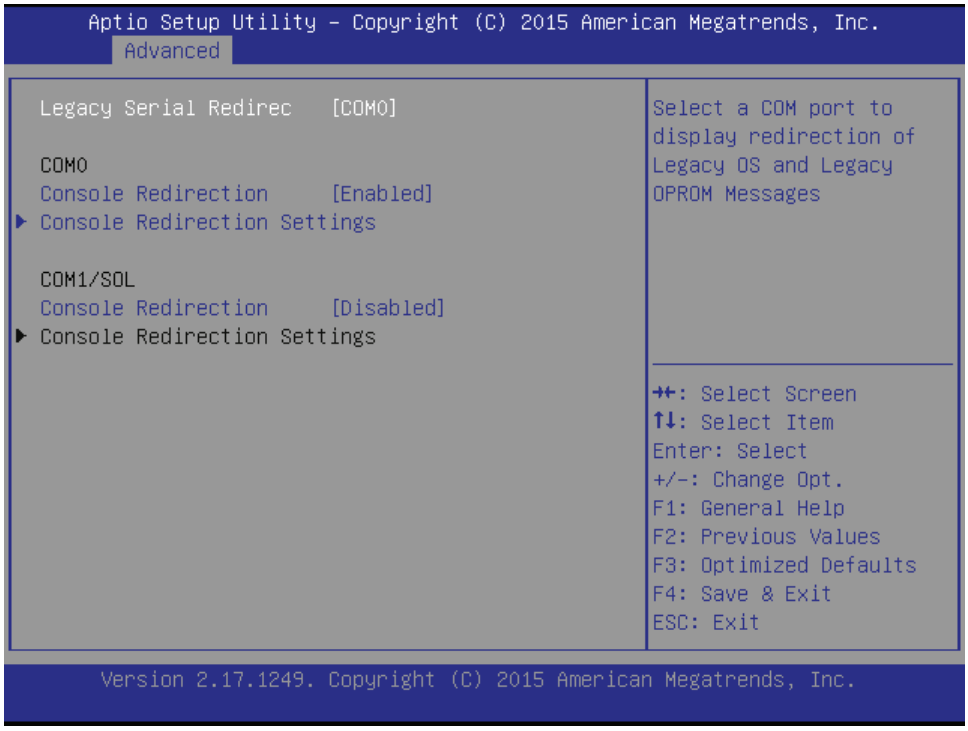
4.4.4 System Hardware Monitor







4.4.5 Serial Port Console Redirection



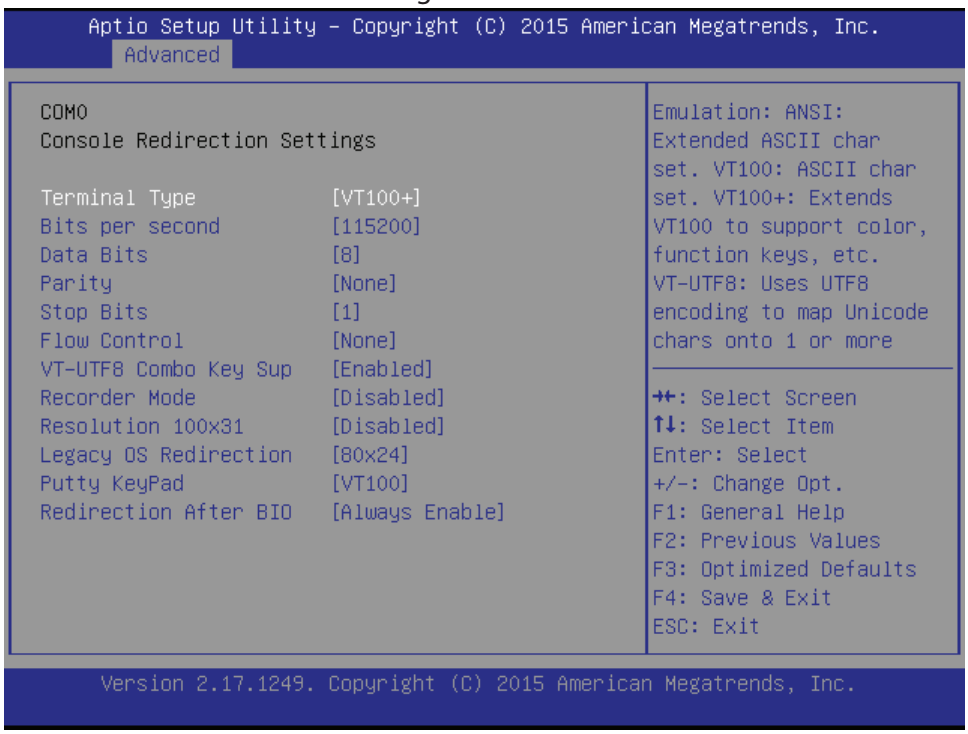
Legacy Serial Redirection Port

Select a COMport to display redirection of Legacy OS and Legacy OPROMMessages

COM0/COM1 Console Redirection

Console Redirection Enable or Disable.

4.4.5.1 Console Redirection settings



Terminal Type

Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.

Bits per second

Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

Data Bits

Data Bits.

Parity

A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Flow Control

Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

VT - UTF8 Combo Key Support

Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.

Recorder Mode

With this mode enabled only text will be sent. This is to capture Terminal data.

Resolution 100x31

Enables or disables extended terminal resolution.

Legacy OS Redirection Resolution

On Legacy OS, the Number of Rows and Columns supported redirection.

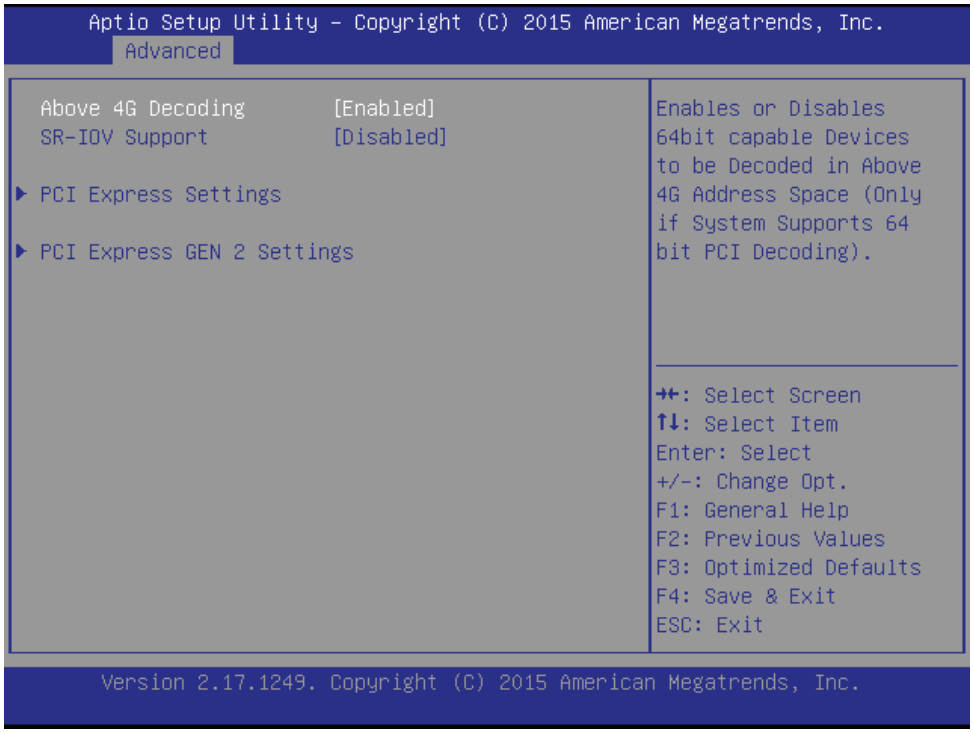
Putty KeyPad

Select FunctionKey and KeyPad on Putty.

Redirection After BIOS POST

The Settings specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legacy console Redirection is enabled for Legacy OS.

4.4.6 PCI Subsystem Settings



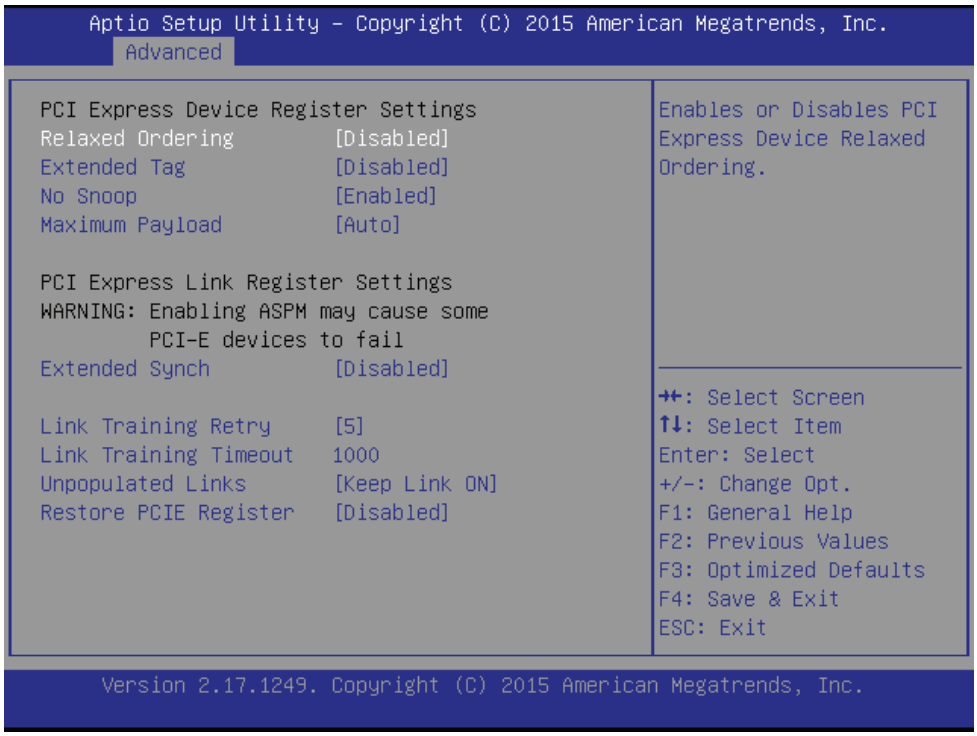
Above 4G Decoding

Enables or Disables 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).

SR -IOV Support

If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.

4.4.6.1 PCI Express Settings



Relaxed Ordering

Enables or Disables PCI Express Device Relaxed Ordering.

Extended Tag

If ENABLED allows Device to use 8-bit Tag field as a requester.

No Snoop

No Snoop Enable/Disable for each CB device

Maximum Payload

Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

Extended Synch

If ENABLED allows generation of Extended Synchronization patterns.

Lin k Training Retry

Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

Link Training Timeout

Defines number of Mcroseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 10000 uS.

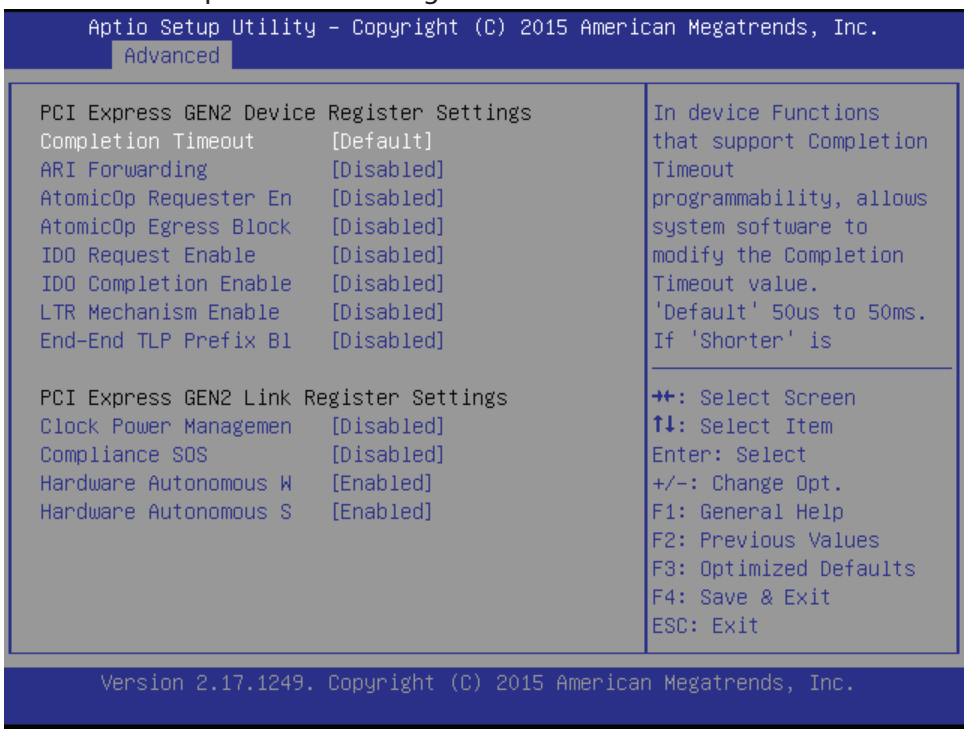
Unpopulated Links

In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

Restore PCIE Registers

On non-PCI Express aware OS's (Pre Windows Vista) some devices may not be correctly reinitialized after S3. Enabling this restores PCI Express device configurations on S3resume. Warning: Enabling this may cause issues with other hardware after S3resume.

4.4.6.2 PCI Express Gen2 Setting



Completion Timeout

In device Functions that support Completion Timeout programmability, allows system software to modify the Completion Timeout value. 'Default' 50us to 50ms. If 'Shorter' is selected, software will use shorter timeout ranges supported by hardware. If 'Longer' is selected, software will use longer timeout ranges.

ARI Forwarding

If supported by hardware and set to 'Enabled', the Downstream Port disables its traditional Device Number field being 0 enforcement when turning a Type1 Configuration Request into a Type0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. Default value:

Disabled

AtomicOp Requester Enable

If supported by hardware and set to 'Enabled', this function initiates AtomicOp Requests only if Bus Master Enable bit is in the Command Register Set.

AtomicOp Egress Blocking

If supported by hardware and set to 'Enabled', outbound AtomicOp Requests via Egress Ports will be blocked.

IDO Request Enable

If supported by hardware and set to 'Enabled', this permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated.

IDO Completion Enable

If supported by hardware and set to 'Enabled', this permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated.

LTR Mechanism Enable

If supported by hardware and set to 'Enabled', this enables the Latency Tolerance Reporting (LTR) Mechanism.

End - End TLP Prefix Blocking

If supported by hardware and set to 'Enabled', this function will block forwarding of TLPs containing End-End TLP Prefixes.

Clock Power Management

If supported by hardware and set to 'Enabled', the device is permitted to use CLKREQ# signal for power management of Link clock in accordance to protocol defined in appropriate form factor specification.

Compliance SOS

If supported by hardware and set to 'Enabled', this will force LTSSM to send SKP Ordered Sets between sequences when sending Compliance Pattern or Modified Compliance Pattern.

Hardware Autonomous Width

If supported by hardware and set to 'Disabled', this will disable the hardware's ability to change link width except width size reduction for the purpose of correcting unstable link operation.

Hardware Autonomous Speed

If supported by hardware and set to 'Disabled', this will disable the hardware's ability to change link speed except speed rate reduction for the purpose of correcting unstable link operation.

4.4.7 CSM Configuration

CSM Support

Enable/Disable CSM Support.

GateA20 Active

UPON REQUEST - GA20 can be disabled using BIOS services. ALWAYS - do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

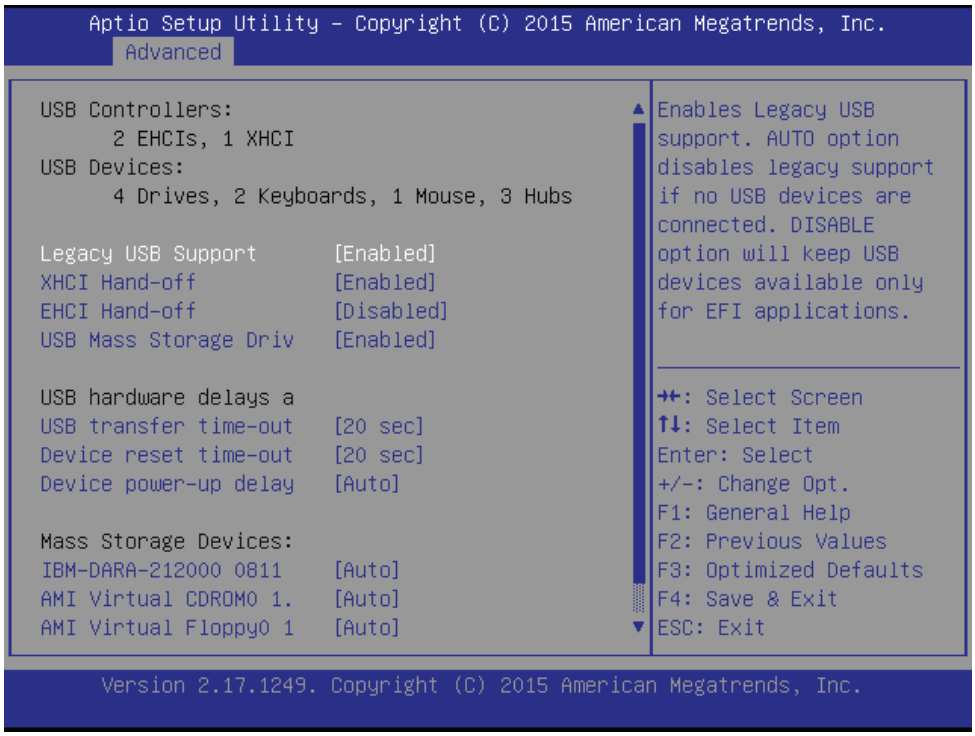
Option ROM Messages

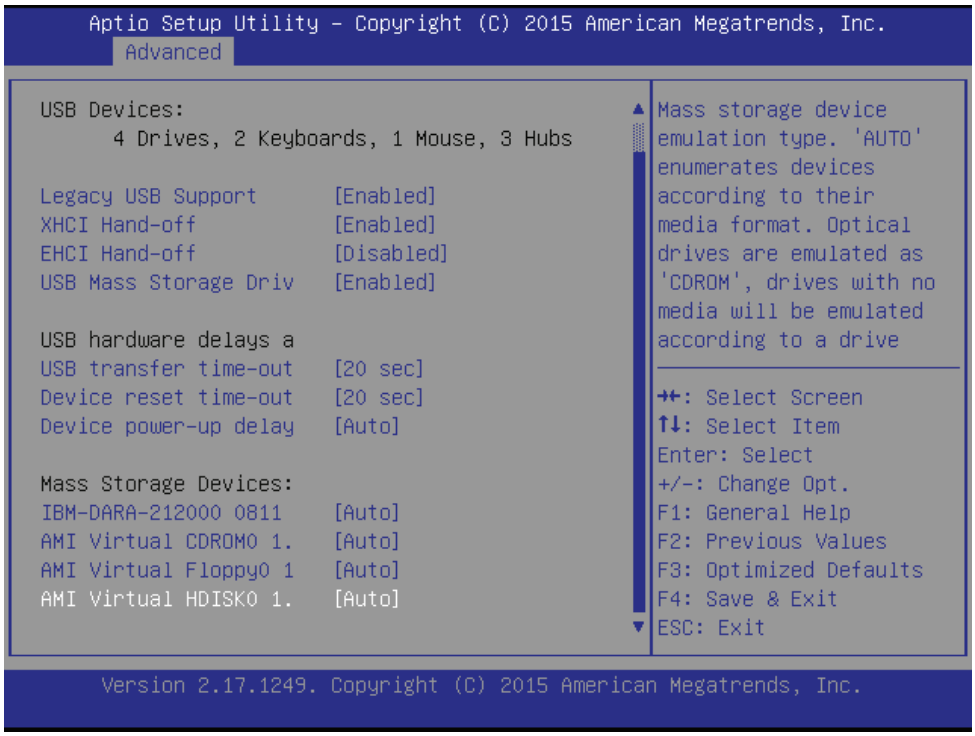
Set display mode for Option ROM

Boot option filter

This option controls Legacy/UEFI ROMs priority

4.4.8 USB Configuration





Legacy USB Support

Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

USB Mass Storage Driver Support

Enable/Disable USB Mass Storage Driver Support.

USB transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

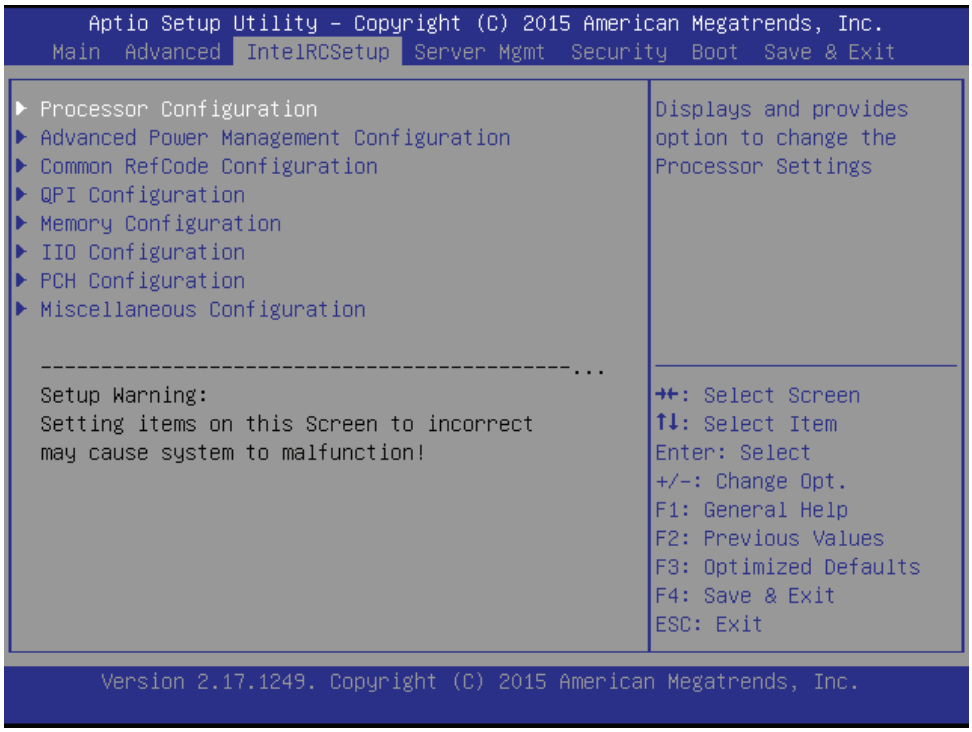
Device reset time-out

USB mass storage device Start Unit command time-out.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

4.5 IntelRCSetup



Processor Configuration

Displays and provides option to change the Processor Settings

Advanced Power Management Configuration

Displays and provides option to change the Power Management Settings

Common RefCode Configuration

Displays and provides option to change the Common RefCode Settings

QPI Configuration

Displays and provides option to change the QPI Settings

Memory Configuration

Displays and provides option to change the Memory Settings

IIO Configuration

Displays and provides option to change the IIO Settings

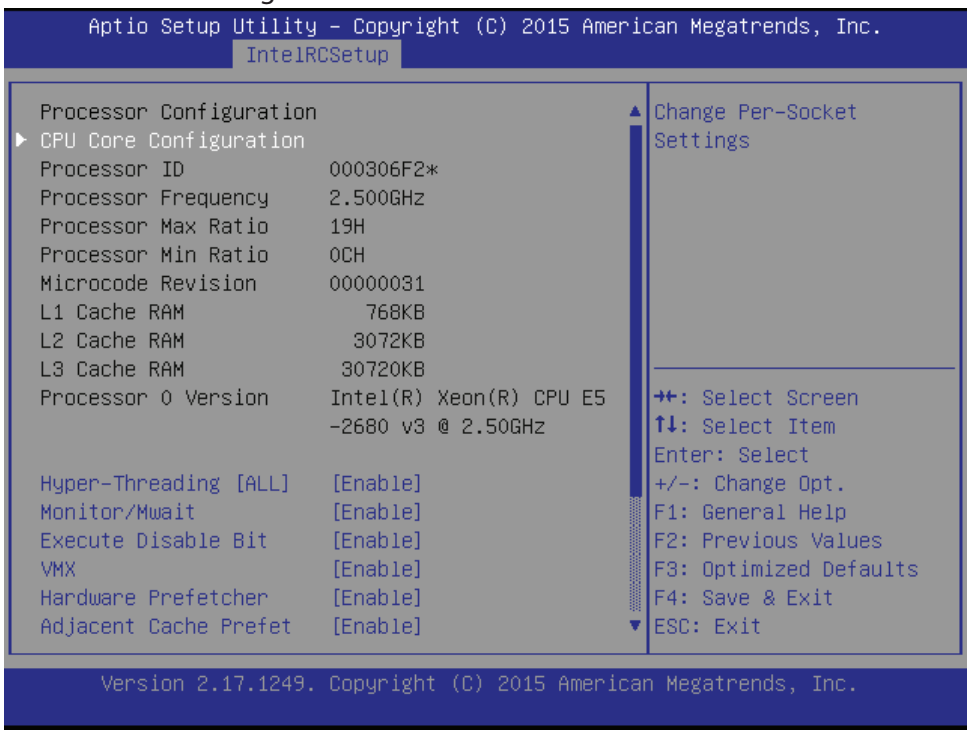
PCH Configuration

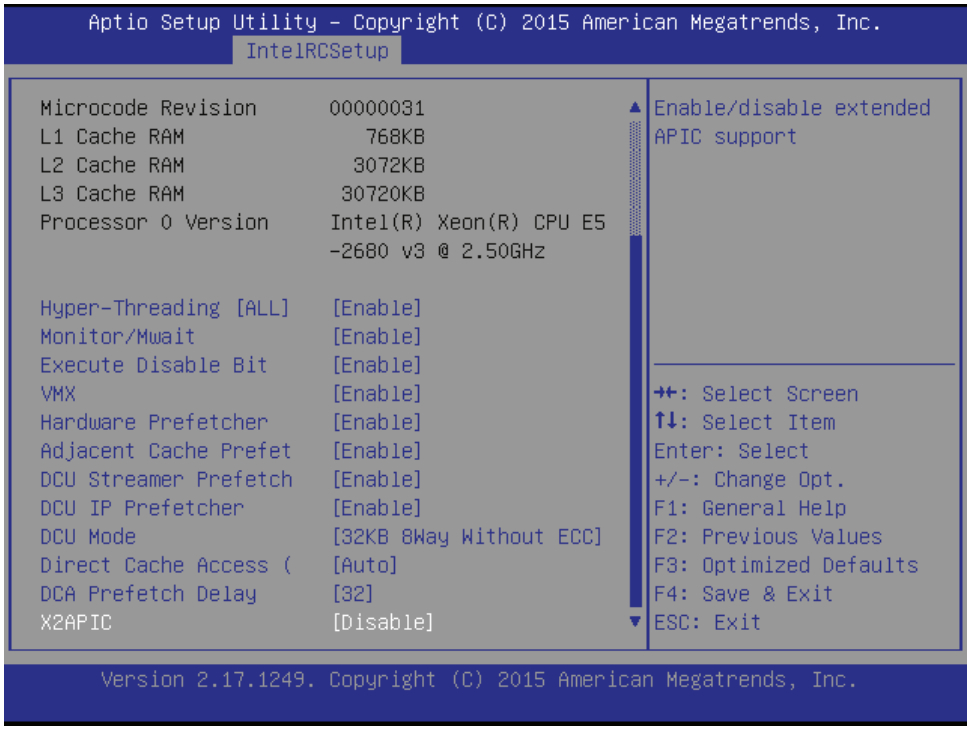
Displays and provides option to change the PCH Settings

Miscellaneus Configuration

Displays and provides option to change the Miscellaneous Settings

4.5.1 Processor Configuration





Hyper-threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology)

and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.

Monitor/Mwait

Enable or Disable the Monitor/Mwait instruction

Execute Disable Bit

XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3.)

VMX

Enables the Vanderpool Technology, takes effect after reboot.

Hardware Prefetcher

Enable the Mid Level Cache (L2) streamer prefetcher.

Adjacent Cache Prefetch

MLC Spatial Prefetcher

DCU Streamer Prefetcher

Enable prefetch of next L1 Data line based upon multiple loads in same cache line.

DCU IP Prefetcher

Enable prefetch of next L1 line based upon sequential load history.

DCU Mode

MSR 31h Bit[0] - A write of 1 selects the DCU mode as 16KB 4-way with ECC.

Direct Cache Access (DCA)

Enables Direct Cache Access

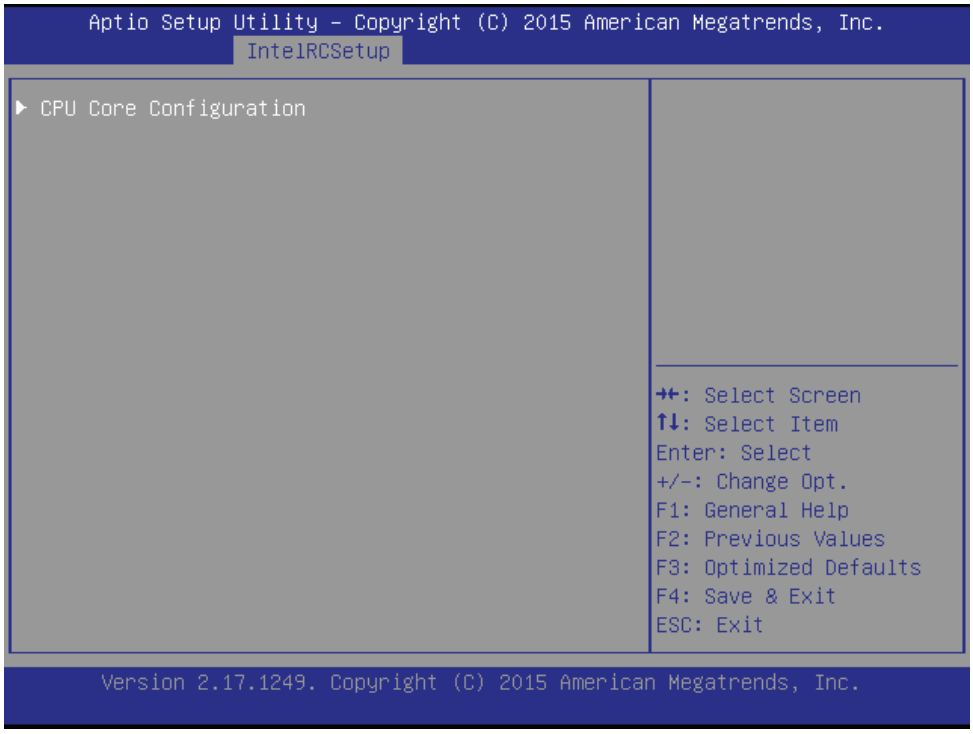
DCA Prefetch Delay

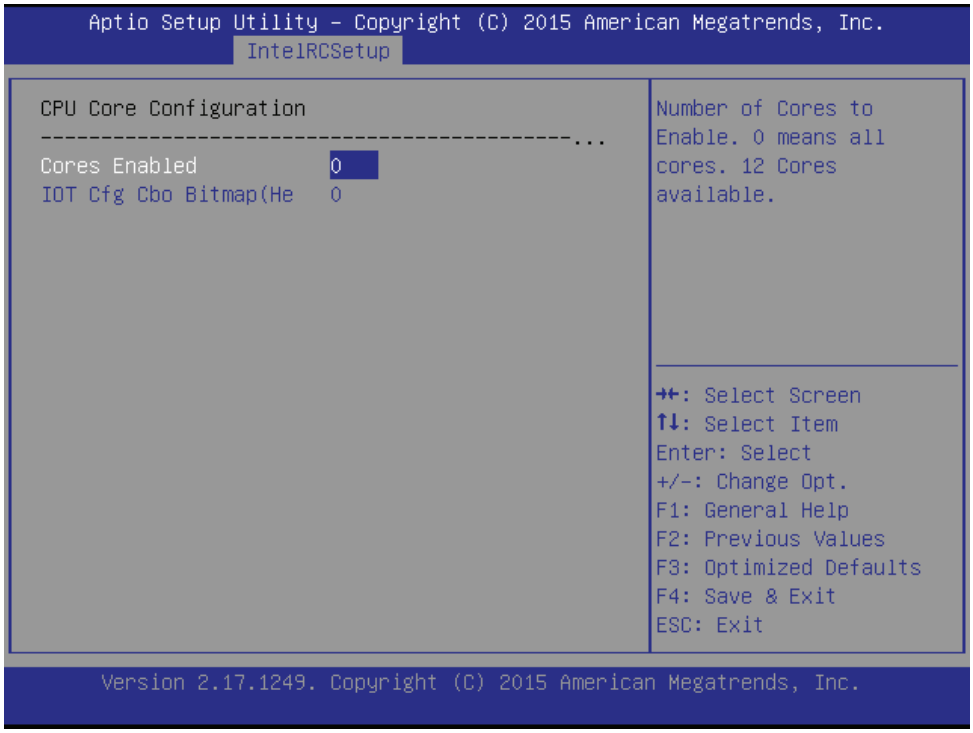
Enables Direct Cache Delay

X2APIC

Enable/disable extended APIC support

4.5.1.1 CPU Core Configuration





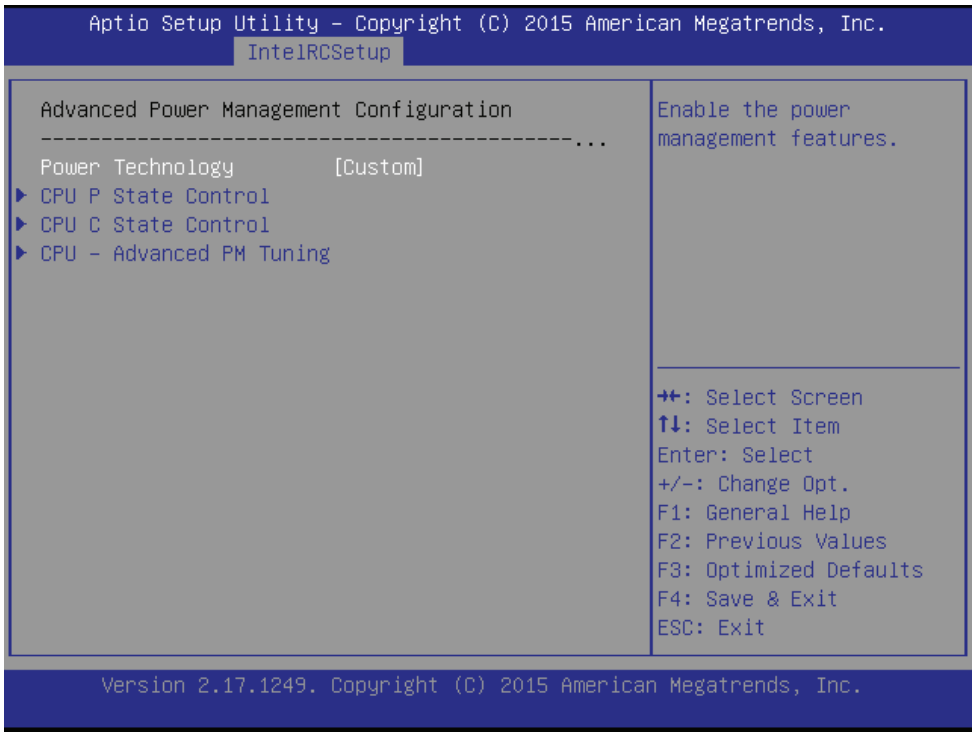
Cores Enable

Number of Cores to Enable. 0 means all cores. %d Cores available. In STR_CORE_ENABLE_HELP, %d will be replaced with number of cores.

IOT Cfg Cbo Bitmap

Each bit enables IOT/OCLA for a CBo.

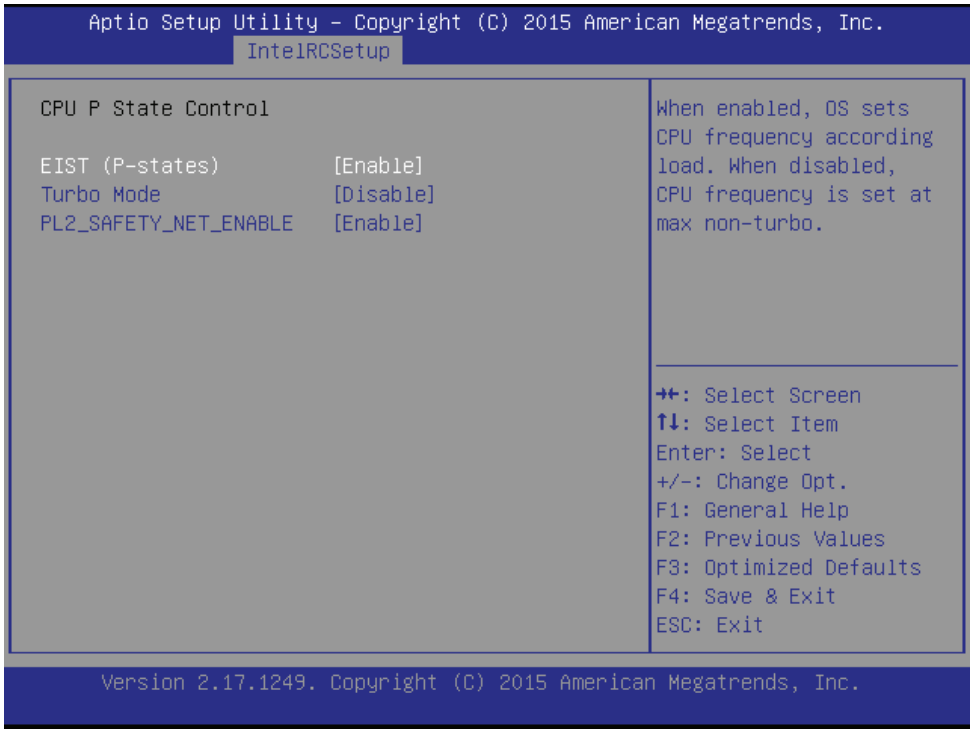
4.5.2 Advanced Power Management Configuration



Power Technology

Enable, disable or custom the power management features.

4.5.2.1CPU P State Control



EIST (P- states)

When enabled, OS sets CPU frequency according load. When disabled, CPU frequency is set at max non-turbo.

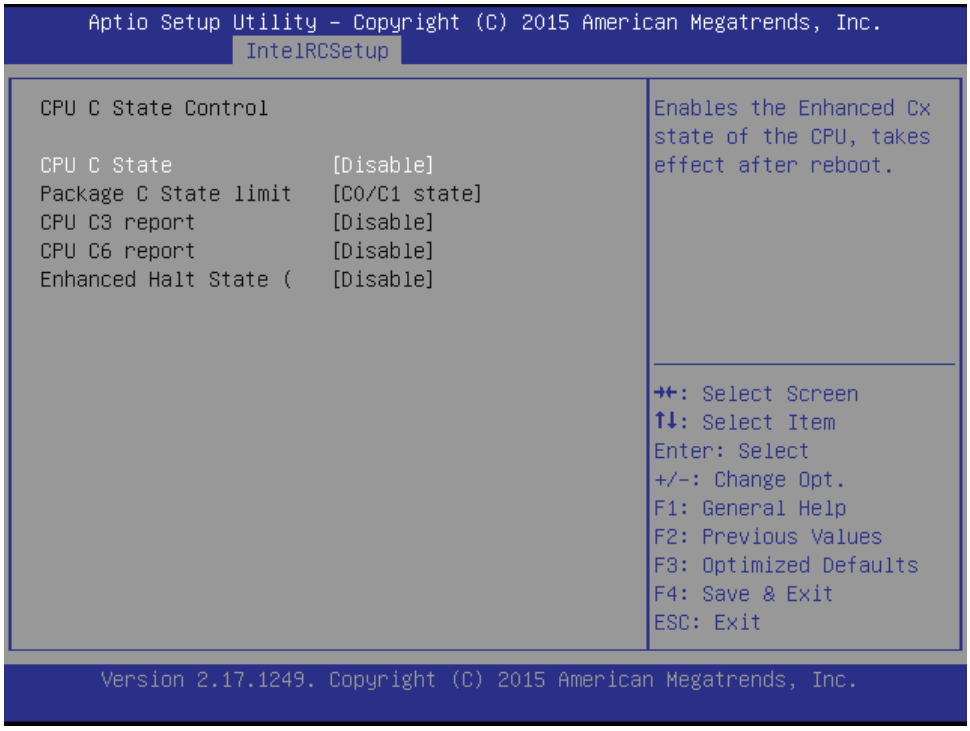
Turbo Mode

Turbo mode allows a CPU logical processor to execute a higher frequency when enough power is available not exceed CPU defined limits.

PL2_SAFETY_NET_ENABLE

Enable PL2_Safety

4.5.2.2 CPU C State Control



CPU C State

Enables the Enhanced Cx state of the CPU, takes effect after reboot.

P a ckage C State limit

Package C State limit

CPU C3 report

Enable/Disable CPU C3(ACPI C2) report to OS. Recommended to be disabled.

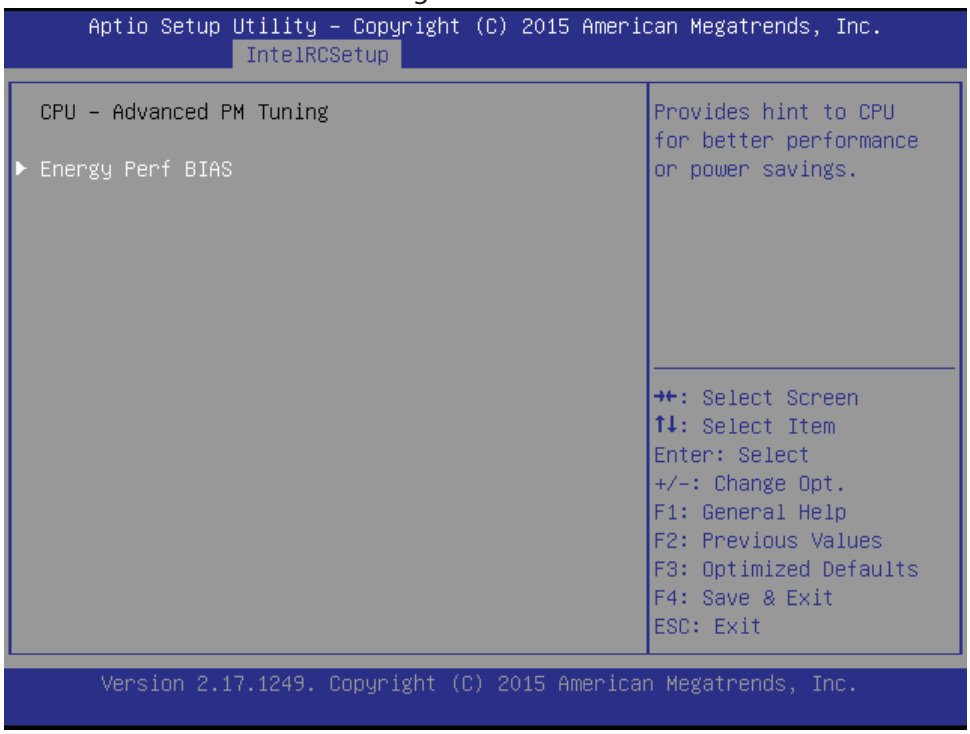
CPU C6 report

Enable/Disable CPU C6(ACPI C2) report to OS Recommended to be enabled.

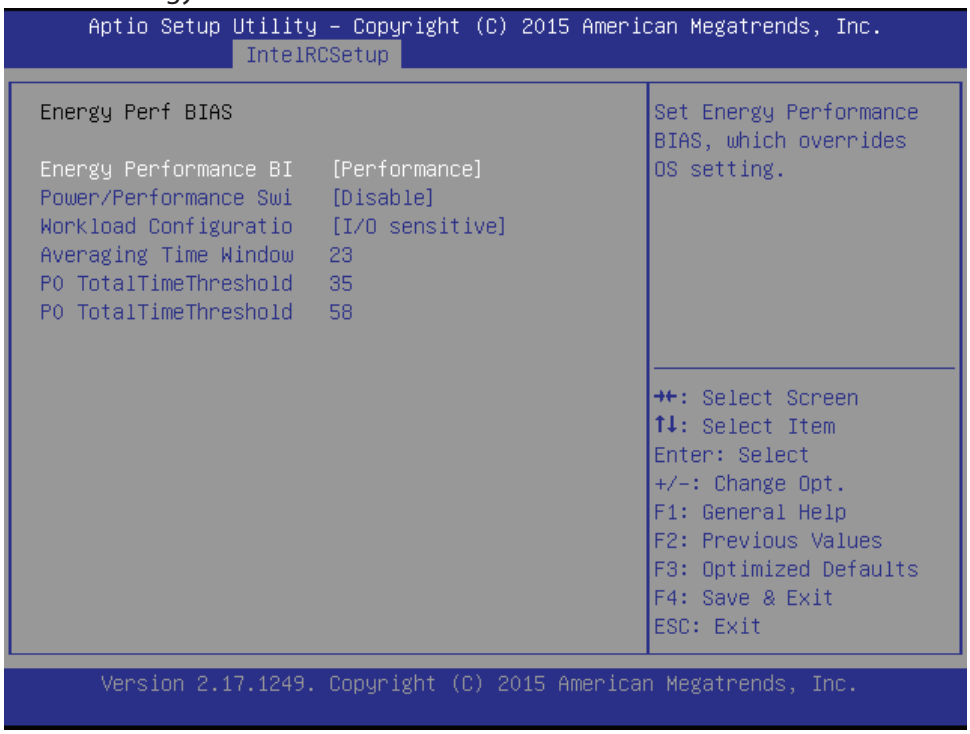
Enhanced halt State

Enables the Enhanced C1E state of the CPU, takes effect after reboot.

4.5.2.3 CPU - Advanced PM Tuning



4.5.2.3.1 Energy Perf BIAS



Energy Performance BI

Set Energy Performance BIAS, which overrides OS setting.

Power/Performance Switch

Enable or Disable Power/Performance Switch

Workload Configuration

Optimization for the workload characterization. Balanced is recommended.

Averaging Time Window

This is used to control the effective window of the average for C0 and P0 time

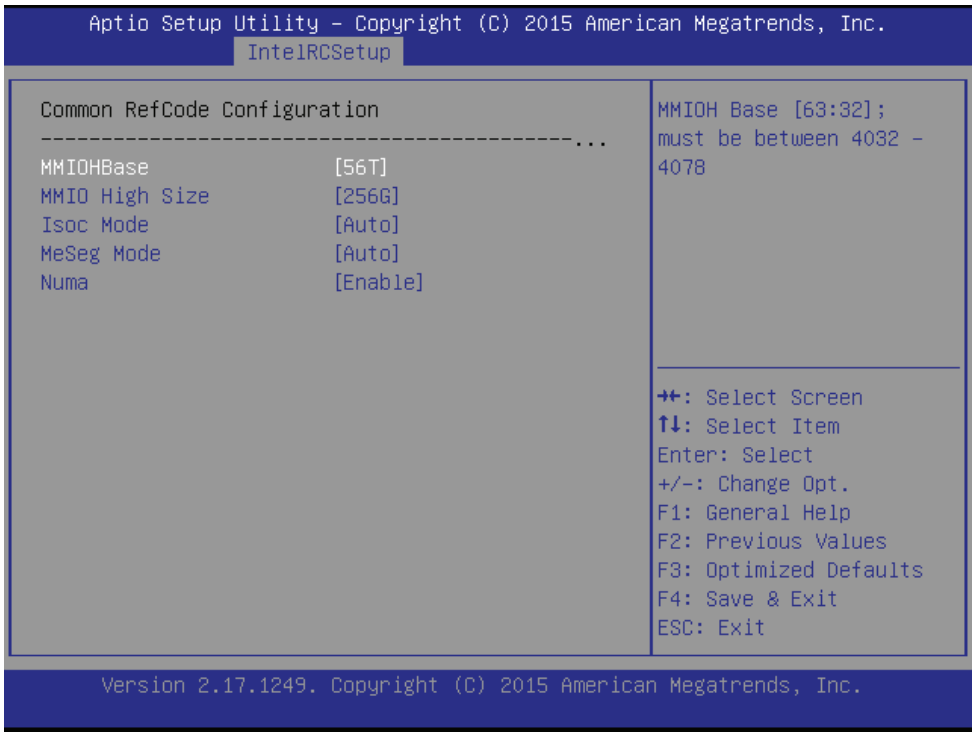
P0 TotalTimeThreshold Low

The HW switching mechanism DISABLES the performance setting (0) when the total P0 time is less than this threshhold

P0 TotalTimeThreshold High

The HW switching mechanism ENABLES the performance setting (0) when the total P0 time is greater than this threshold

4.5.3 Common RefCode Configuration



MMIOHBase

Select MMIO High Base

MMIO High Size

Select MMIO High Size

Isoc Mode

Disable or Enable Isoc Mode.

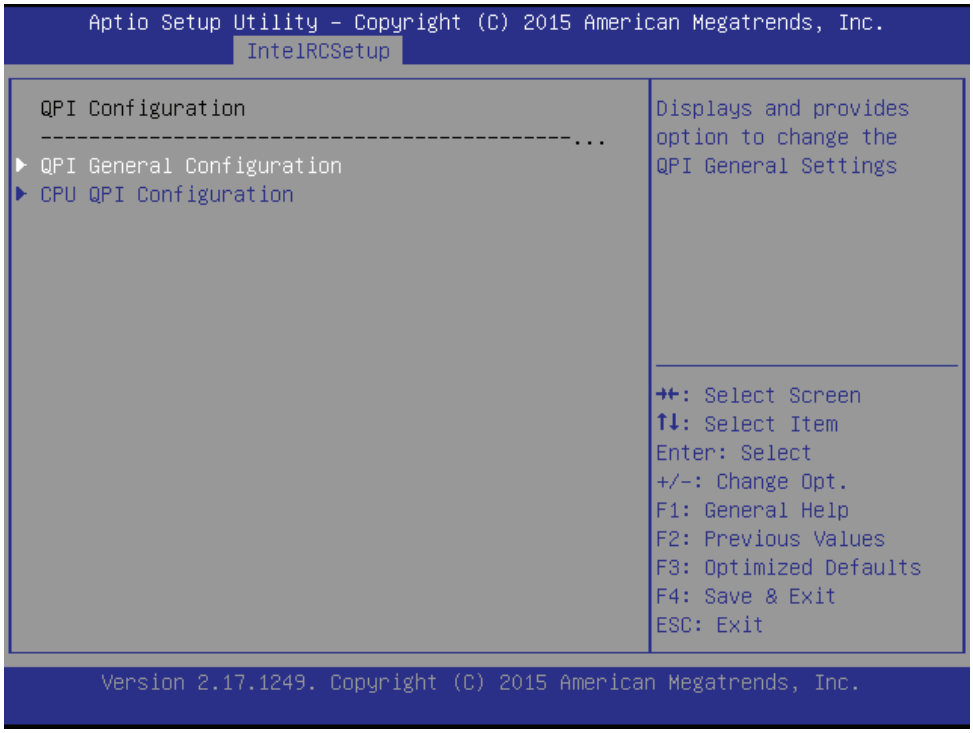
Meseg Mode

Disable or Enable Meseg Mode.

Numa

Enable or Disable Non uniform Memory Access (NUMA).

4.5.4 QPI Configuration



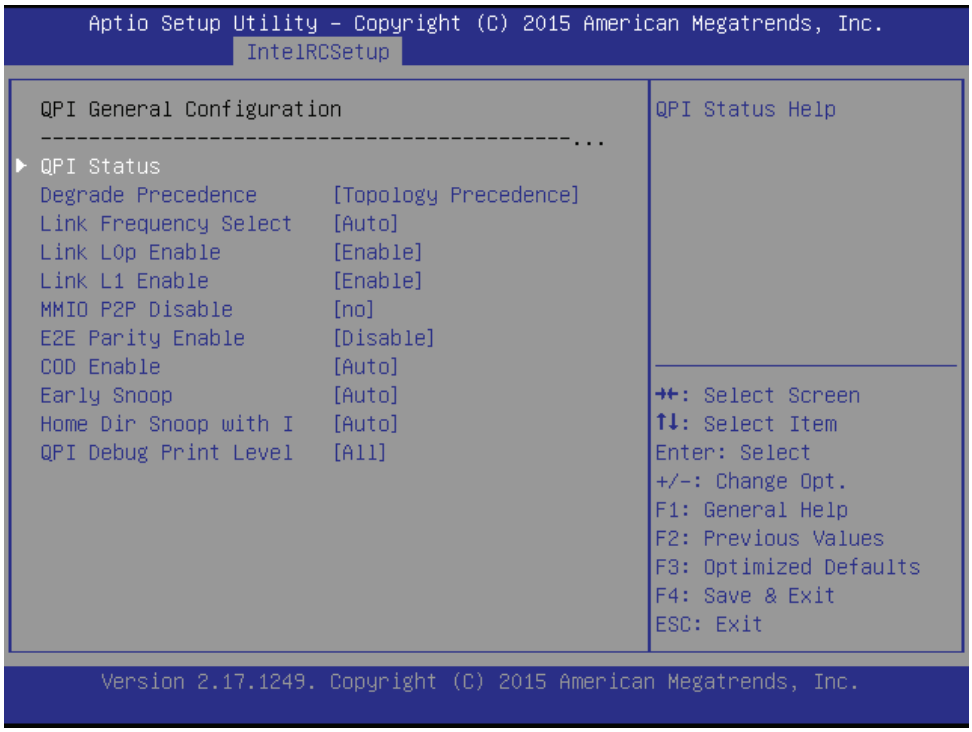
QPI General Configuration

Displays and provides option to change the QPI General Settings

CPU QPI Configuration

QPI Per Socket Configuration

4.5.4.1 QPI General Configuration



QPI Status

QPI Status Help

Degrade Precedence

Choose Topology Precedence to degrade features if system options are in conflict or choose Feature Precedence to degrade topology if system options are in conflict.

Link Frequency Select

Allows for selecting the QPI Link Frequency

Link L0p Enable

Link L0p Enable: Disable, Enable, Auto(default)

Link L1 Enable

Link L1 Enable: Disable, Enable, Auto(default)

MMIO P2P Disable

To disable MMIOL P2P traffic across Sockets. Default is NO to not disable.

COD Enable

Enable/disable Cluster on Die.

Early Snoop

Select Snoop Mode.

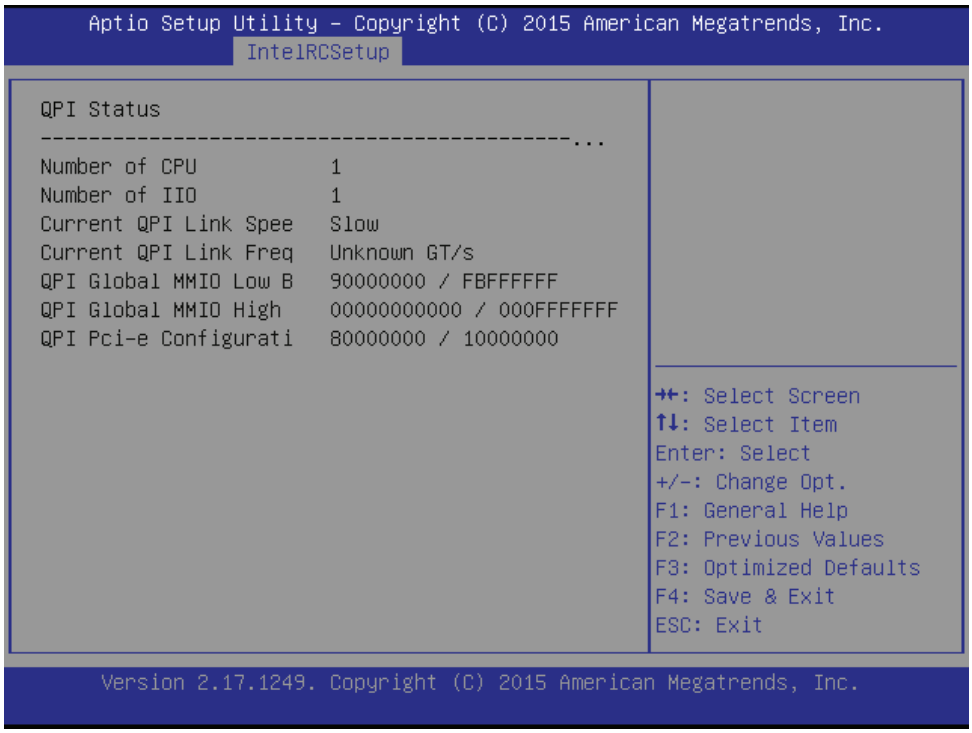
Home Dir Snoop with

Enable/disable Home Dir Snoop with IVT- Style OSB

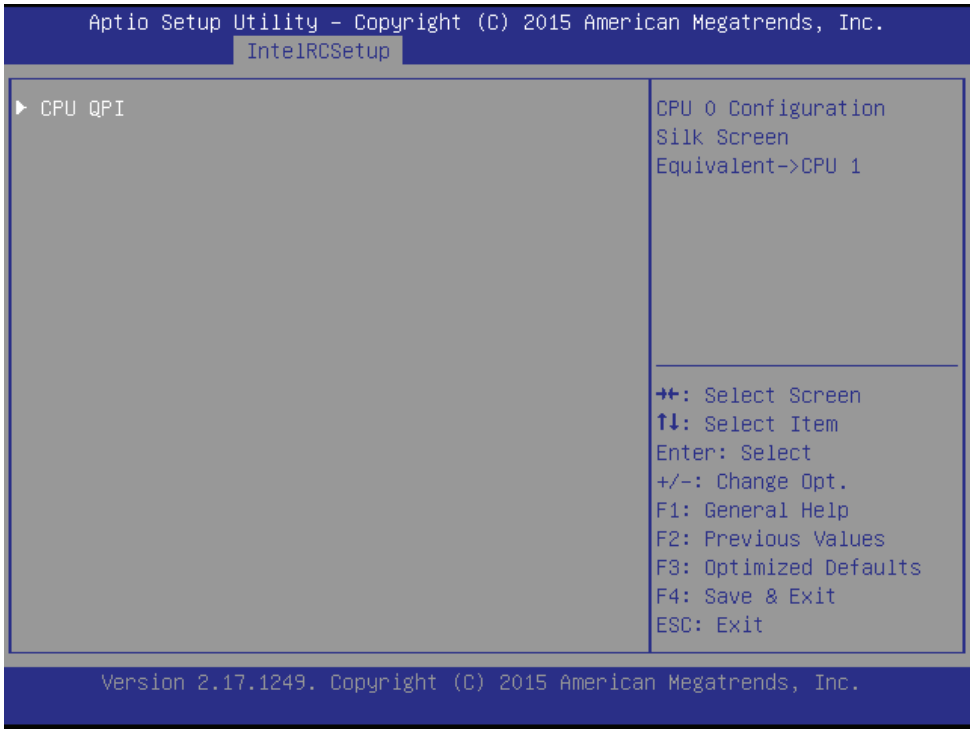
QPI Debug Print Level

QPI Debug Print Level Enable-Disable.

4.5.4.1.1 QPI Status



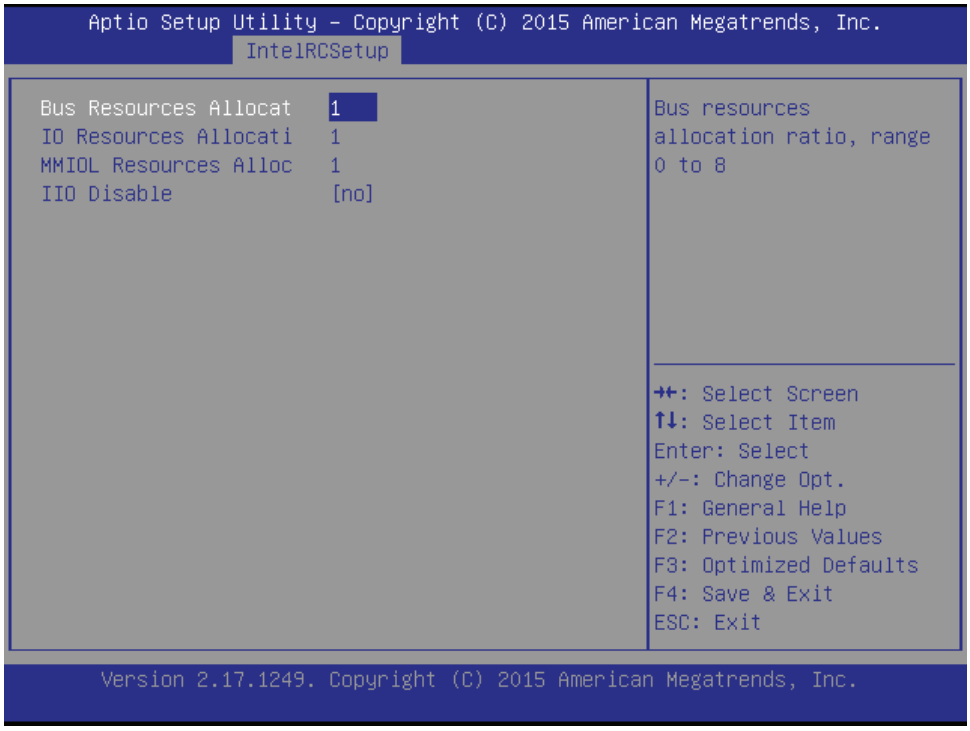
4.5.4.2 CPU QPI Configuration



CPU QPI

QPI Per Socket Configuration

4.5.4.2.1 CPU QPI



Bus Resources Allocation

Bus resources allocation ratio, range 0 to 8

IO Resources Allocation

IO resources allocation ratio, range 0 to 8

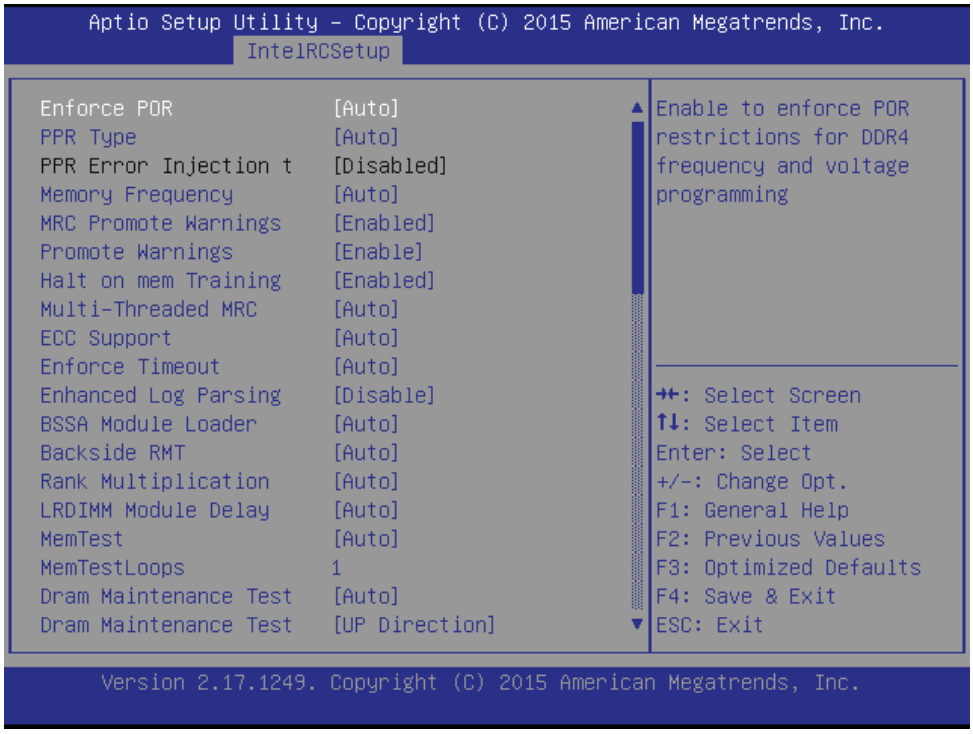
MMIOL Resources Allocation

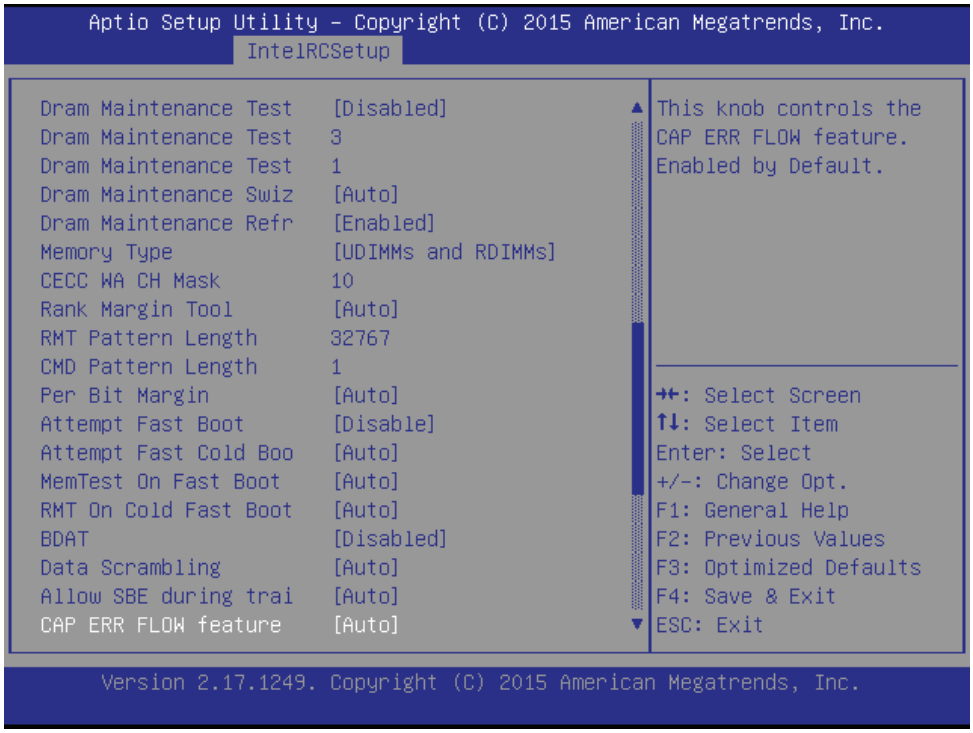
MMIOL resources allocation ratio, range 0 to 8

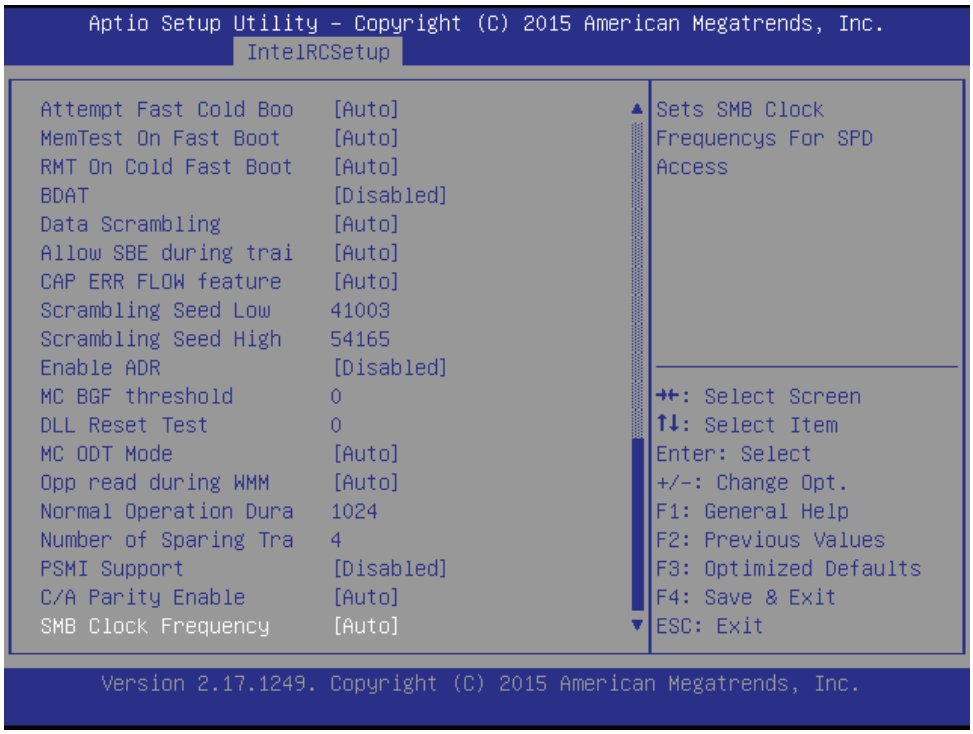
IIO Disable

Disable Ports and Clock Gate IIO

4.5.5 Memory Configuration







Enforce POR

Enable to enforce POR restrictions for frequency and voltage programming

PPR Type

Select PPR Type - Hard / Soft / Disabled

PPR Error Injection

Enable / Disable support for c-script error injection test

Memory Frequency

Maximum Memory Frequency Selections in Mhz. Do not select Reserved

MRC Promote Warnings

Determines if MRC warnings are promoted to system level

Promote Warnings

If enabled RC warnings are promoted to errors (except MRC warnings)

Halt on mem Training

Halt on mem Training Error Disable/Enable

Multi -Threaded MRC

Enable to execute the Memory Reference Code multi-threaded

ECC Support

Enable/disable DDR ECC Support

E n force Timeout

Enable/disable forcing cold reset after three months

Enhanced Log Parsing

Enables additional output in debug log for easier machine parsing

BSSA Module Loader

Enabling BSSA and loading of the test module

Backside RMT

Enable Backside RMT

Rank Multiplication

Force the Rank Multiplication factor for LRDIMM

LRDIMM Module Del ay

When Disabled, MRC will not use SPD bytes 90-95 for LRDIMM Module Delay. When Auto, MRC will boundary check the values and use default values, if SPD is 0 or out of range

Memtest

Enable/disable memory test during normal boot

MemtestLoops

Number of memory test loops during normal boot, set to 0 to run memtest infinitely

Dram Maintenance Test

Dram Maintenance Test during normal boot

Dram Maintenance Test Direction

Dram Maintenance Test Direction UP or DOWN

Dram Maintenance Test Inversion

Dram Maintenance Test Invertion Enable or Disable

Dram Maintenance Test Repetitions

Number of Dram Maintenance Test Repetitions

Dram Maintenance Test Interation on Row

Number of Dram Maintenance Test Interation on Row

Dram Maintenance Swizzling

Dram Maintenance Address Swizzling enable if needed

Dram Maintenance Refresh

Dram Maintenance Test can disable refresh during the test

Memory Type

Selects the Memory type supported by this platform.

CECC WA CH Mask

CH bitmask to apply CECC WA. 1 bit per CH. value 2 applies WA on CH1, 3 on CH0 and 1

Rank Margin Tool

Enables the rank margin tool to run after DDR3 memory training

RMT Pattern Length

Sets the pattern length for the Rank Margin Tool

CMD Pattern Length

Sets the pattern length for the Rank Margin Tool

Per Big Margin

Enables the per bit margining

Attempt Fast Boot

When enabled, portions of memory reference code will be skipped when possible to increase boot speed

Attempt Fast Cold Boot

When enabled, portions of memory reference code will be skipped when possible to increase boot speed

Memtest on Fast Boot

Enable/disable memory test during fast boot

RMT on Cold Fast Boot

Enable/Disable Rank Margin Tool on Cold Fast Boot

BDAT

Enable Disables BDAT

Data Scrambling

Enables data scrambling

Allow SBE during trai

Allow SBE during training knob enable/disable

CAP ERR FlOW Feature

This knob controls the CAP ERR FLOW feature.

Scrambling Seed Low

Low 32 bits of the scrambling seed

Scrambling Seed High

High 32 bits of the scrambling seed

Enable ADR

Enables the detecting and enabling of ADR

MC BGF threshold

The HA to MC BGF threshold is used for scheduling MC request in bypass condition.

DLL Reset Test

Set this to the number of loops to execute the DDL reset test. The test will execute

RMT for the provided number of loops without DLL resets and then it will exectue RMT for the same number of loops with DLL resets.

MC ODT Mode

Select MC ODT Mode

Opp read during WMM

Enable/Disable issuing read commands opportunistically during WMM

Normal Operation Duration

Set normal operation duration interval (0 - 65535)

Number of Sparing Transactions

Set number of sparing transactions interval (0 - 65535)

PSMI Support

PSMI Support Disable/Enable

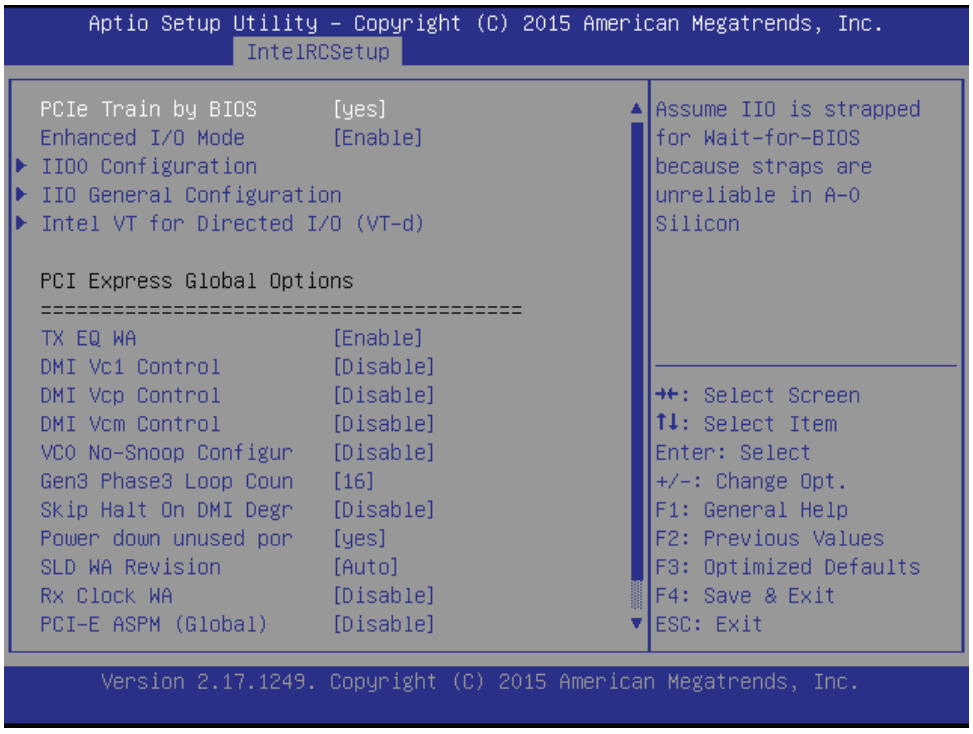
C/A Parity Enable

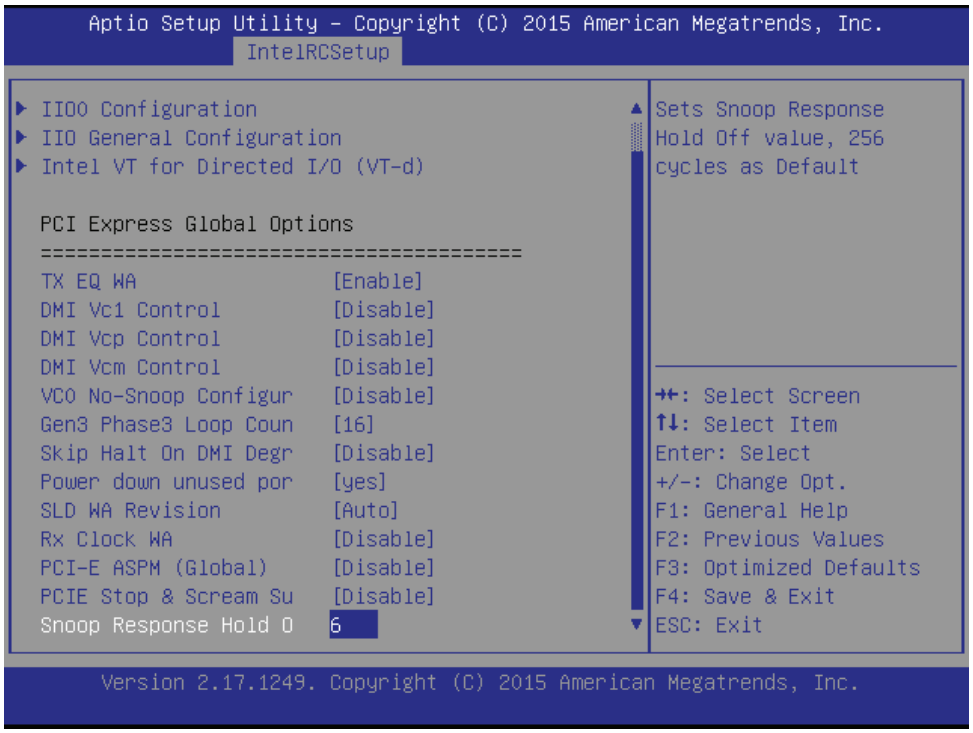
Enable/Disable Command Address Parity

SMB Clock Frequency

Sets SMB Clock Frequencys For SPD Access

4.5.6 IIO Configuration





PCIe Train by BIOS

Assume IIO is strapped for Wait-for-BIOS because straps are unreliable in A-0 Silicon

Enhanced I/O Mode

Enhanced I/O Mode

TX EQ WA

Use special table for TX_EQ and vendor specific cards

DMI Vc1 Control

Enable/Disable DMI Vc1

DMI Vcp Control

Enable/Disable DMI Vcp

DMI Vcm Control

Enable/Disable DMI Vcm

VC0 No-Snoop Configuration

Enables No-Snoop on reads and writes for Vc0 traffic.

Gen3 Phase3 Loop Count

Gen3 Phase3 Loop Count: 1, 4, 16, 256

Skip Halt On DMI Degradation

Enable this option to avoid the system to be halted on DMI width/link degradation

Power down unused ports

Power down unused ports. Yes or no.

SLD WA Revision

SLD WA Revision

Rx Clock WA

Rx Clock WA

PCI-E ASPM (Global)

This option enables / disables the ASPM control for all downstream devices.

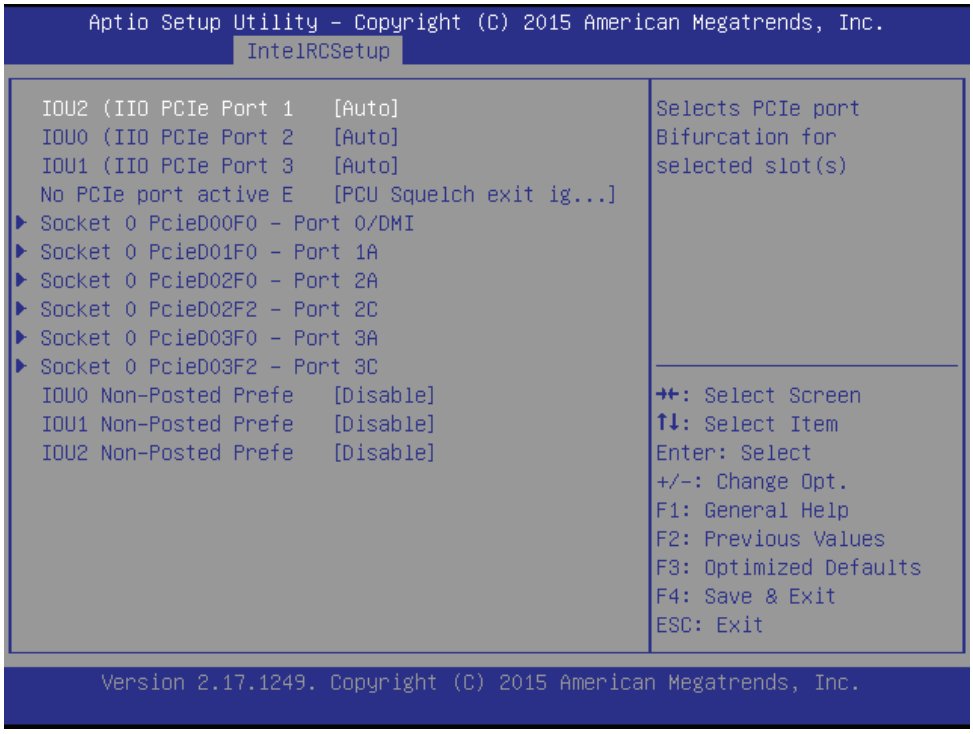
PCIE Stop & Scream Support

This option enables / disables PCIE Stop & Scream Support

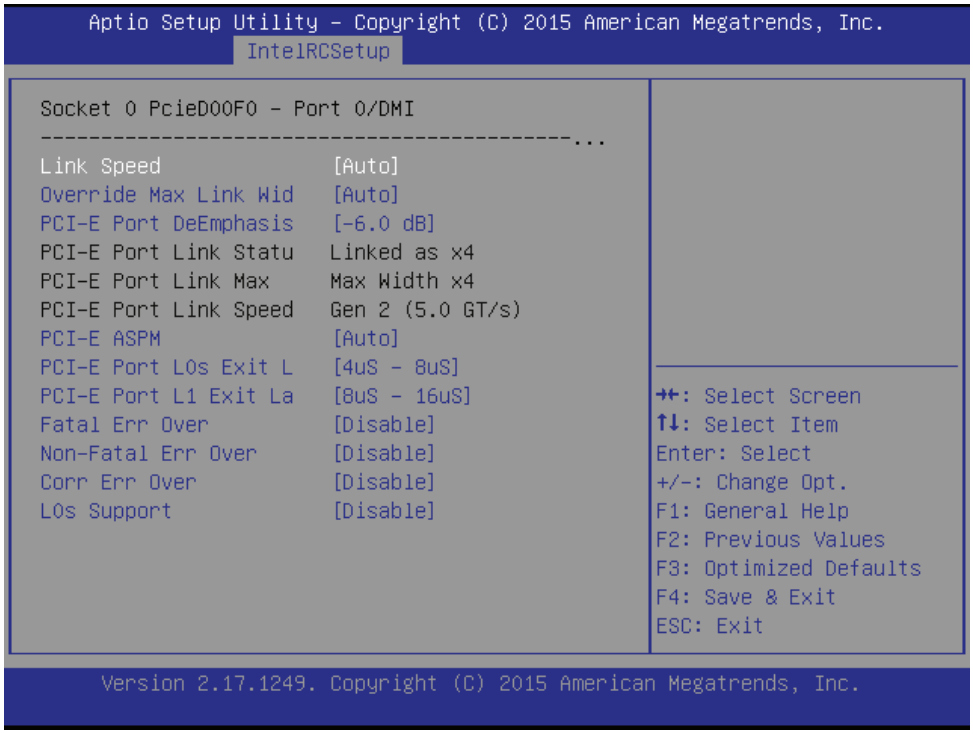
Snoop Response Hold

Sets Snoop Response Hold Off value, 256 cycles as Default

4.5.6.1 IIO Configuration



4.5.6.1.1 Socket 0 PcieD00F0 - Port 0/DMI



Link Speed

If supported by hardware and set to 'Force to 2.5GT/s' for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used.

Override Max Link Wid

Override the max link width that was set by bifurcation

PCI-E Port DeEmphasis

De-Emphasis control (LNKCON2[6]) for this PCIe port.

PCI-E ASPM

This option enables /disables the ASPM(L1) for the downstream devices.

PCI-E Port L0s Exit Latency

The length of time this port requires to complete transition from L0s to L0

PCI-E Port L1 Exit Latency

The length of time this port requires to complete transition from L1 to L0

Fatal Err Over

Enables forcing non-fatal error propogation to the IIO core error logic for this port

Non-Fatal Err Over

Enables forcing non-fatal error propogation to the IIO core error logic for this port

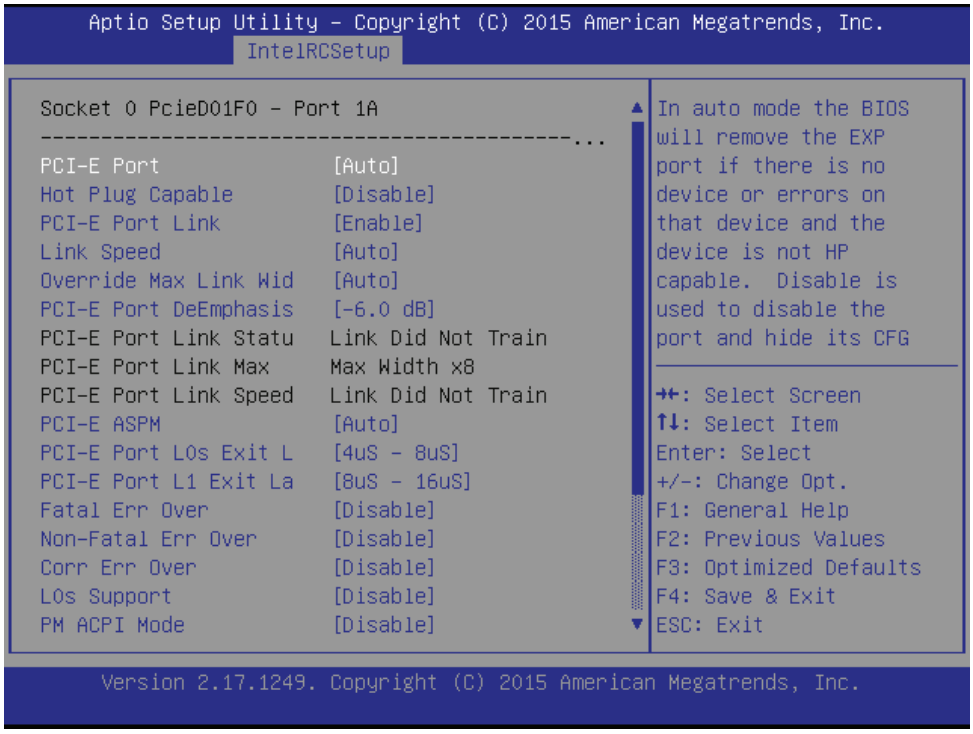
Corr Err Over

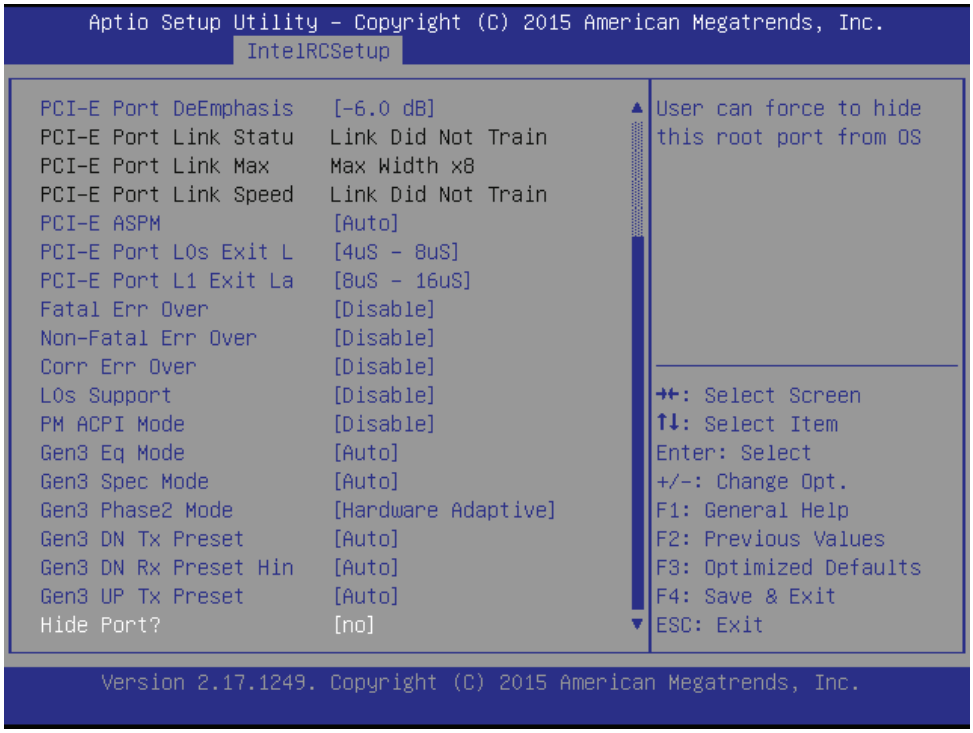
Enables forcing correctable error propogation to the IIO core error logic for this port

L0s Support

When disabled, IIO never puts its transmitter in L0s state

4.5.6.1.2 Socket 0 PcieD01F0 - Port 1A





Hot Plug Capable

This option specifies if the link is considered Hot Plug capable.

PCI - E Port Link

This option disables the link so that the no training occurs but the CFG space is still active.

Link Speed

If supported by hardware and set to 'Force to 2.5 GT/s' for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used.

Override Max Link Wid

Override the max link width that was set by bifurcation

PCI - E Port DeEmphasis

De-Emphasis control (LNKCON2[6]) for this PCIe port.

PCI - E ASPM

This option enables / disables the ASPM(L1) for the downstream devices.

PCI - E Port L0s Exit Latency

The length of time this port requires to complete transition from LOs to LO

PCI - E Port L1 Exit Latency

The length of time this port requires to complete transition from L1 to LO

Fatal Err Over

Enables forcing non-fatal error propogation to the IIO core error logic for this port

Non - Fatal Err Over

Enables forcing non-fatal error propogation to the IIO core error logic for this port

Corr Err Over

Enables forcing correctable error propogation to the IIO core error logic for this port

L0s Support

When disabled, IIO never puts its transmitter in LOs state

PM ACPI Mode

When Disabled, MSI is generated on PMevent. When Enabled, _HPGPE message is generated

Gen3 Eq Mode

PCIe Gen3 Adaptive Equilization Mode

Gen3 Spec Mode

PCIe Gen3 Spec Mode

Gen3 DN Tx Preset

PCIe Gen3 Downstream Tx Preset

Gen3 DN Rx Preset Hint

PCIe Gen3 Downstream Rx Preset Hint

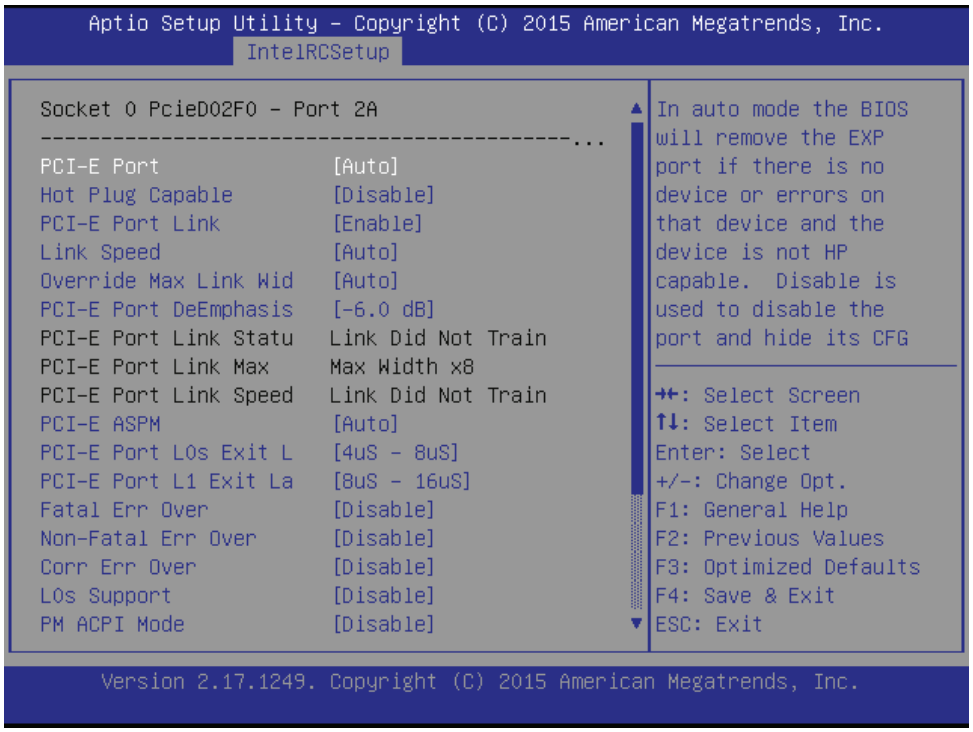
Gen3 UP Tx Preset

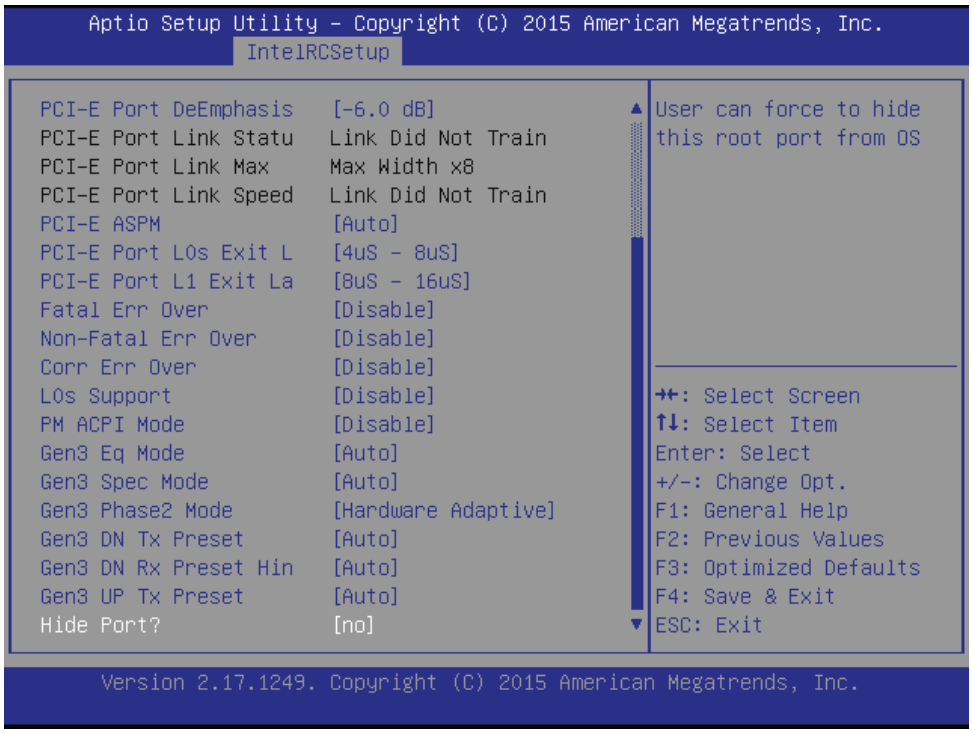
PCIe Gen3 Upstream Tx Preset

Hide Port?

User can force to hide this root port from OS

4.5.6.1.3 Socket 0 PcieD02F0 - Port 2A





Hot Plug Capable

This option specifies if the link is considered Hot Plug capable.

PCI - E Port Link

This option disables the link so that the no training occurs but the CFG space is still active.

Link Speed

If supported by hardware and set to 'Force to 2.5 GT/s' for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used.

Override Max Link Wid

Override the max link width that was set by bifurcation

PCI - E Port DeEmphasis

De-Emphasis control (LNKCON2[6]) for this PCIe port.

PCI - E ASPM

This option enables / disables the ASPM(L1) for the downstream devices.

PCI - E Port L0s Exit Latency

The length of time this port requires to complete transition from L0s to L0

PCI - E Port L1 Exit Latency

The length of time this port requires to complete transition from L1 to LO

Fatal Err Over

Enables forcing non-fatal error propogation to the IIO core error logic for this port

Non - Fatal Err Over

Enables forcing non-fatal error propogation to the IIO core error logic for this port

Corr Err Over

Enables forcing correctable error propogation to the IIO core error logic for this port

L0s Support

When disabled, IIO never puts its transmitter in LOs state

PM ACPI Mode

When Disabled, MSI is generated on PMevent. When Enabled, _HPGPE message is generated

Gen3 Eq Mode

PCIe Gen3 Adaptive Equilization Mode

Gen3 Spec Mode

PCIe Gen3 Spec Mode

Gen3 DN Tx Preset

PCIe Gen3 Downstream Tx Preset

Gen3 DN Rx Preset Hint

PCIe Gen3 Downstream Rx Preset Hint

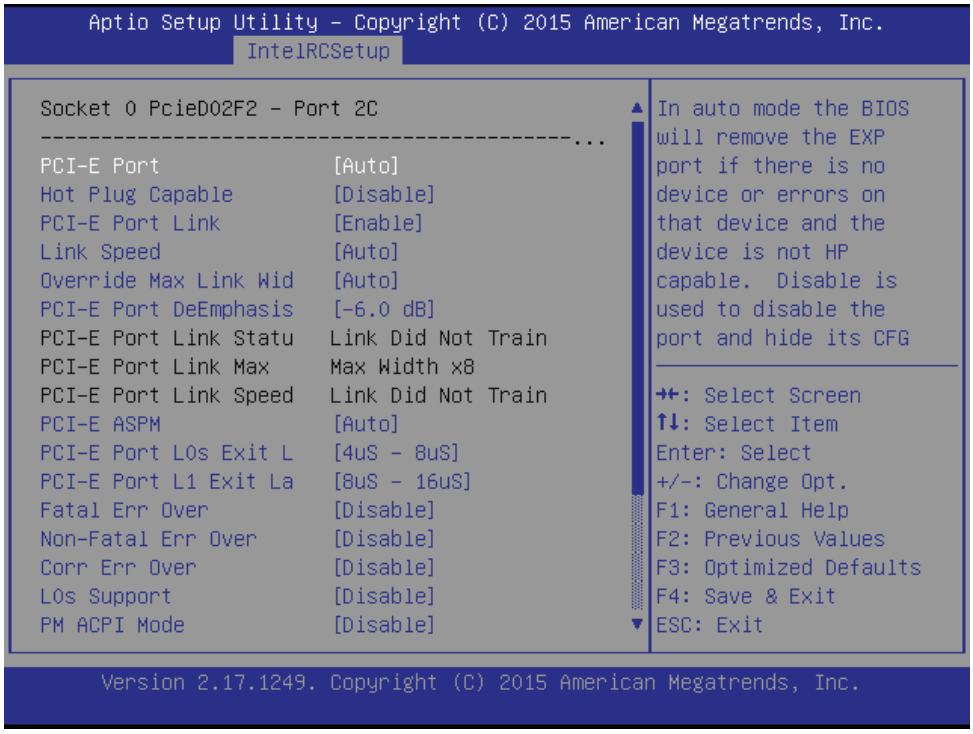
Gen3 UP Tx Preset

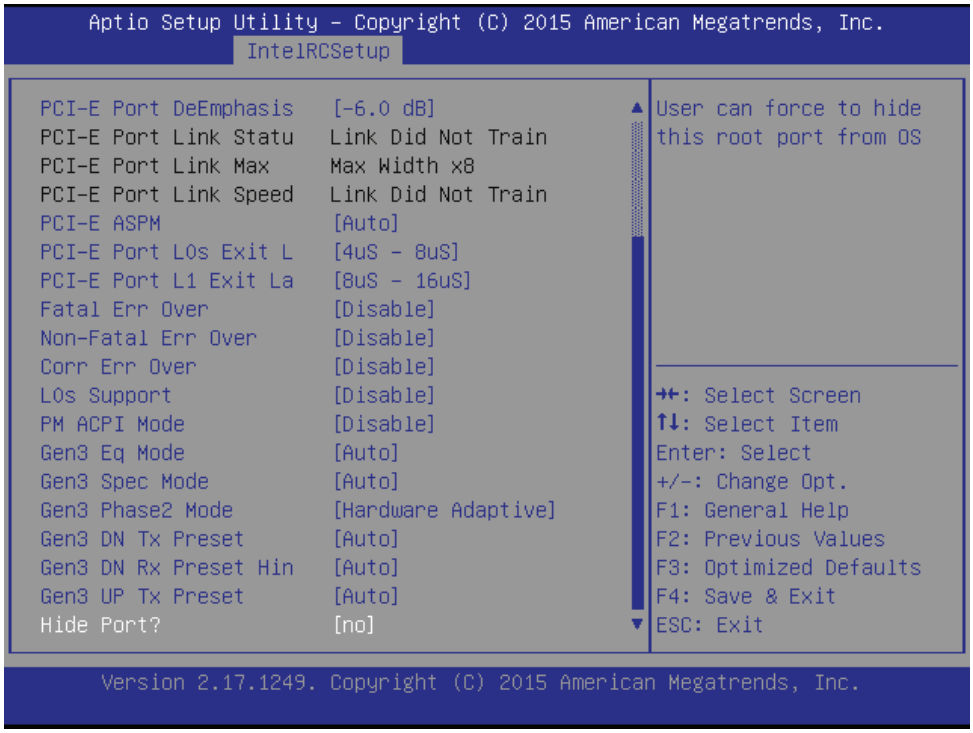
PCIe Gen3 Upstream Tx Preset

Hide Port?

User can force to hide this root port from OS

4.5.6.1.4 Socket 0 PcieD02F2 - Port 2C





Hot Plug Capable

This option specifies if the link is considered Hot Plug capable.

PCI - E Port Link

This option disables the link so that the no training occurs but the CFG space is still active.

Link Speed

If supported by hardware and set to 'Force to 2.5 GT/s' for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used.

Override Max Link Wid

Override the max link width that was set by bifurcation

PCI - E Port DeEmphasis

De-Emphasis control (LNKCON2[6]) for this PCIe port.

PCI - E ASPM

This option enables / disables the ASPM(L1) for the downstream devices.

PCI - E Port L0s Exit Latency

The length of time this port requires to complete transition from LOs to LO

PCI - E Port L1 Exit Latency

The length of time this port requires to complete transition from L1 to LO

Fatal Err Over

Enables forcing non-fatal error propogation to the IIO core error logic for this port

Non - Fatal Err Over

Enables forcing non-fatal error propogation to the IIO core error logic for this port

Corr Err Over

Enables forcing correctable error propogation to the IIO core error logic for this port

L0s Support

When disabled, IIO never puts its transmitter in LOs state

PM ACPI Mode

When Disabled, MSI is generated on PMevent. When Enabled, _HPGPE message is generated

Gen3 Eq Mode

PCIe Gen3 Adaptive Equilization Mode

Gen3 Spec Mode

PCIe Gen3 Spec Mode

Gen3 Phase2 Mode

Gen3 Phase2 Mode

Gen3 DN Tx Preset

PCIe Gen3 Downstream Tx Preset

Gen3 DN Rx Preset Hint

PCIe Gen3 Downstream Rx Preset Hint

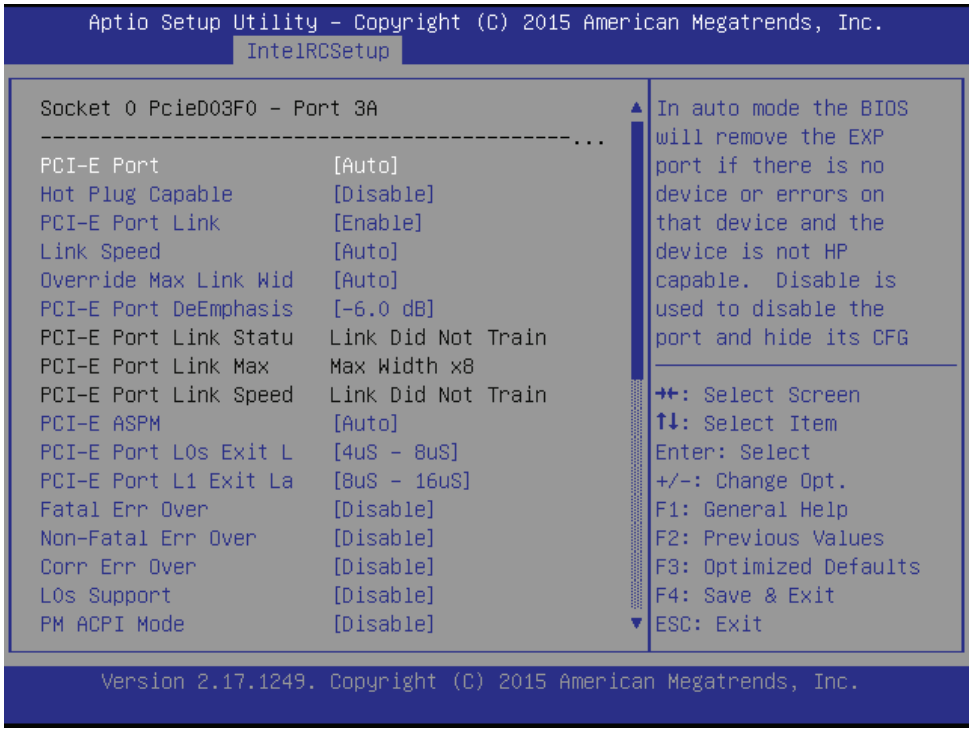
Gen3 UP Tx Preset

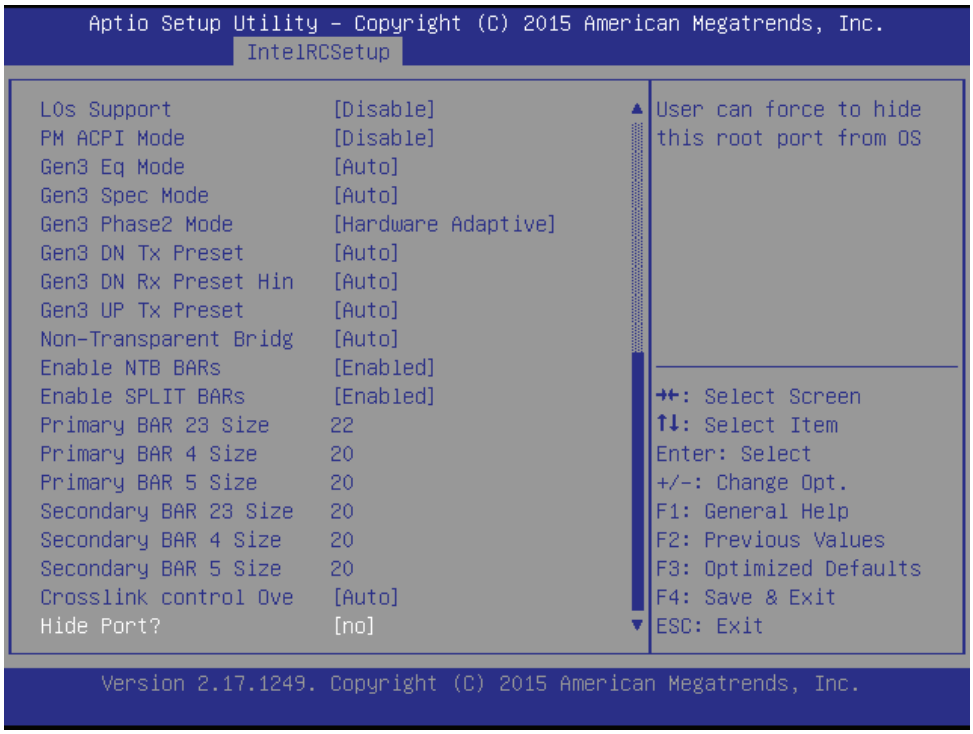
PCIe Gen3 Upstream Tx Preset

Hide Port?

User can force to hide this root port from OS

4.5.6.1.5 Socket 0 PcieD03F0 - Port 3A





Hot Plug Capable

This option specifies if the link is considered Hot Plug capable.

PCI - E Port Link

This option disables the link so that the no training occurs but the CFG space is still active.

Link Speed

If supported by hardware and set to 'Force to 2.5 GT/s' for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used.

Override Max Link Wid

Override the max link width that was set by bifurcation

PCI - E Port D eEmphasis

De-Emphasis control (LNKCON2[6]) for this PCIe port.

PCI - E ASPM

This option enables / disables the ASPM(L1) for the downstream devices.

PCI - E Port L0s Exit Latency

The length of time this port requires to complete transition from L0s to L0

PCI - E Port L1 Exit Latency

The length of time this port requires to complete transition from L1 to LO

Fatal Err Over

Enables forcing non-fatal error propogation to the IIO core error logic for this port

Non - Fatal Err Over

Enables forcing non-fatal error propogation to the IIO core error logic for this port

Corr Err Over

Enables forcing correctable error propogation to the IIO core error logic for this port

L0s Support

When disabled, IIO never puts its transmitter in LOs state

PM ACPI Mode

When Disabled, MSI is generated on PMevent. When Enabled, _HPGPE message is generated

Gen3 Eq Mode

PCIe Gen3 Adaptive Equilization Mode

Gen3 Spec Mode

PCIe Gen3 Spec Mode

Gen3 Phase2 Mode

Gen3 Phase2 Mode

Gen3 DN Tx Preset

PCIe Gen3 Downstream Tx Preset

Gen3 DN Rx Preset Hint

PCIe Gen3 Downstream Rx Preset Hint

Gen3 UP Tx Preset

PCIe Gen3 Upstream Tx Preset

Non - Transparent Bridge

Configures port as TB, NTB-NTB, or NTB-RP (DON'T SELECT NTB-RP for legacy IIO on AO Si!). On platforms that support NTB, Auto is NTB-NTB.

Enable NTB BARs

If disabled, BIOS will not program NTB BAR size registers

Enable SPLIT BARs

If Enabled, will use two 32 bit BARs instead of 64 bit BAR

Primary BAR 23 Size

Used to set the prefetchable BAR 23 size on primary side of NTB. Value < than 12 or > 29 (39 for BIOS supporting > 4G PCI) disables BAR.

Primary BAR 4 Size

Used to set the prefetchable BAR 4 size on primary side of NTB. Value < than 12 or

> 29 (39 for BIOS supporting > 4G PCI) disables BAR.

Primary BAR 5 Size

Used to set the prefetchable BAR 5 size on primary side of NTB. Value < than 12 or > 29 (39 for BIOS supporting > 4G PCI) disables BAR.

Secondary BAR 23 Size

Used to set the prefetchable BAR 23 size on secondary side of NTB. Value < than 12 or > 39 disables BAR.

Secondary BAR 4 Size

Used to set the prefetchable BAR 4 size on Secondary side of NTB. Value < than 12 or > 29 (39 for BIOS supporting > 4G PCI) disables BAR.

Secondary BAR 5 Size

Used to set the prefetchable BAR 5 size on Secondary side of NTB. Value < than 12 or > 29 (39 for BIOS supporting > 4G PCI) disables BAR.

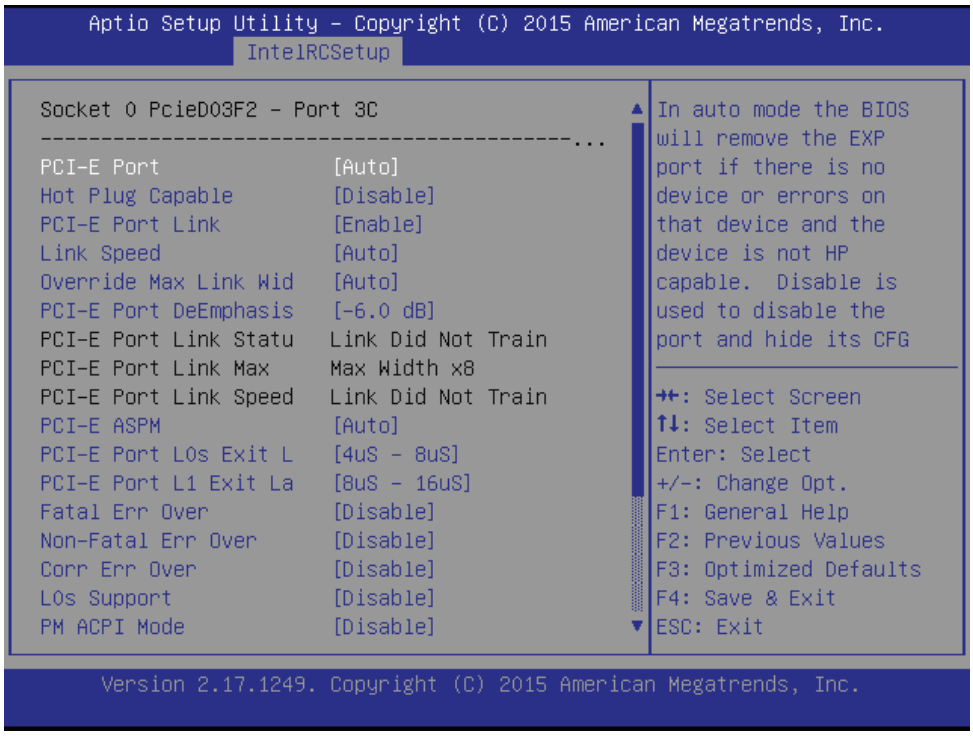
Crosslink control Ove

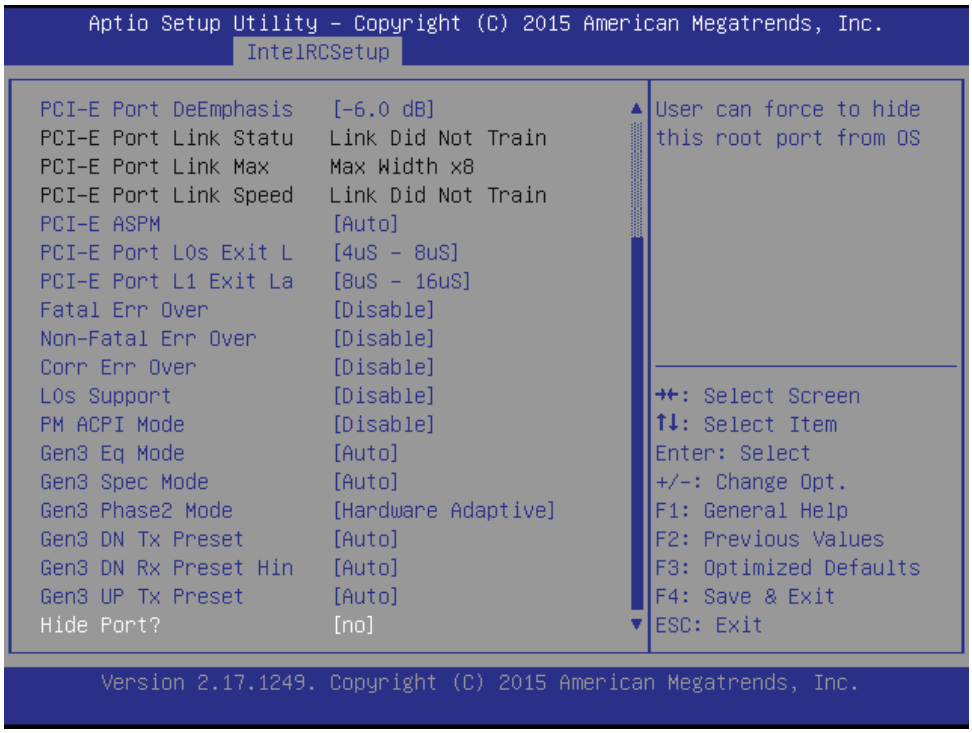
Configure NTB port as DSP/USP, USD/DSP, or use external pin

Hide Port?

User can force to hide this root port from OS

4.5.6.1.6 Socket 0 PcieD03F2 - Port 3C





Hot Plug Capable

This option specifies if the link is considered Hot Plug capable.

PCI - E Port Link

This option disables the link so that the no training occurs but the CFG space is still active.

Link Speed

If supported by hardware and set to 'Force to 2.5 GT/s' for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used.

Override Max Link Wid

Override the max link width that was set by bifurcation

PCI - E Port DeEmphasis

De-Emphasis control (LNKCON2[6]) for this PCIe port.

PCI - E ASPM

This option enables / disables the ASPM(L1) for the downstream devices.

PCI - E Port L0s Exit Latency

The length of time this port requires to complete transition from LOs to LO

PCI - E Port L1 Exit Latency

The length of time this port requires to complete transition from L1 to LO

Fatal Err Over

Enables forcing non-fatal error propogation to the IIO core error logic for this port

Non - Fatal Err Over

Enables forcing non-fatal error propogation to the IIO core error logic for this port

Corr Err Over

Enables forcing correctable error propogation to the IIO core error logic for this port

L0s Support

When disabled, IIO never puts its transmitter in LOs state

PM ACPI Mode

When Disabled, MSI is generated on PMevent. When Enabled, _HPGPE message is generated

Gen3 Eq Mode

PCIe Gen3 Adaptive Equilization Mode

Gen3 Spec Mode

PCIe Gen3 Spec Mode

Gen3 Phase2 Mode

Gen3 Phase2 Mode

Gen3 DN Tx Preset

PCIe Gen3 Downstream Tx Preset

Gen3 DN Rx Preset Hint

PCIe Gen3 Downstream Rx Preset Hint

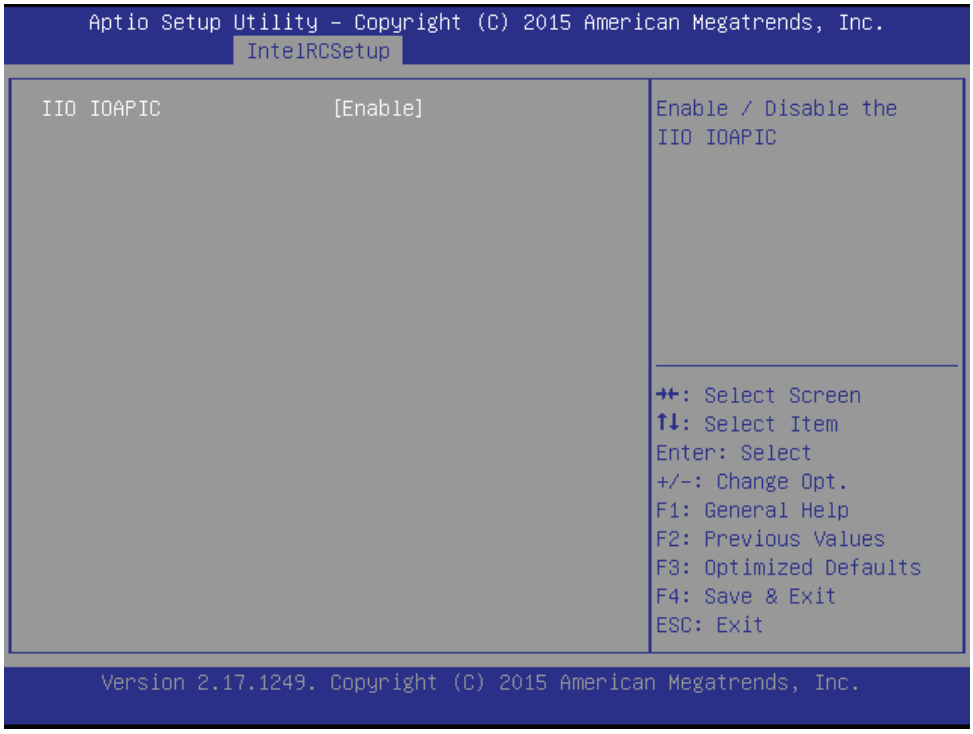
Gen3 UP Tx Preset

PCIe Gen3 Upstream Tx Preset

Hide Port?

User can force to hide this root port from OS

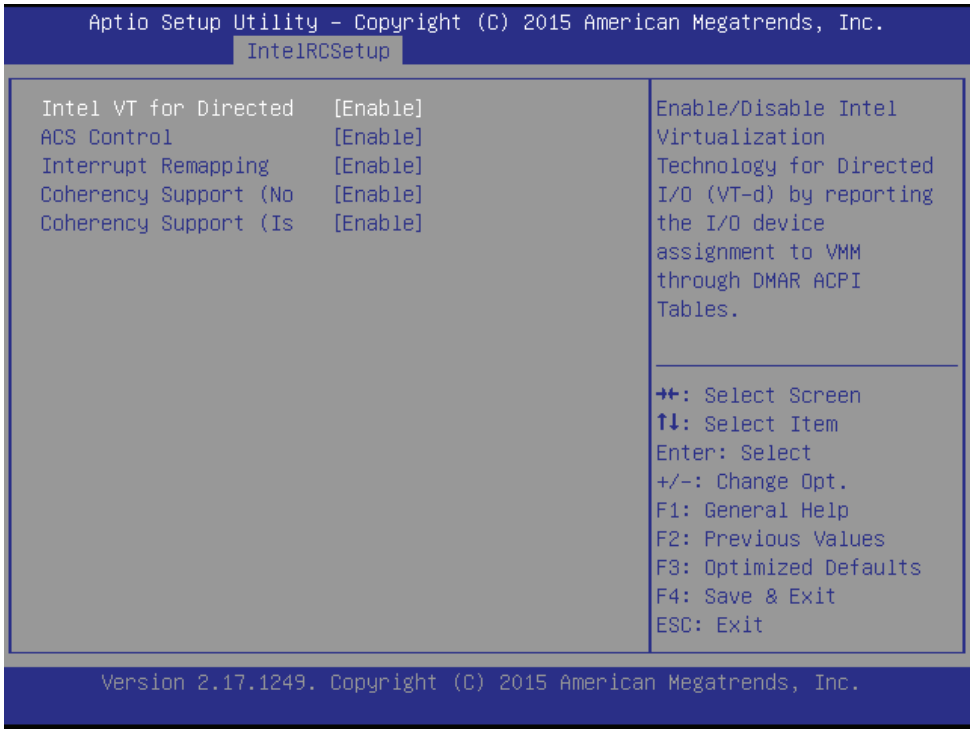
4.5.6.2 IIO General Configuration



IIO IOAPIC

Enable / Disable the IIO IOAPIC

4.5.6.3 Intel VT for Directed I/O (VT-d)



Intel VT for Directed

Enable/Disable Intel Virtualization Technology for Directed I/O (VT-d) by reporting the I/O device assignment to VMM through DMAR ACPI Tables.

ACS Control

Enable: Programs ACS only to Chipset Pcie Root Ports Bridges; Disable: Programs ACS to all Pcie bridges

Interrupt Remapping

Enable/Disable VT_D Interrupt Remapping Support

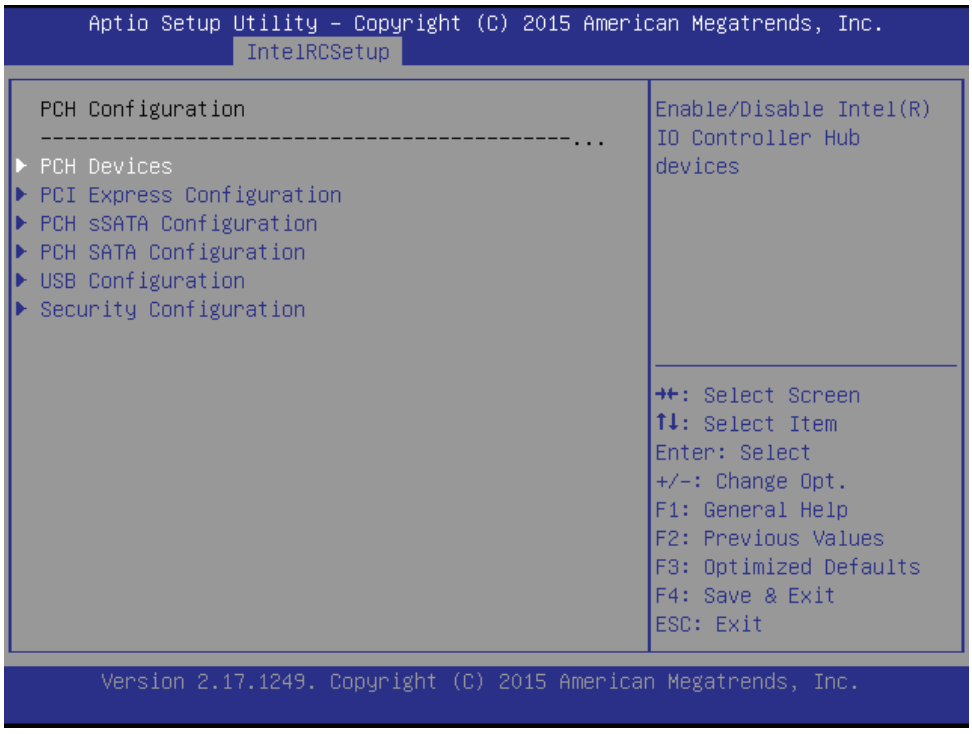
Coherency (Non-Isoch)

Enable/Disable Non-Isoch VT_D Engine Coherency support

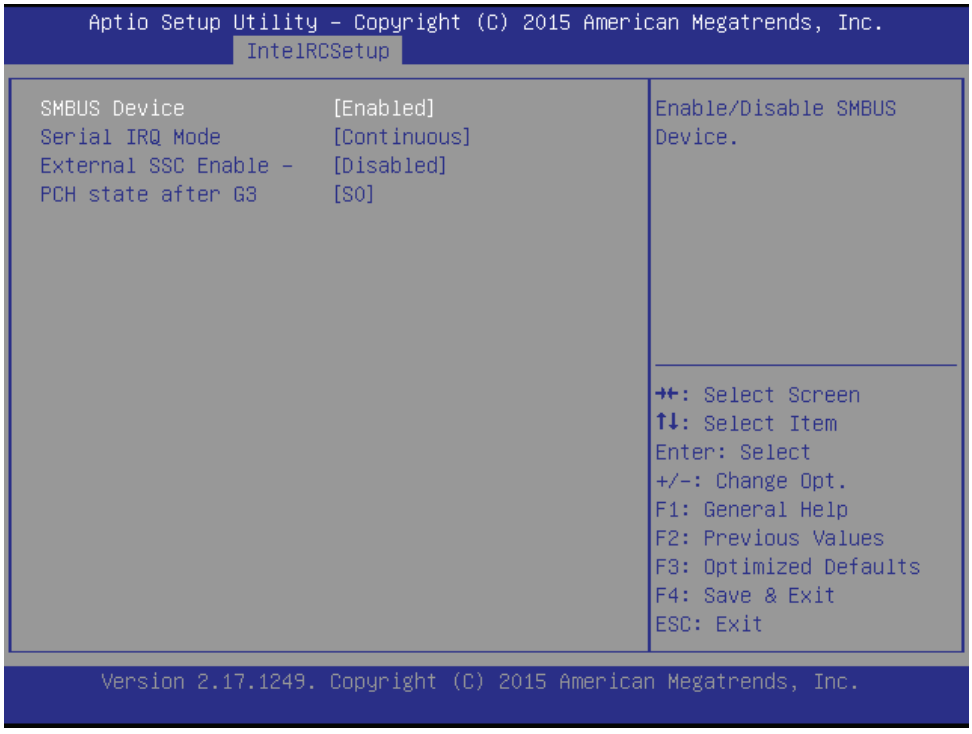
Coherency (Isoch)

Enable/Disable Isoch VT_D Engine Coherency support

4.5.7 PCH Configuration



4.5.7.1 PCH Devices



SMBUS Device

Enable/Disable SMBUS Device.

Serial IRQ Mode

Configure Serial IRQ Mode.

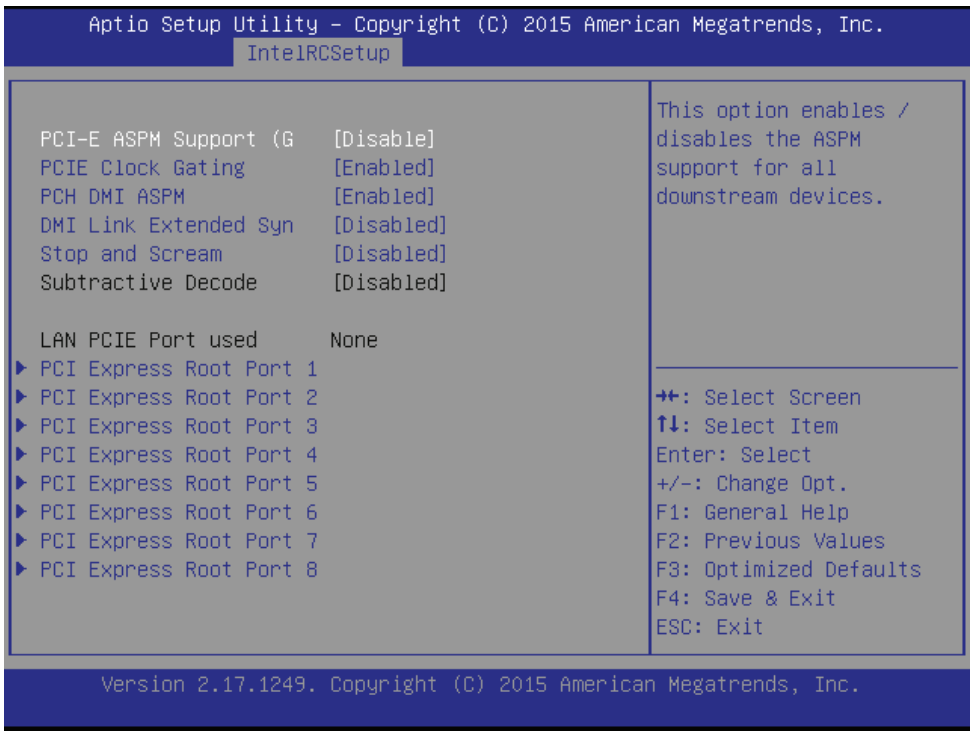
External SSC Enable

Enable Spread Spectrum - only affects external clock generator

PCH State after G3

Select SO/S5 for ACPI state after a G3

4.5.7.2 PCI Express Configuration



PCI - E ASPM Support

This option enables / disables the ASPM support for all downstream devices.

PCIE Clock Gating

PCIE Clock Gating Enable/Disable for all PCH PCIE Ports.

PCH DMI ASPM

PCH DMI ASPM Setting

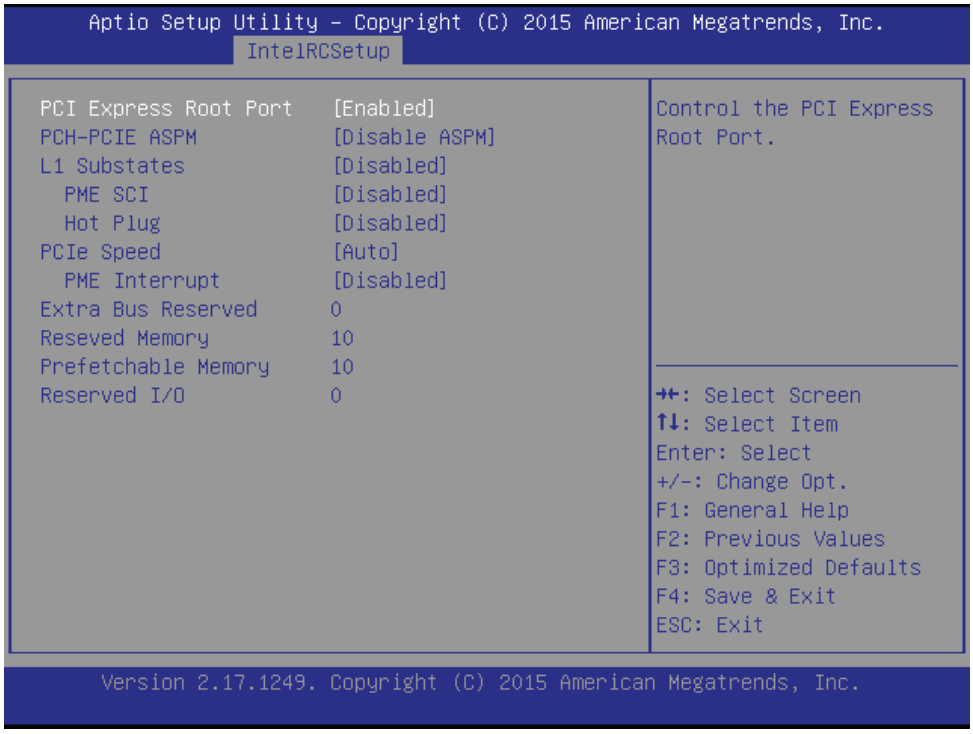
DMI Link Extended Synch

The control of Extended Synch on SB side of the DMI Link.

Stop and Scream

When Enabled DS packets on DMI with the EP bit set, will have their UT bit set

4.5.7.2.1 PCI Express Root Port 1



PCI Express Root Port

Control the PCI Express Root Port.

PCH - PCIE ASPM

PCI Express Root port ASPM Setting

L1 Substates

PCI Express L1 Substates settings.

PME SCI

PCI Express PME SCI Enable/Disable.

Hot Plug

Designates this port as Hot Pluggable.

PCIe Speed

Configure PCIe Speed

PME Interrupt

PCI Express PME Interrupt Enable/Disable.

Extra Bus Reserved

Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

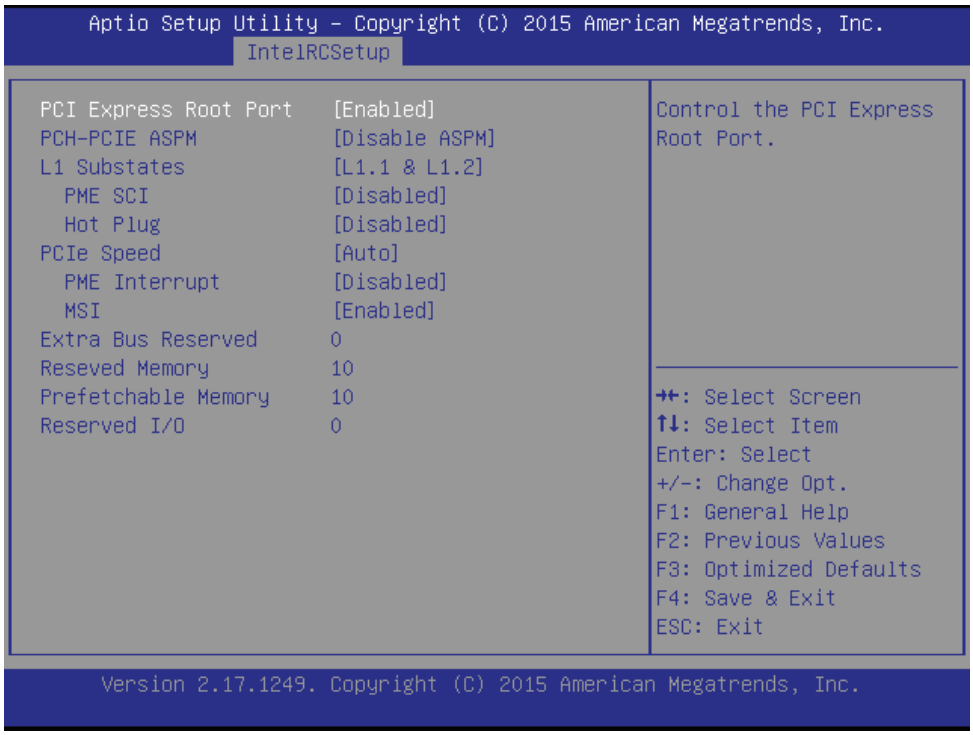
Reserved Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

Reserve d I/O

Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.

4.5.7.2.2 PCI Express Root Port 2



PCI Express Root Port

Control the PCI Express Root Port.

PCH - PCIE ASPM

PCI Express Root port ASPM Setting

L1 Substates

PCI Express L1 Substates settings.

PME SCI

PCI Express PME SCI Enable/Disable.

Hot Plug

Designates this port as Hot Pluggable.

PCIe Speed

Configure PCI e Speed

PME Interrupt

PCI Express PME Interrupt Enable/Disable.

MSI

PCI E MSI Enable/Disable.

Extra Bus Reserved

Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

Reserved Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

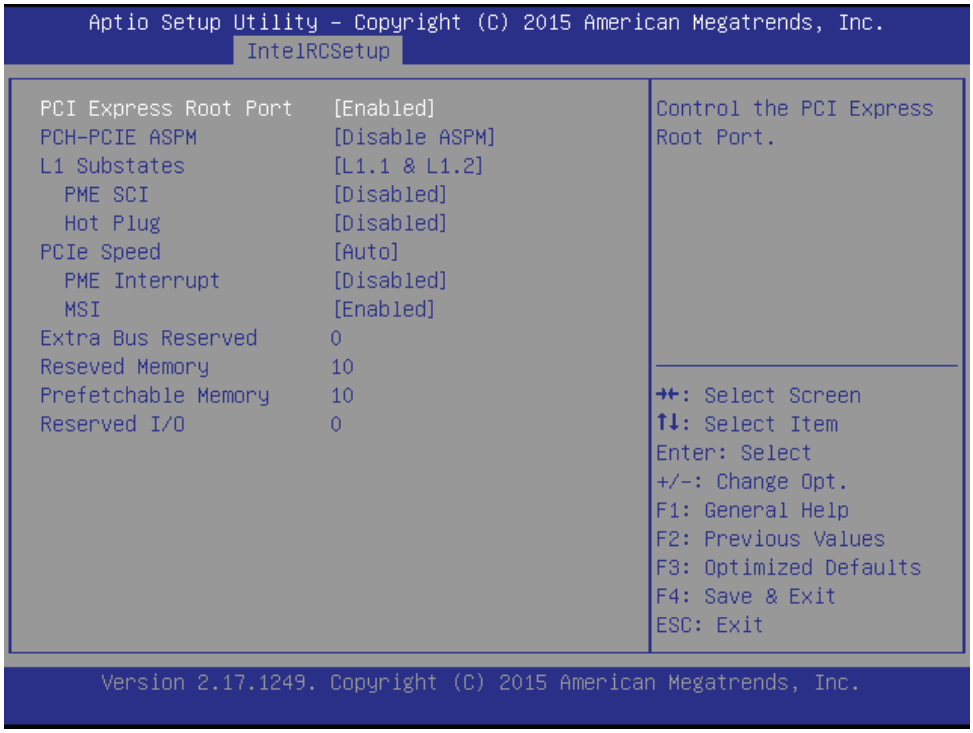
Prefetchable Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

Reserved I/O

Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.

4.5.7.2.3 PCI Express Root Port 3



PCI Express Root Port

Control the PCI Express Root Port.

PCH - PCIE ASPM

PCI Express Root port ASPM Setting

L1 Substates

PCI Express L1 Substates settings.

PME SCI

PCI Express PME SCI Enable/Disable.

Hot Plug

Designates this port as Hot Pluggable.

PCIe Speed

Configure PCIe Speed

PME Interrupt

PCI Express PME Interrupt Enable/Disable.

MSI

PCIE MSI Enable/Disable.

Extra Bus Reserved

Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

Reserved Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

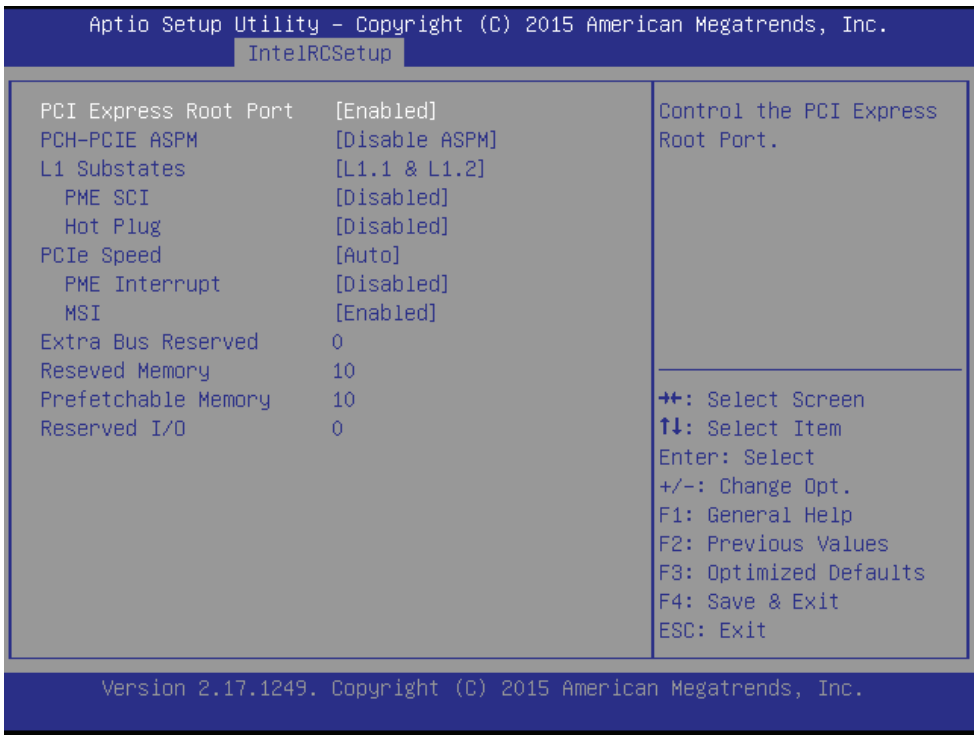
Prefetchable Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

Reserved I/O

Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.

4.5.7.2.4 PCI Express Root Port 4



PCI Express Root Port

Control the PCI Express Root Port.

PCH - PCIE ASPM

PCI Express Root port ASPM Setting

L1 Substates

PCI Express L1 Substates settings.

PME SCI

PCI Express PME SCI Enable/Disable.

Hot Plug

Designates this port as Hot Pluggable.

PCIe Speed

Configure PCIe Speed

PME Interrupt

PCI Express PME Interrupt Enable/Disable.

MSI

PCIE MSI Enable/Disable.

Extra Bus Reserved

Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

Reserved Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

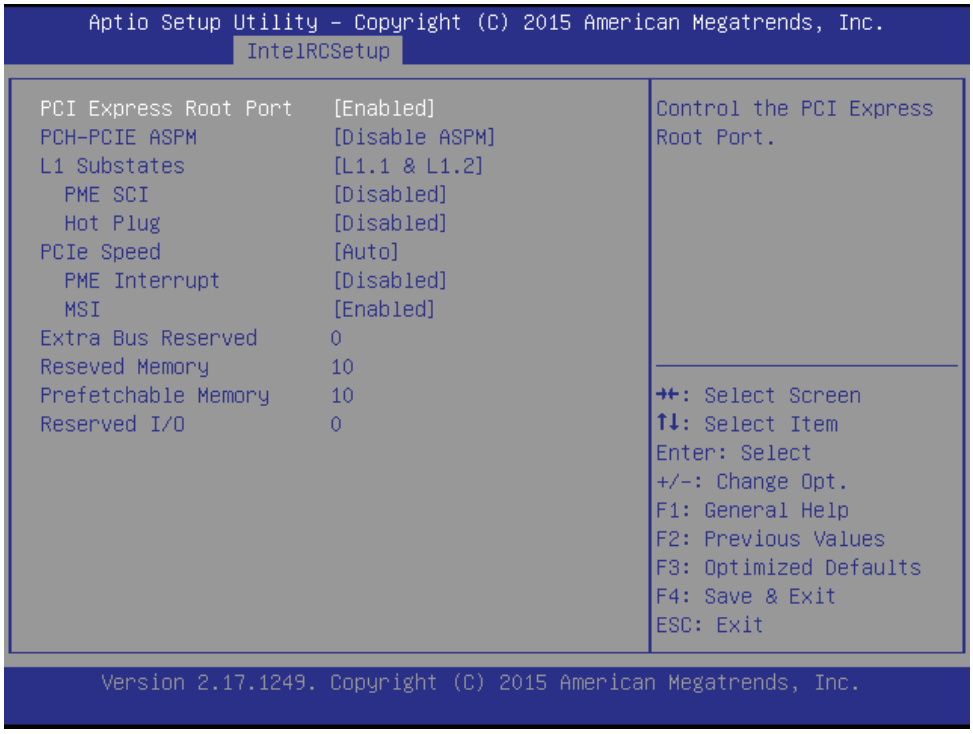
Prefetchable Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

Reserved I/O

Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.

4.5.7.2.5 PCI Express Root Port 5



PCI Express Root Port

Control the PCI Express Root Port.

PCH - PCIE ASPM

PCI Express Root port ASPM Setting

L1 Substates

PCI Express L1 Substates settings.

PME SCI

PCI Express PME SCI Enable/Disable.

Hot Plug

Designates this port as Hot Pluggable.

PCIe Speed

Configure PCIe Speed

PME Interrupt

PCI Express PME Interrupt Enable/Disable.

MSI

PCIE MSI Enable/Disable.

Extra Bus Reserved

Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

Reserved Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

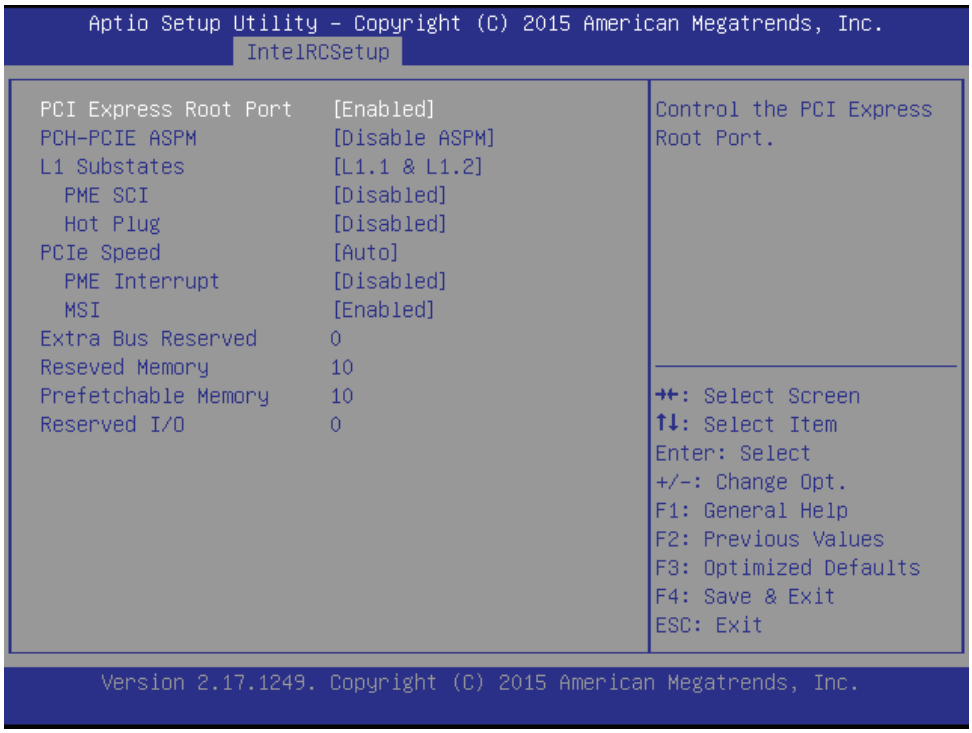
Prefetchable Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

Reserved I/O

Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.

4.5.7.2.6 PCI Express Root Port 6



PCI Express Root Port

Control the PCI Express Root Port.

PCH - PCIE ASPM

PCI Express Root port ASPM Setting

L1 Substates

PCI Express L1 Substates settings.

PME SCI

PCI Express PME SCI Enable/Disable.

Hot Plug

Designates this port as Hot Pluggable.

PCIe Speed

Configure PCIe Speed

PME Interrupt

PCI Express PME Interrupt Enable/Disable.

MSI

PCIE MSI Enable/Disable.

Extra Bus Reserved

Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

Reserved Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

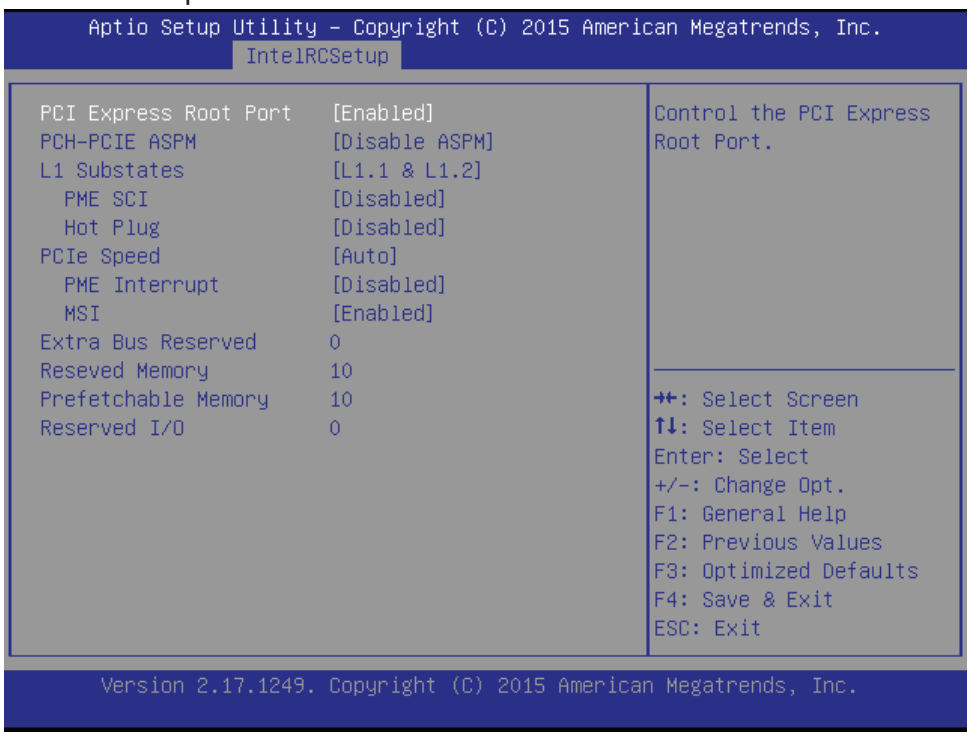
Prefetchable Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

Reserved I/O

Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.

4.5.7.2.7 PCI Express Root Port 7



PCI Express Root Port

Control the PCI Express Root Port.

PCH -PCIE ASPM

PCI Express Root port ASPM Setting

L1 Substates

PCI Express L1 Substates settings.

PME SCI

PCI Express PME SCI Enable/Disable.

Hot Plug

Designates this port as Hot Pluggable.

PCIe Speed

Configure PCIe Speed

PME Interrupt

PCI Express PME Interrupt Enable/Disable.

MSI

PCIE MSI Enable/Disable.

Extra Bus Reserved

Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

Reserved Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

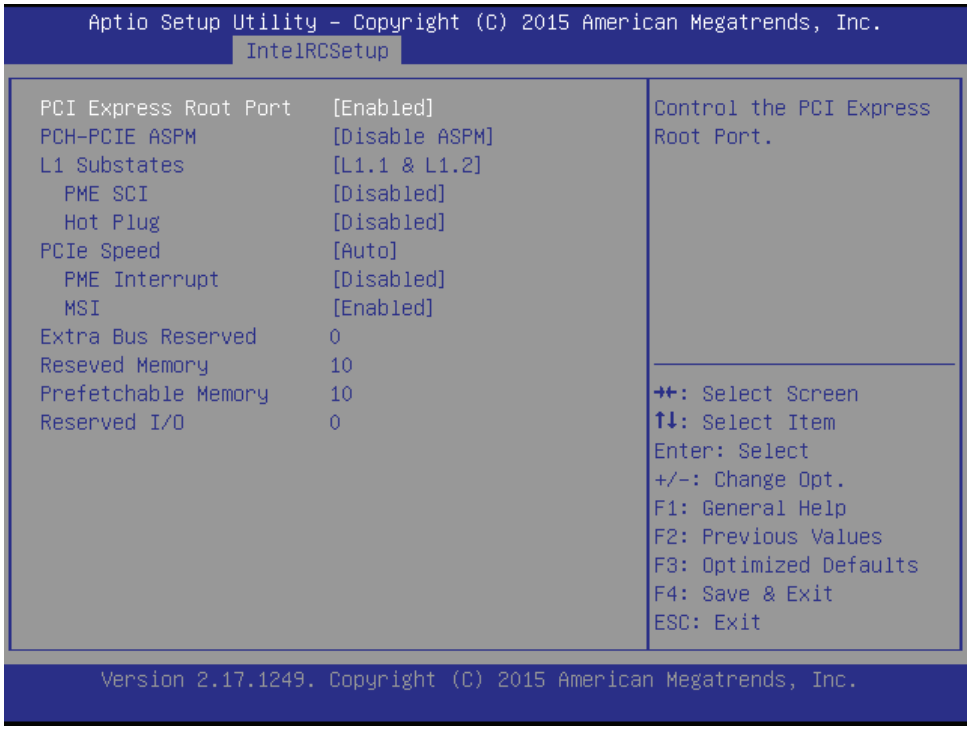
Prefetchable Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

Reserved I/O

Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.

4.5.7.2.8 PCI Express Root Port 8



PCI Express Root Port

Control the PCI Express Root Port.

PCH - PCIE ASPM

PCI Express Root port ASPM Setting

L1 Substates

PCI Express L1 Substates settings.

PME SCI

PCI Express PME SCI Enable/Disable.

Hot Plug

Designates this port as Hot Pluggable.

PCIe Speed

Configure PCIe Speed

PME Interrupt

PCI Express PME Interrupt Enable/Disable.

MSI

PCIE MSI Enable/Disable.

Extra Bus Reserved

Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

Reserved Memory

Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

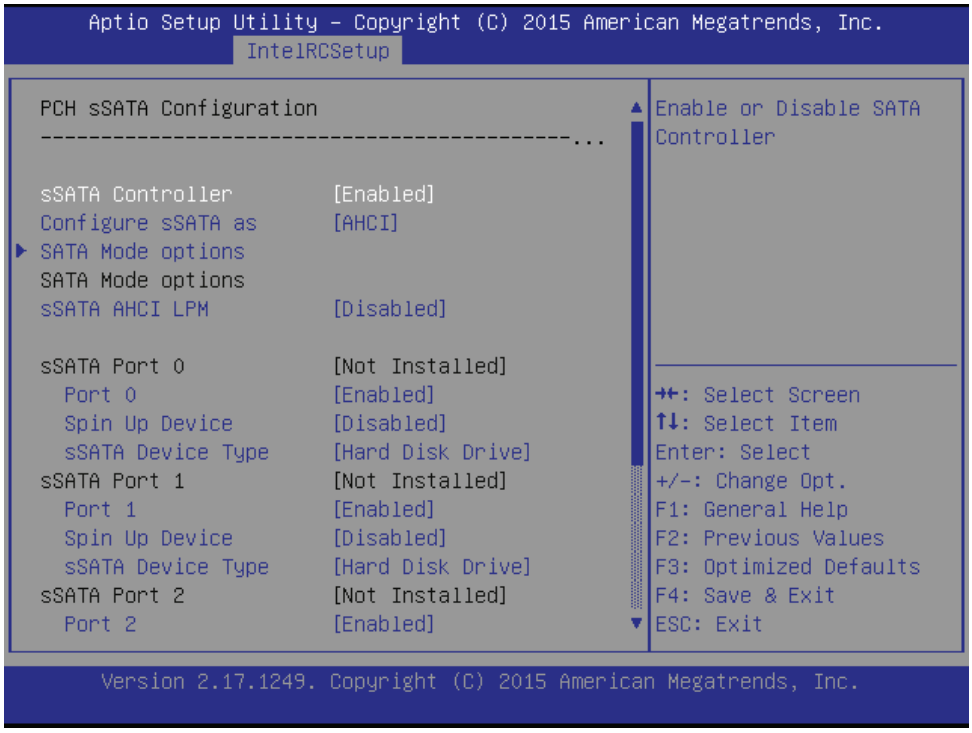
Prefetchable Memory

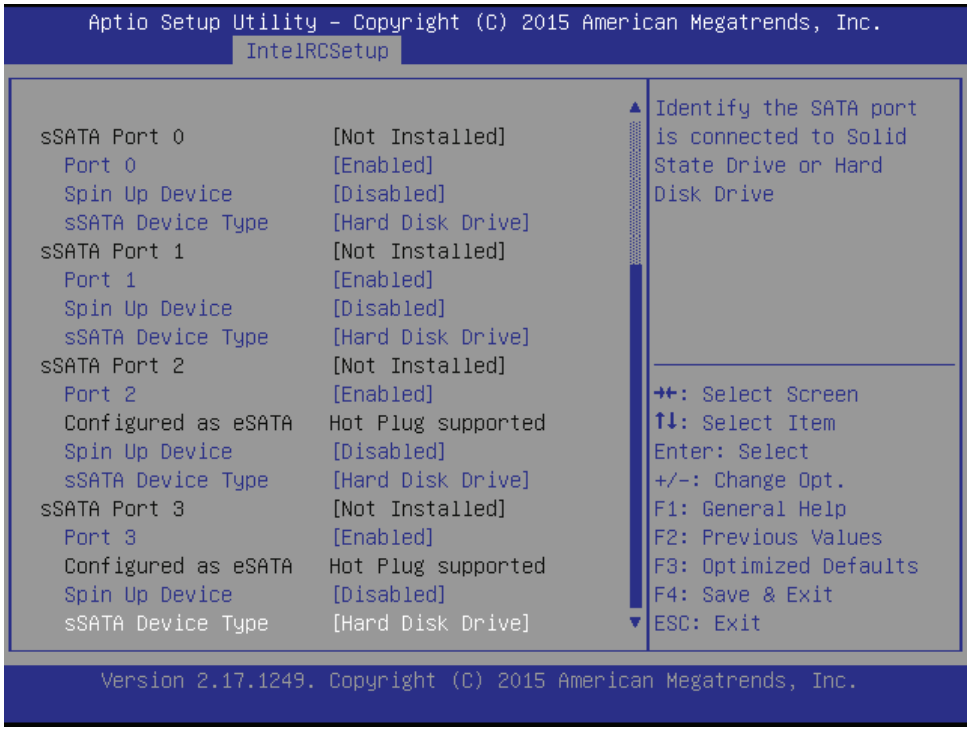
Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

Reserved I/O

Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.

4.5.7.3 PCH sSATA Configuration





sSATA Controller

Enable or Disable SATA Controller

Configure sSATA as

This will configure sSATA as IDE ,RAID or AHCI.

sSATA AHCI LPM

Enables/Disables Link Power Management

Port 0, 1, 2

Enable or Disable SATA Port

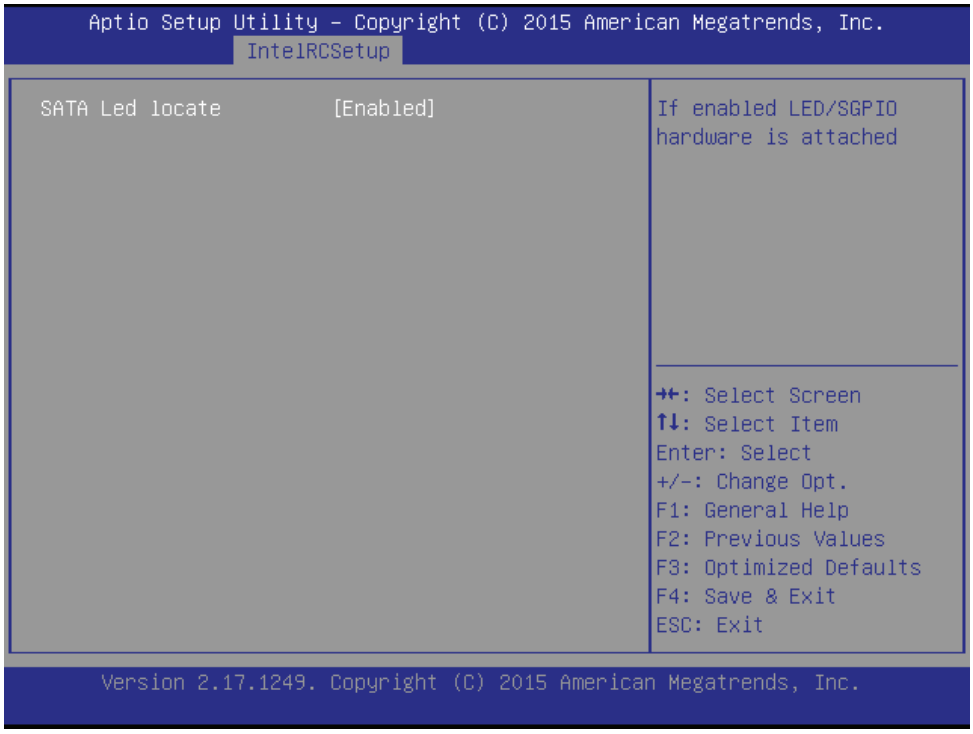
Spin Up Device

If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.

sSATA Device Type

Identify the SATA port is connected to Solid State Drive or Hard Disk Drive

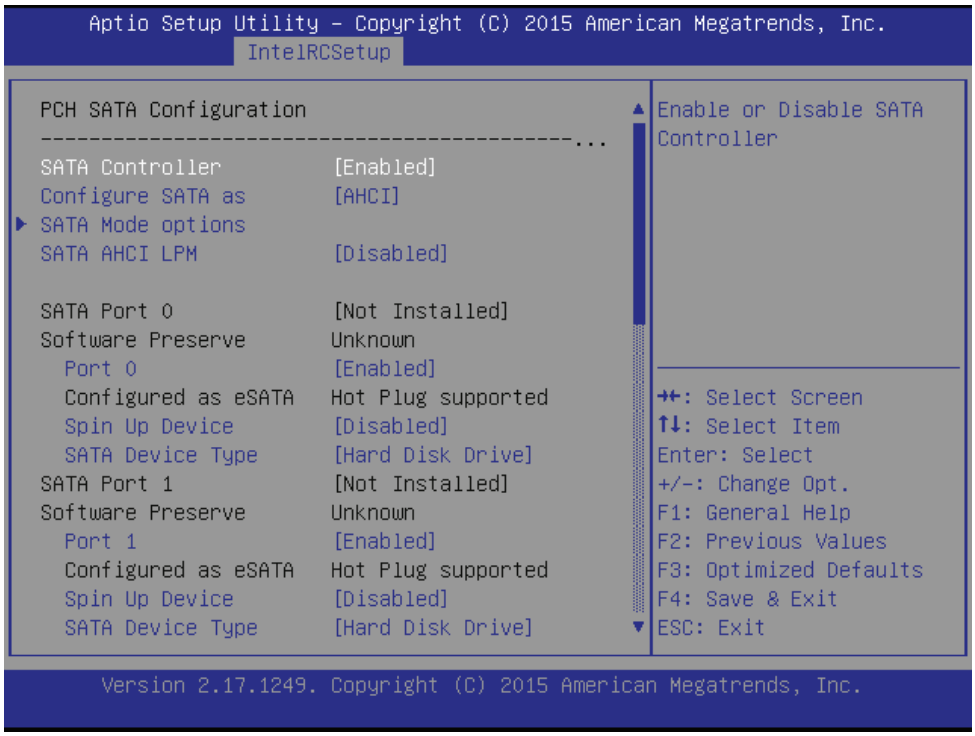
4.5.7.3.1 SATA Mode Options

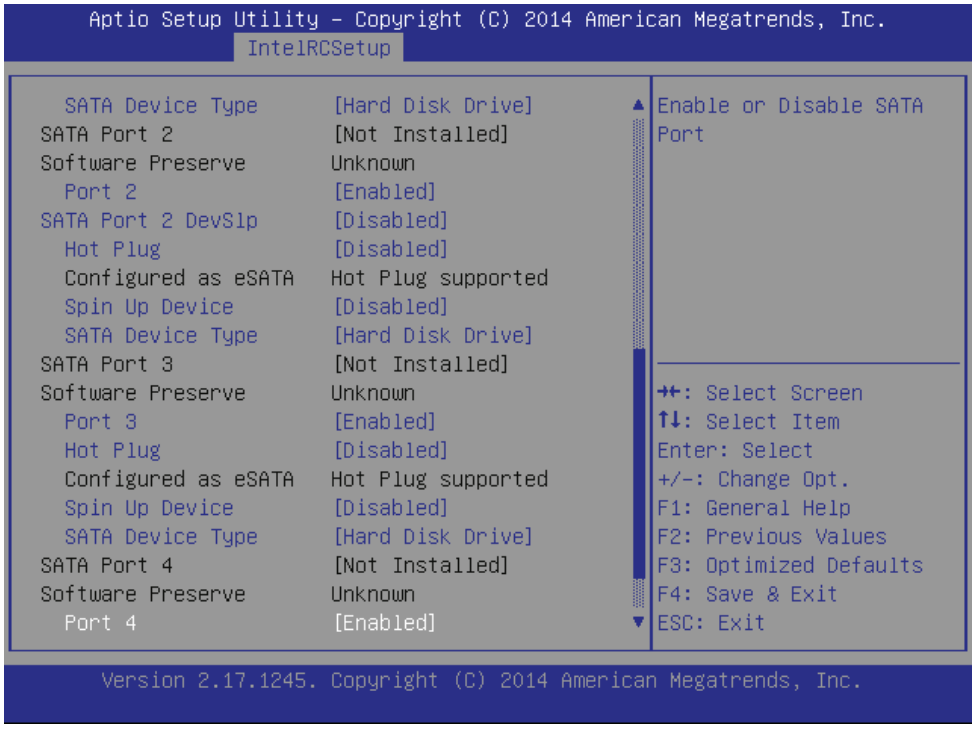


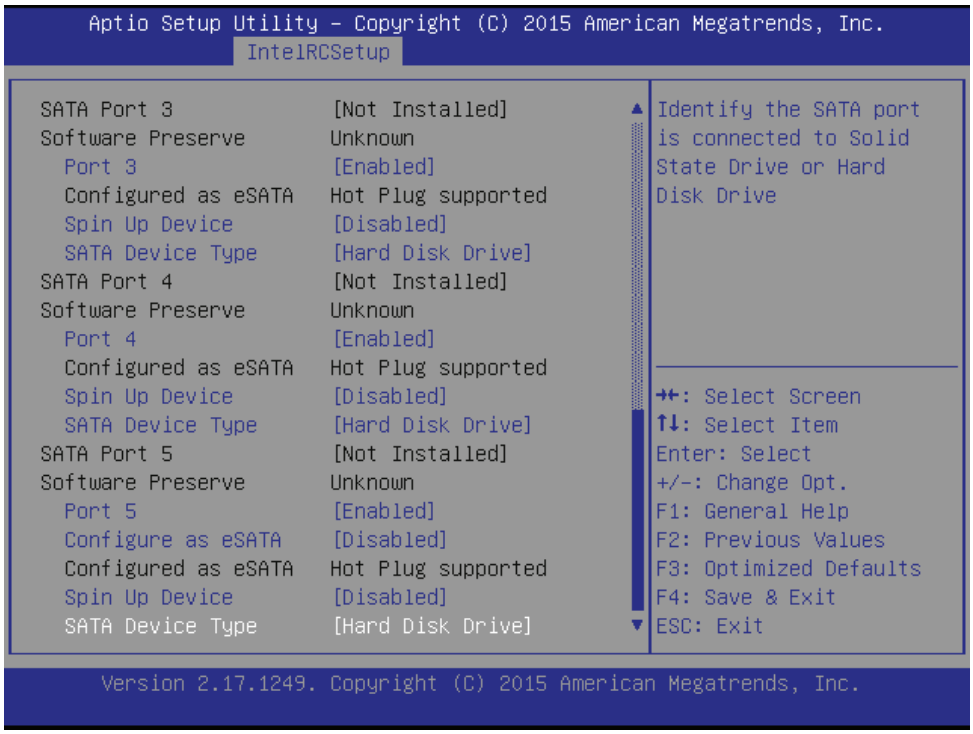
SATA Led locate

If enabled LED/SGPIO hardware is attached

4.5.7.4 PCH SATA Configuration







SATA Controller

Enable or Disable SATA Controller

Configure SATA as

This will configure SATA as IDE, RAID or AHCI.

SATA Mode options

SATA mode related options

SATA AHCI LPM

Enables/Disables Link Power Management

SATA Port 0, 1, 2, 3, 4, 5

SATA Port 0, 1, 2, 3, 4, 5

Software Preserve

Software Preserve

Port 0, 1, 2, 3, 4, 5

Enable or Disable SATA Port

Configure as eSATA

Configures port as External SATA (eSATA)

Spin Up Device

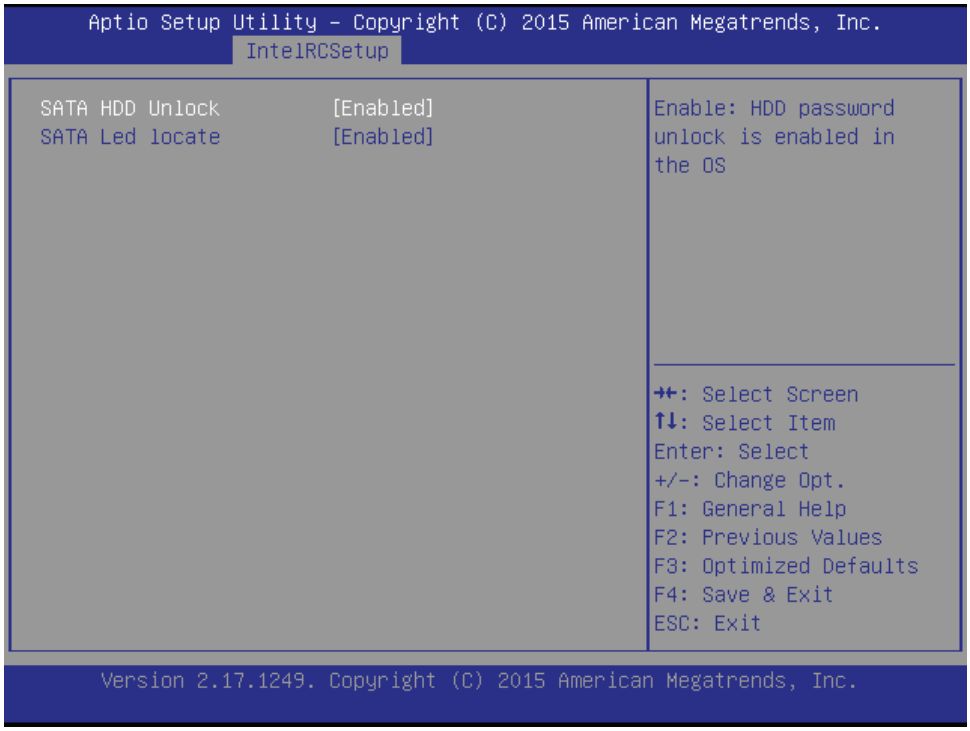
If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at

boot.

SATA Device Type

Identify the SATA port is connected to Solid State Drive or Hard Disk Drive

4.5.7.4.1 SATA Mode Options



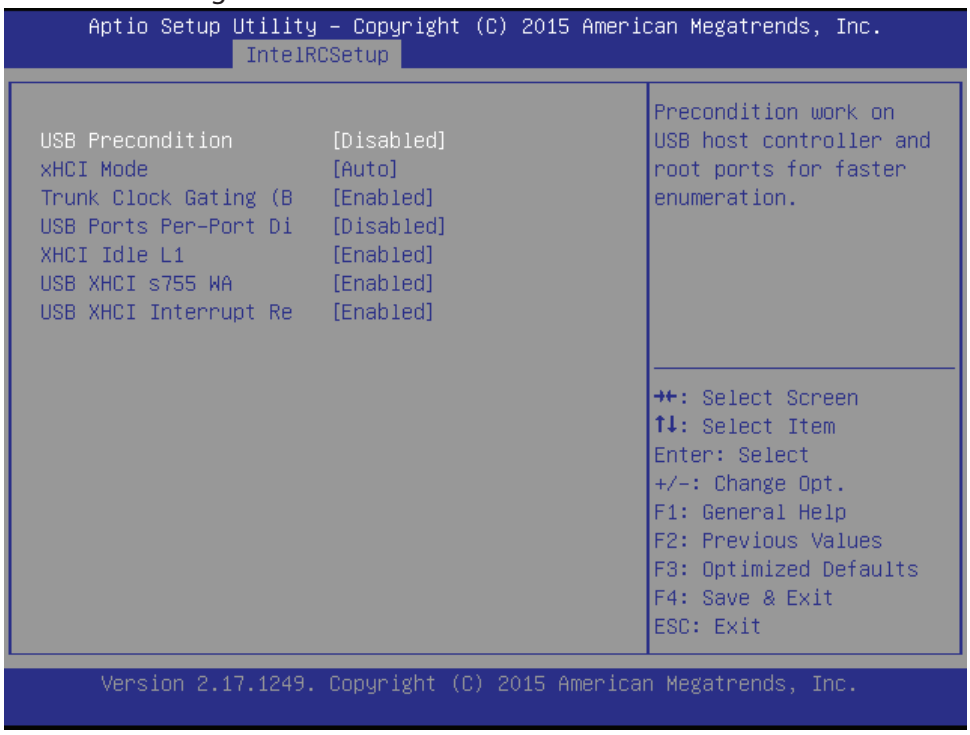
SATA HDD Unlock

Enable: HDD password unlock is enabled in the OS

SATA Led locate

If enabled LED/SGPIO hardware is attached

4.5.7.5 USB Configuration



USB Precondition

Precondition work on USB host controller and root ports for faster enumeration.

XHCI Mode

Mode of operation of xHCI controller.

Trunk Clock Gating

Enable/Disable BTCG

USB Ports Per-Port

Control each of the USB ports (0~13) disabling.

XHCI Idle L1

Enabled XHCI Idle L1. Disabled to workaround USB3 hot plug will fail after 1 hot plug removal. Please put the system to G3 for the new settings to take effect.

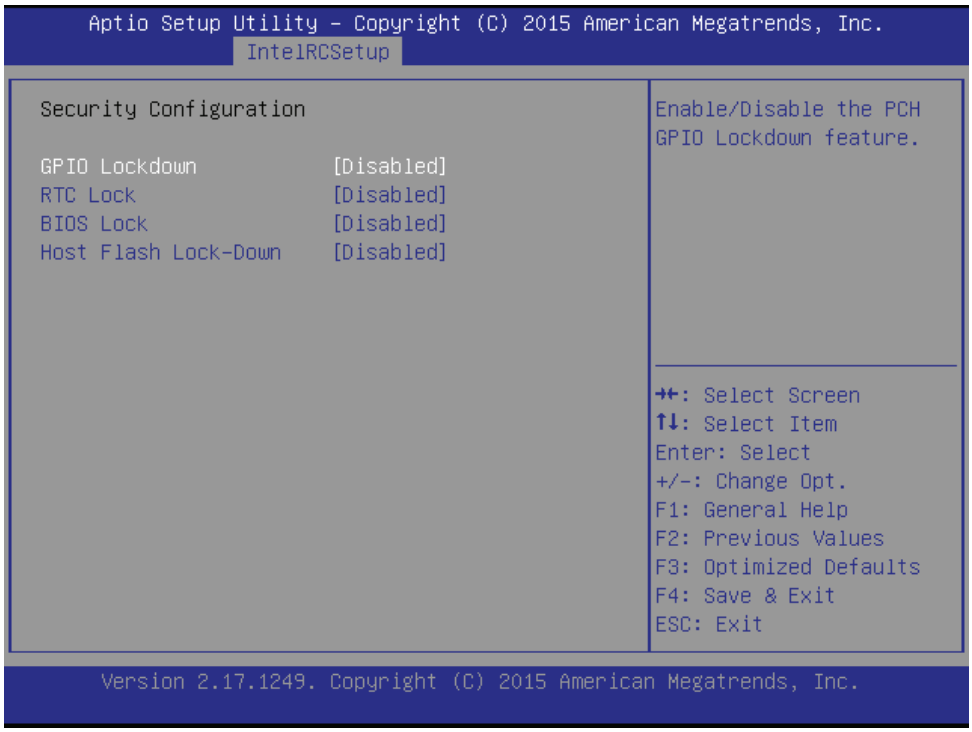
USB XHCI s755

ONLY for WBG < B1! Enable/Disable USB XHCI s755 WA to avoid CATERRs.

USB XHCI Interrupt

Enable/Disable USB XHCI s116 WA. ENABLE = hides MSI capability on XHCI

4.5.7.6 Security Configuration



GPIO Lockdown

Enable/Disable the PCH GPIO Lockdown feature.

RTC Lock

Enable will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM

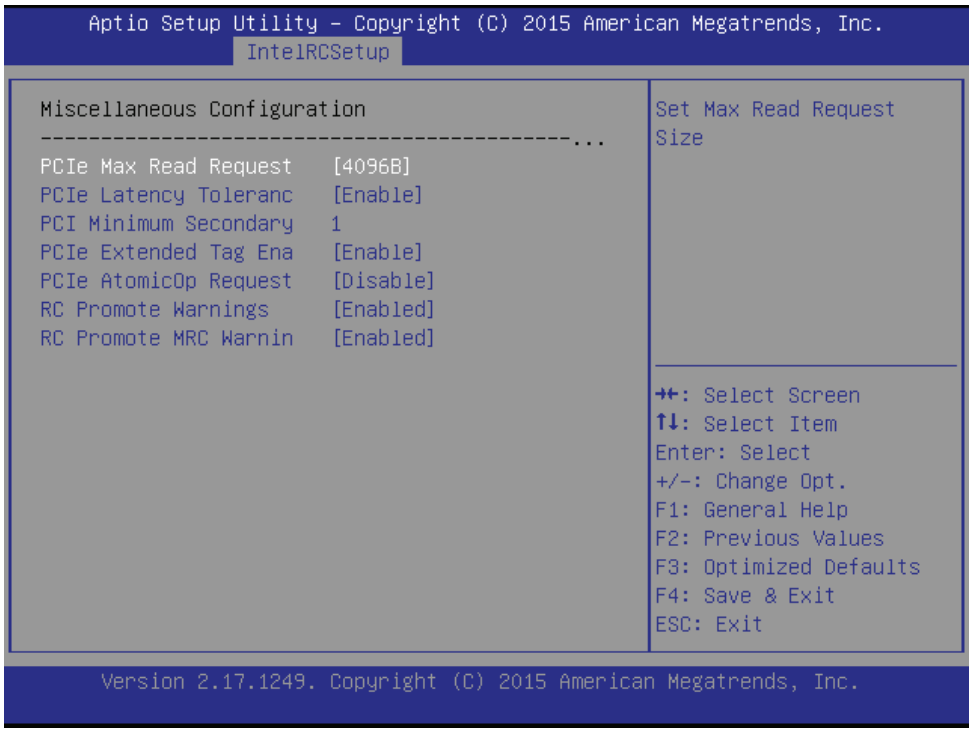
BIOS Lock

Enable/Disable the PCH BIOS Lock Enable feature.

Host Flash Lock-Down

Enable/Disable Host Flash Lock-Down

4.5.8 Miscellaneos Configuration



PCIe Max Read Request

Set Max Read Request Size

PCIe Latency Tolerance

Enable or disable or Auto the LTR support

PCI Minimum Secondary Bus Number

Specify the PCI minimum secondary bus number in system

PCIe Extended Tag Enable

Enable or Disable Extended Tag Enable Field Support

PCIe AtomicOp Request

Enable or disable AtomicOp Request support

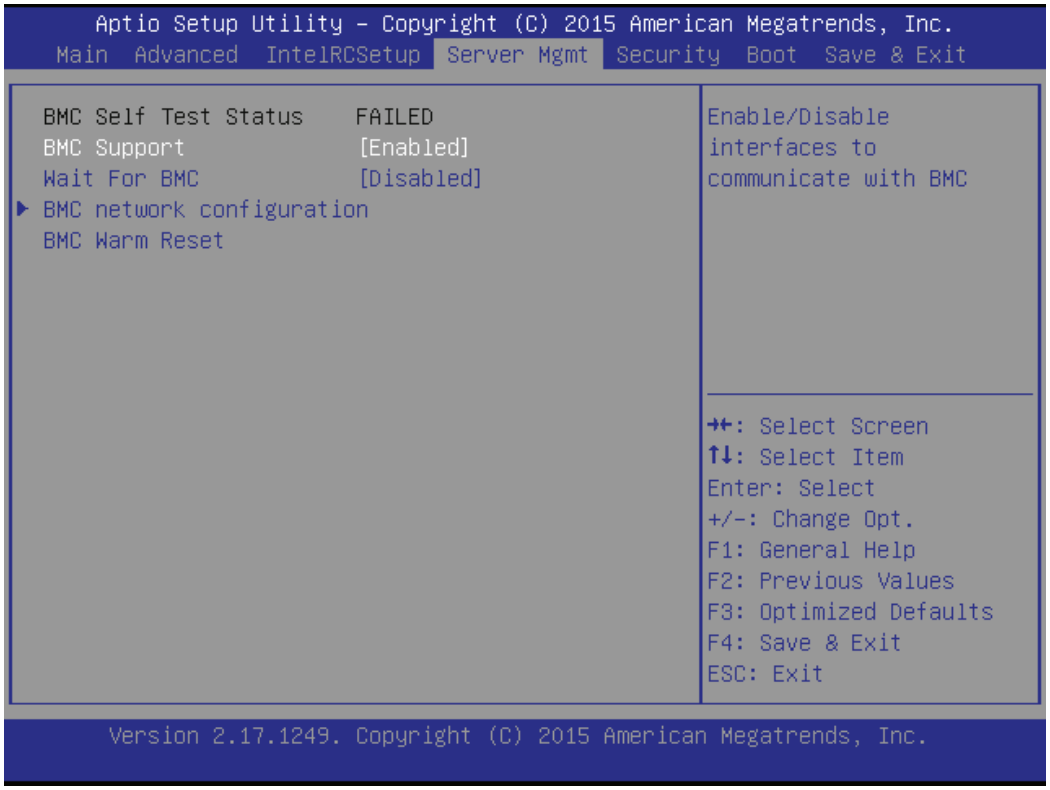
RC Promote Warnings

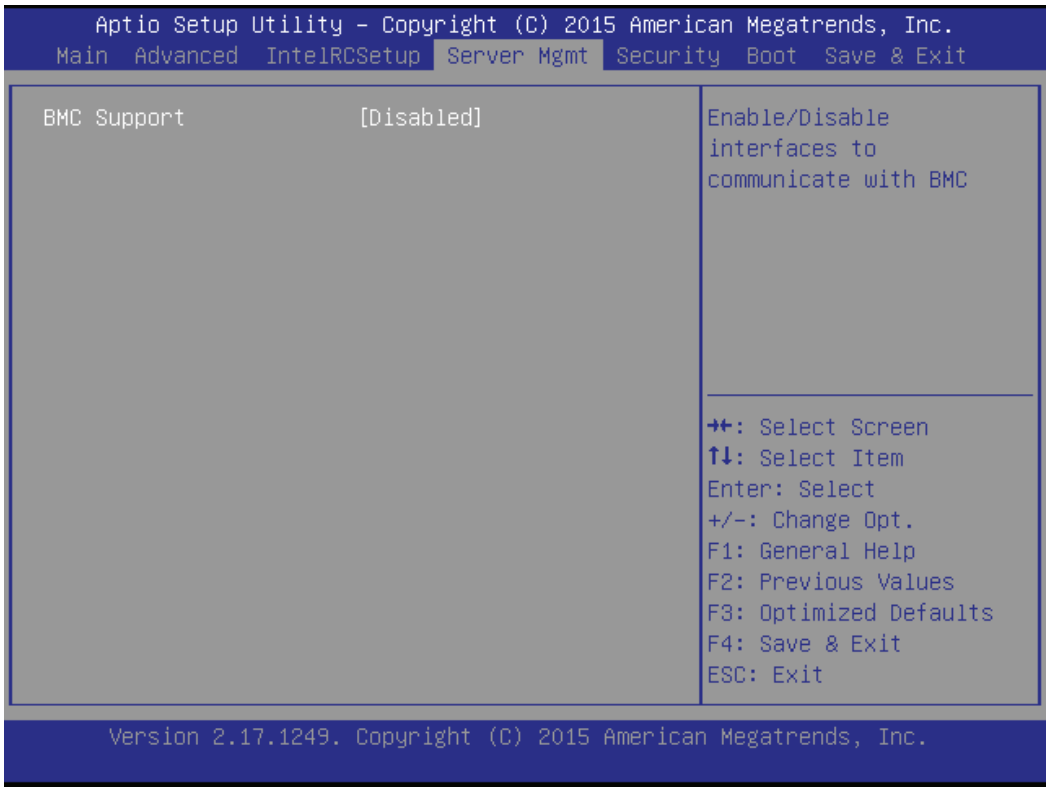
If enabled RC warnings are promoted to errors (except MRC warnings)

RC Promote MRC Warning

If enabled MRC warnings are promoted to errors

4. 6 Server Mgmt





BMC Support

Enable/Disable interfaces to communicate with BMC

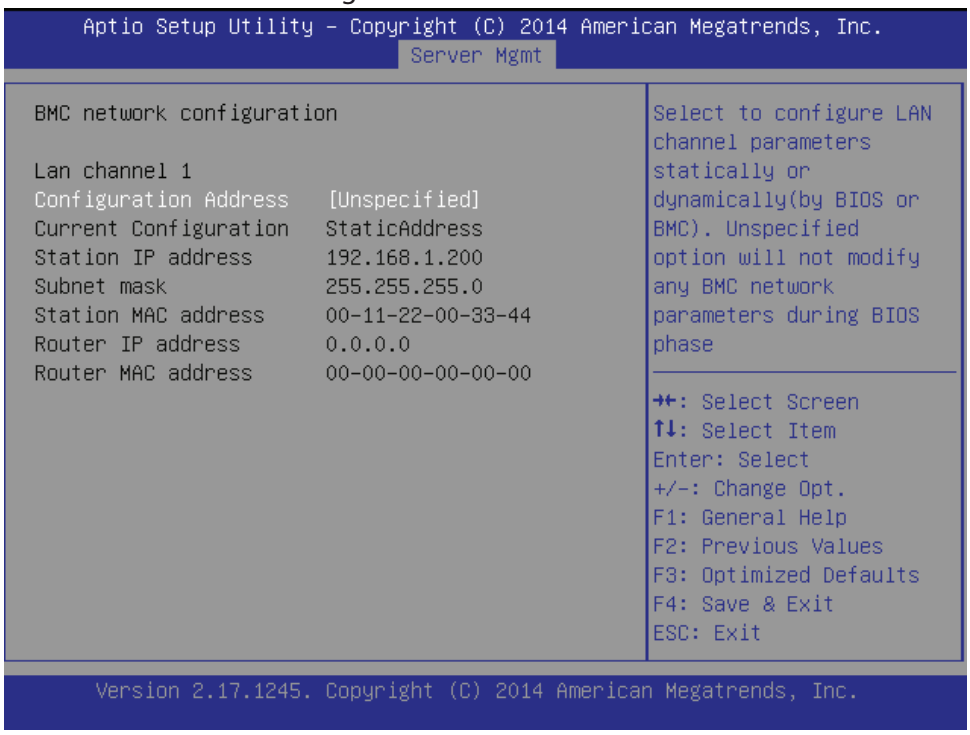
Wait For BMC

Wait For BMC response for specified time out. In PILOTII, BMC starts at the same time when BIOS starts during AC power ON. It takes around 30 seconds to initialize Host to BMC interfaces.

BMC Warm Reset

Press <Enter> to do Warm Reset BMC.

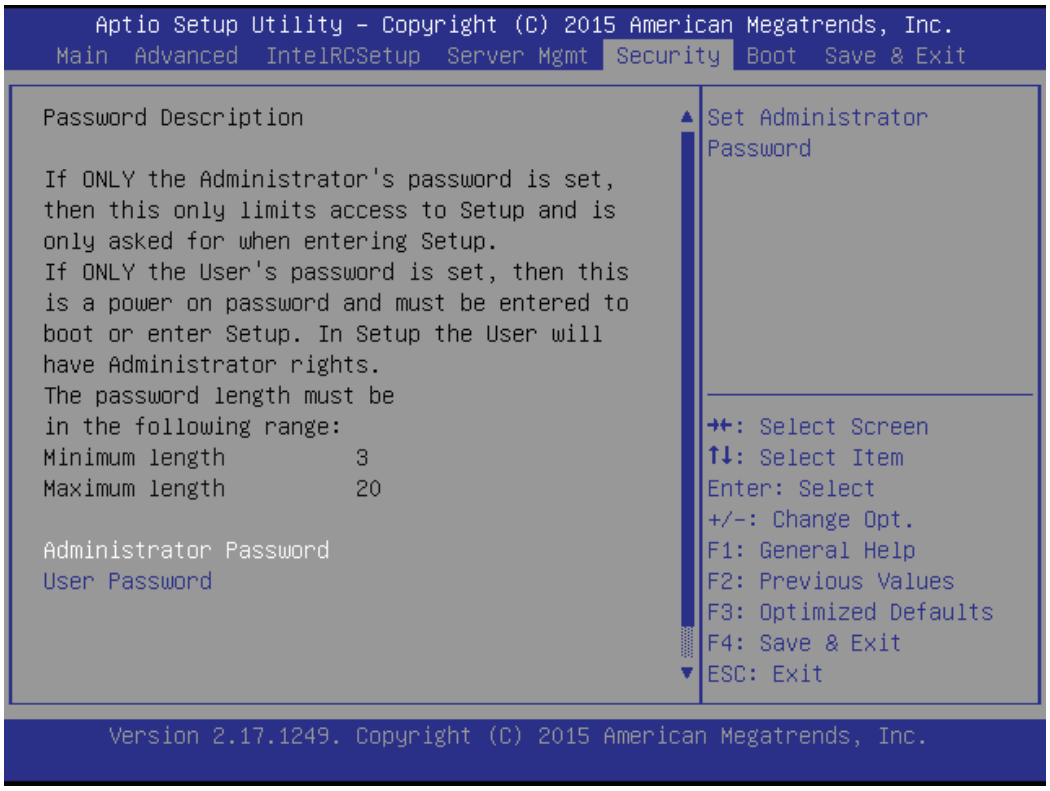
4. 6.1 BMC Network Config uration



4. 7 Security Menu

⇩Use the Security Setup option as follows:

1. Choose "Security" from the main menu. The following screen appears:



2. Move between items and select values by using the arrow keys. Modify the selected fields using the PgUP/PgDN keys. Please press the <F1> key for information on the various options.

3. After you have finished with the Security setup, press the <? > or <? > key to switch to other setup menu or press <F4> key to save setting.

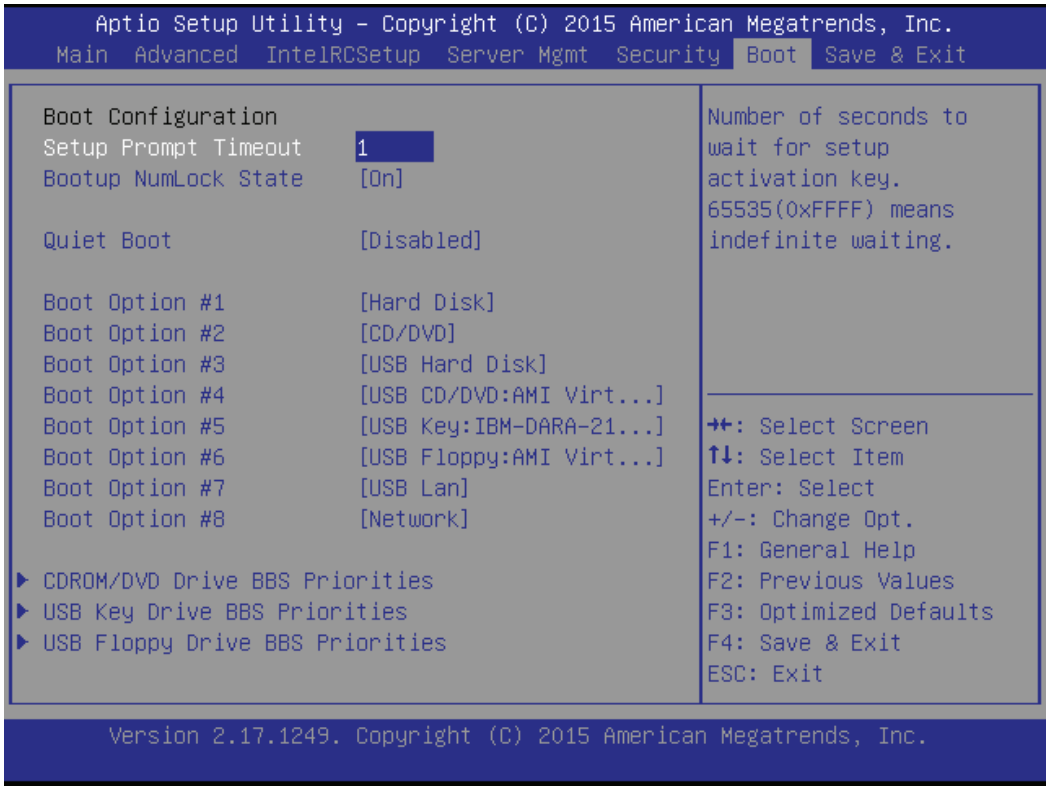
Administrator Password:

This item allows you to set or change the administrator password. The Administrator Password item on top of the screen shows the default Not Installed. After you have set a password, this item shows Installed.

User Password:

Set User Password

4. 8 Boot Menu



Setup Prompt Timeout

Use the <+> and <-> keys to adjust the number of seconds to wait for setup activation key.

Bootup NumLock State

This item allows you to select "On" or "Off" power-on state for the NumLock.

Quiet Boot

If this option is set to Disabled, the BIOS displays normal POST messages. If Enabled, an OEM Logo is shown instead of POST messages.

CDROM/DVD Drive BBS Priorities

Specifies the Boot Device Priority sequence from available CDROM/DVD Drives.

USB Key Drive BBS Priorities

Specifies the Boot Device Priority sequence from available USB Key Drives.

USB Floppy Drive BBS Priorities

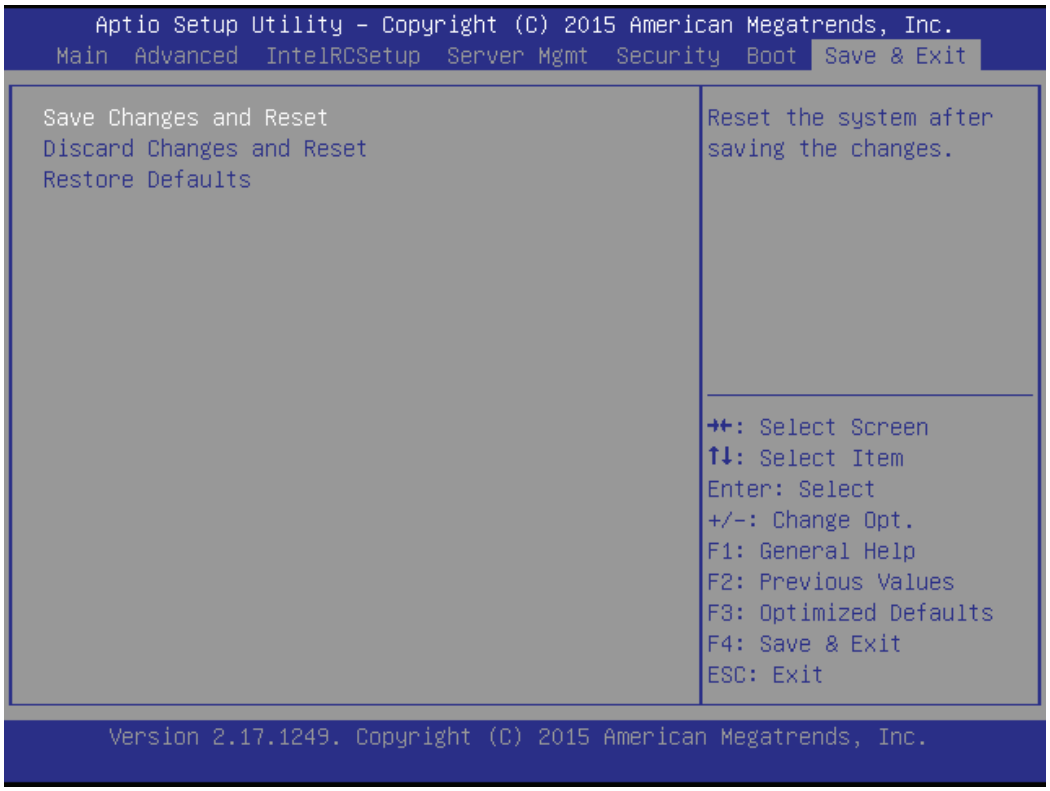
Specifies the Boot Device Priority sequence from available USB Floppy Drives.

4. 9 Save & Exit

The item allows you to save or discard your changes to the BIOS items, and load the optimal defaults or user defaults for the BIOS items.

⇩ Use the Exit option as follows:

1. Choose "Exit" from the main menu, the following screen appears.



2. Move between items and select values by using the arrow keys. Modify the selected fields using the PgUP/PgDN keys. For information on the various options, please press <F1> key.

3. Press the <?> or <?> key to switch to other setup menu or press <F4> key to save setting.

Save Changes and Reset:

Store all changes you made into CMOS and reboot system. F4 key can be used for this operation.

Discard Changes and Reset:

Discard all changes you made and reboot system. ESC key can be used for this operation.

Restore Defaults:

This item allows you to load optimal defaults for each setting on the Setup Utility menus, which will provide the best performance settings for system. F3 key can be used for this operation.

Chapter 5. Utility & Driver Installation

Please install the GbE modules properly before you install the OS, driver or other software.

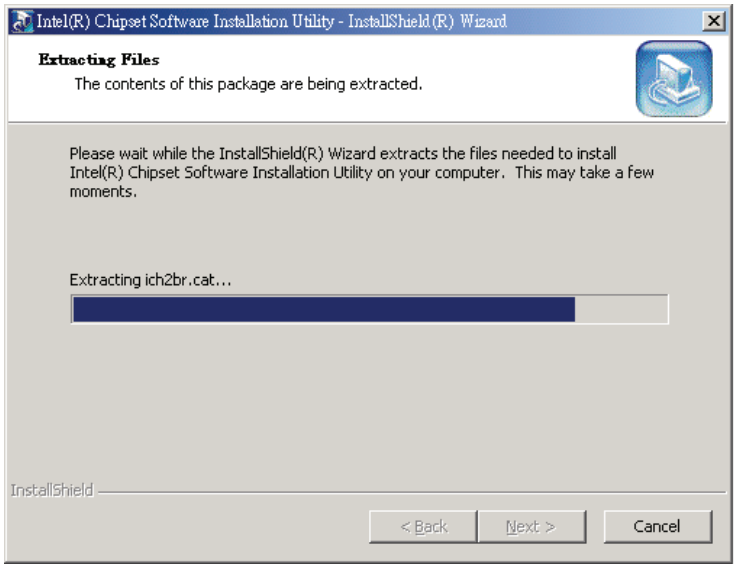
5.1 Operation System Supporting

PL-80930 can support Windows® and Linux® operating systems as follows. Before installation, please check your OS version. If your OS is not in the following list, please upgrade your OS version.

OS	Version
DOS	DOS 6.22
Windows®	Microsoft Windows Server 2008 R2 (x64) Microsoft Windows 2012 (x64) Microsoft Windows 2012 R2 (x64)
Linux®	Red Hat Enterprise Linux Server* (x32 and x64) SUSE Linux Enterprise Server* (x86 and x64) Ubuntu Linux Server* (x86 and x64)

5.2 System Driver Installation

PL-80930 offers the system driver in the setup CD. Please install the driver following the procedures.



5. 3 LAN Driver Installation

PL-80930 offers the LAN driver in the setup CD. Please click the Autorun file and install the driver following the procedures.

1. Insert the setup CD of PL-80930 into your CD-ROM drive.
2. Choose the Drivers file to click the Autorun icon.
3. Follow the procedures to finish the installation.

Appendix A: DOS / Linux Sample Code

We offer some sample code for PL-80930 appliance for customers wanting sample code. It is placed into the Driver CD for software development use.

Custom x86 Embedded Solutions

Appendix B : Cable Development Kit

The PL-80930 is offered with some cables for development purposes.

DK00 2

Item & Description	Part No.	Qty
Ethernet Cat. 5 Cable 2M/ RoHS	CB-EC5200-00	1
Cross Over 2M Color/ RoHS	CB-CO5202/4-00	1
RJ45 to DB9 2M Cable/ RoHS	CB-RJDB91-00	1
2m null modem cable/ RoHS	CB-DB9200-01	1
VGA CABLE (2mm) 15CM/ RoHS	CB-IVGA01-00	1
KB/MS CABLE 15CM/ RoHS	CB-IPS200-00	1
USB CABLE/ RoHS	CB-IUSB01-00	1

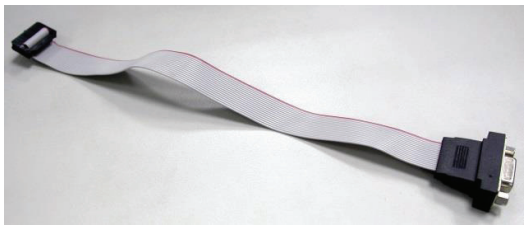
CB-EC5200-00

CB-CO5202/4-00

CB-RJDB91-00

CB-DB9200-00

CB-IVGA01-00



CB-IPS200-00

CB-IUSB01-00

Appendix C: REACH

REACH is a regulation of the European Union, adopted to improve the protection of human health and the environment from the risks that can be posed by chemicals, while enhancing the competitiveness of the EU chemicals industry. It also promote alternative methods for the hazard assessment of substances in order to reduce th number of tests on animals.

DO NOT throw the motherboard in municipal waste. This product has been designed to enable proper reuse of parts and recycling. This symbol of the crossed out wheeled bin indicates that the product (electrical and electronic equipment) should not be placed in municipal waste. Check local regulations for the disposal of electronic products.

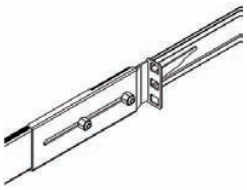
DO NOT throw the mercury-containing button cell battery in municipal waste. This symbol of the crossed out wheeled bin indicates that the battery should not be placed in municipal waste.

Check battery polarity before installation/replacement. Installing battery with reverse polarity can cause explosion. Dispose of used batteries according to your local regulations.

Replace only with the same or equivalent type recommended by the manufacturer.

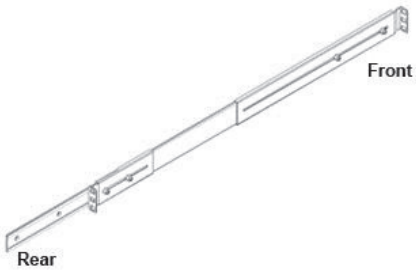
Appendix D: Rack Mount Kit Installation

Step 1 – Remove the chassis (inner) member



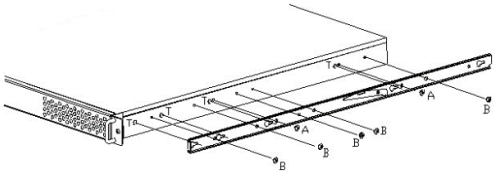
Take the inner member (Bingo slide series) a part by pulling front activating release latch forward

Step 2 - mount the chassis (inner) member to the chassis



Each slide is pre-attached with front and rear adjustable brackets. Loosen the nuts on the both brackets and decide the proper setback distance to the opening then tighten the nuts on the front brackets.

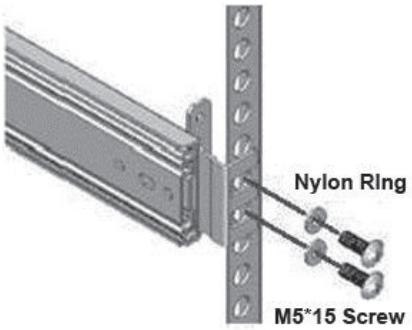
Step 3 - Extend the rear brackets to where it reaches the rear rack.



Do not fully rear bracket mounting screws until adjustment is made. You may for M4 or M5 pan head screw. The screw head of either M4 or M5 cannot exceed 2.0mm. Alternatively, you may mount the slide member to the chassis through standoff. Likewise, the

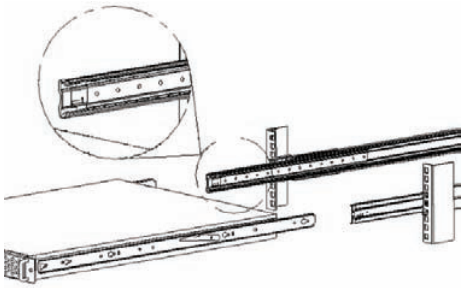
head of stand-off cannot exceed 2.0mm. Each side of chassis is highly suggested to use 3 of screws or stand-off for slide attachment.

Step 4 - At tach the chassis (outer) member to the rail



Attach the L-shaped bracket rack to the front mounting flange using M5 screw & ring from screw kit. Insert the stag into the upper and lower square holes on rail from the back of rail. Push the safety lock forward to secure the bracket. It is important to check if the safety lock is in unlocked position before mounting the brackets.

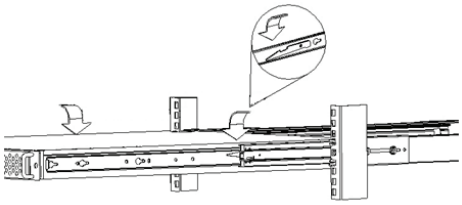
Step 5 - Attach the inner slide member to your chassis



Attach the inner slide member to your chassis using M4 or M5 * 5 screw from screw kit.
Insert the chassis (inner) member into the cabinet member as shown on the drawing. It is important to check if the ball retainer is in fully open position before install the chassis. It might cause catastrophic damage to the chassis if ball retainer is not in fully open position while mounting the chassis. While you are pushing

chassis back to the cabinet, you need to release the slide from locking position by pressing the trigger down.

Step 6 - Mount the chassis into the cabinet



Pick up your chassis; Insert your chassis with inner slide member into the intermediate member. The chassis will be locked when it reaches the fully open position, then pull forward on the front activating release latch in order to push your chassis all the way inward till the closed position.

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