



# User Manual

V 1.0.1

## Model: PL-60590

Fanless Rugged Embedded Box Computer with  
Intel Core 2 Duo Processor



[sales@win-ent.com](mailto:sales@win-ent.com) +1 (978) 688-2000

## Table of Contents

Chapter 1 General Information.....	3
1-1 Introduction.....	3
1-2 Specifications.....	3
1-3 Packaging.....	6
1-4 System Layout.....	6
1-5 MB-73180 SBC Layout.....	9
1-6 MB-73180 Dimensions .....	10
Chapter 2 Connector/Jumper Settings.....	13
2-1 List of Connectors and Jumpers for the MB-73180 board.....	13
2-2 List of Connectors and Jumper for the R093A MIO Module.....	13
2-3 Location of Connectors and Jumpers.....	14
2.4 Connector Pin Assignments.....	17
Chapter 3 Cooling Considerations.....	28
3-0 Proper Cooling.....	28

## Chapter 1 General Information

### 1-1 Introduction

The PL-60590 is a fanless embedded box PC designed for wide application. With four serial ports, four USB ports, DVI, VGA, Dual LAN, PS/2, Audio, it can fulfill various applications such as automation, medical, the automotive PC market, etc.

The PL-60590 is equipped with the low voltage Intel® Core 2 Duo processor, Intel 945GME chipset, a unique heat sink design lets the PL-60590 work without a fan.

### 1-2 Specifications

#### ■ System

CPU	Intel® Socket 479 Core™ 2 Duo/Core™ Duo/Celeron® M processors with 533/667MHz FSB
BIOS	Award® 512KB Flash BIOS
System Chipset	Intel® 945GME+ICH7R
System Memory	1 x 240-pin DIMM socket supports DDRII 533/667 max. up to 2GB w/o ECC

#### ■ Display

Chipset	Built-in 945GME chipset supports dual independent displays
Display Memory	1/4/8/16/32/64MB
Display Interface	CRT DVI & 24-bit LVDS (Optional)

#### ■ Ethernet

Ethernet Controller	Intel® 82573L GbE controllers
Ethernet Connectors	2 x RJ-45

#### ■ Audio & TV Out (Optional)

---

# User's Manual

Audio	AC 97
Audio Interface	Mic in, Speaker out
TV Out	S-Video

## ■ *Other*

Watchdog Timer	255 level timer interval, setup by software
MIO Module	Support optional LVDS, DVI, S-Video, Mic in, Speaker out expansion

## ■ **Features:**

- Fanless operation
- Intel Core™ 2 Duo processors with 533/667MHz FSB
- Fully featured I/O
- 10/100/1000 LAN Ethernet interface
- One mounting kit for 2.5" HDD
- Anti-vibration for maximum reliability

## ■ *Software Options*

Windows XP Embedded, Windows 2000/XP
--------------------------------------

## ■ *Storage*

HDD	Supports drive bay space for 2.5" HDD
SSD Interface	Supports CompactFlash™ socket for type II CompactFlash™ disk

## ■ *Mechanical*

Front Panel External I/O	2 x USB port Power/HDD LEDs
Rear Panel External I/O	2 x USB port 1 x PS/2 connector

## User's Manual

	1 x VGA connector 4 x serial port 2 x RJ45 connector 1 x DC IN 1 x Reset button 1 x Mic in 1 x Speak out 1 x LVDS 1 x DVI 1 x S-Video
Dimensions ( W x D x H )	220mm (W) x 217mm (D) x 88mm (H) (8.7"W x 8.5"D x 3.5"H)

### ■ **Power Supply**

Input Voltage	100~240Vac
Output Rating	Max. +12V @ 5A
Output Voltage	+12Vdc

### ■ **Environment**

Operating Temperature	32 ~ 104°F ( 0 ~ 40°C )
Storage Temperature	-4 ~ 167°F ( -20 ~ 75°C )
Relative Humidity	5 to 95% relative humidity, non-operating, non-condensing
Vibration Loading During Operation	When system is equipped with CompactFlash™ disk, only 3Grms, Sine Wave, 10~15Hz, 1hr/axis
EMC Approved	CE, FCC

For more information on PL-60590 or other WIN Enterprises products visit our website

<http://www.win-ent.com> .

For Technical Supports or Free Catalog, please send mail to

[consultants@win-ent.com](mailto:consultants@win-ent.com) .

## 1-3 Packaging

Please make sure that the following materials have been packed with the board before starting install your PL-60590.

- 1 x PL-60590 unit
- 1 x CD (Manual, Quick installation guide, Utility driver)

## 1-4 System Layout

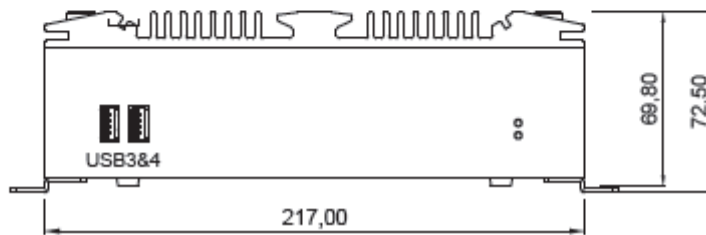
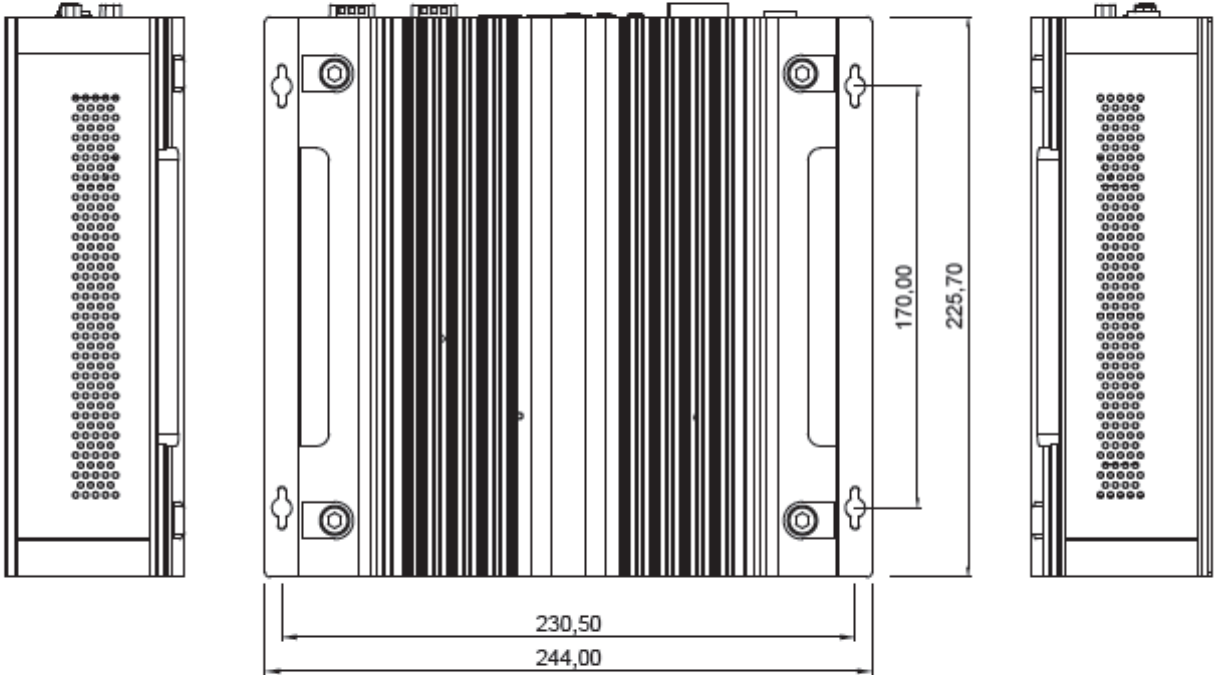
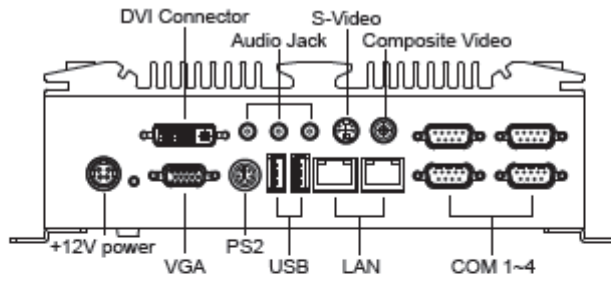
**PL-60590 Front View**



## PL-60590 Rear View

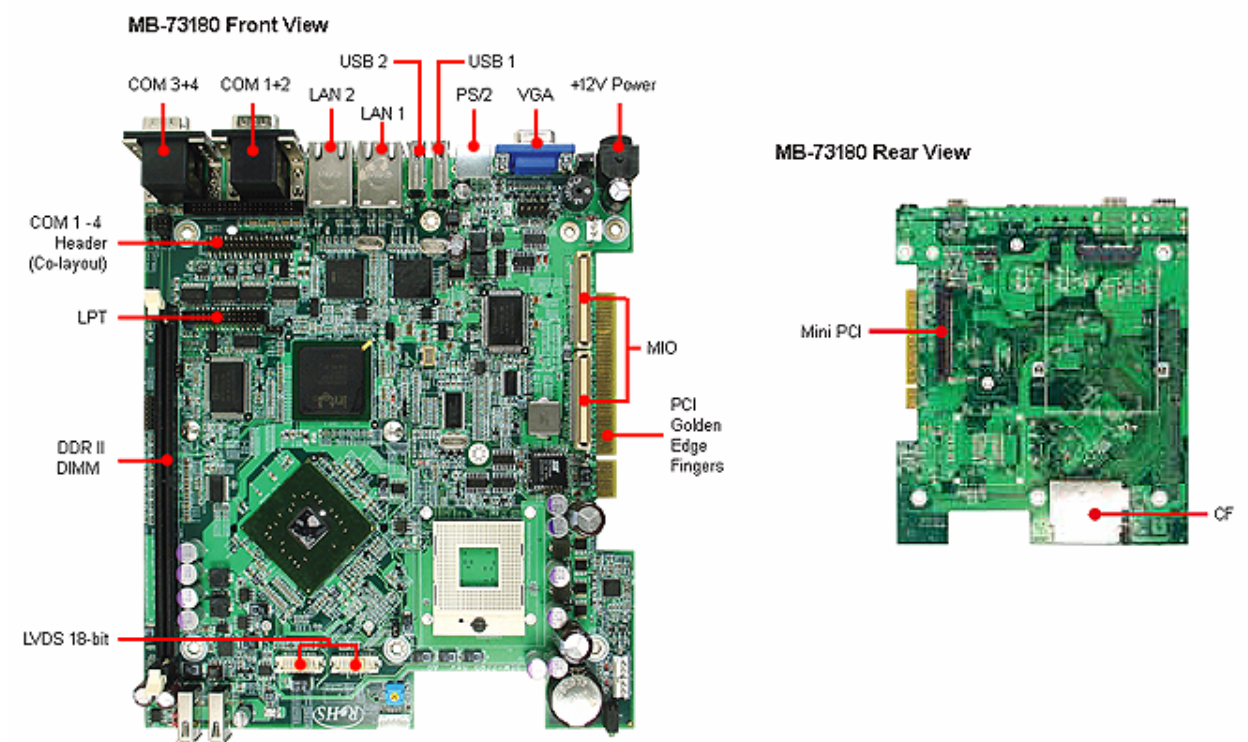


# User's Manual

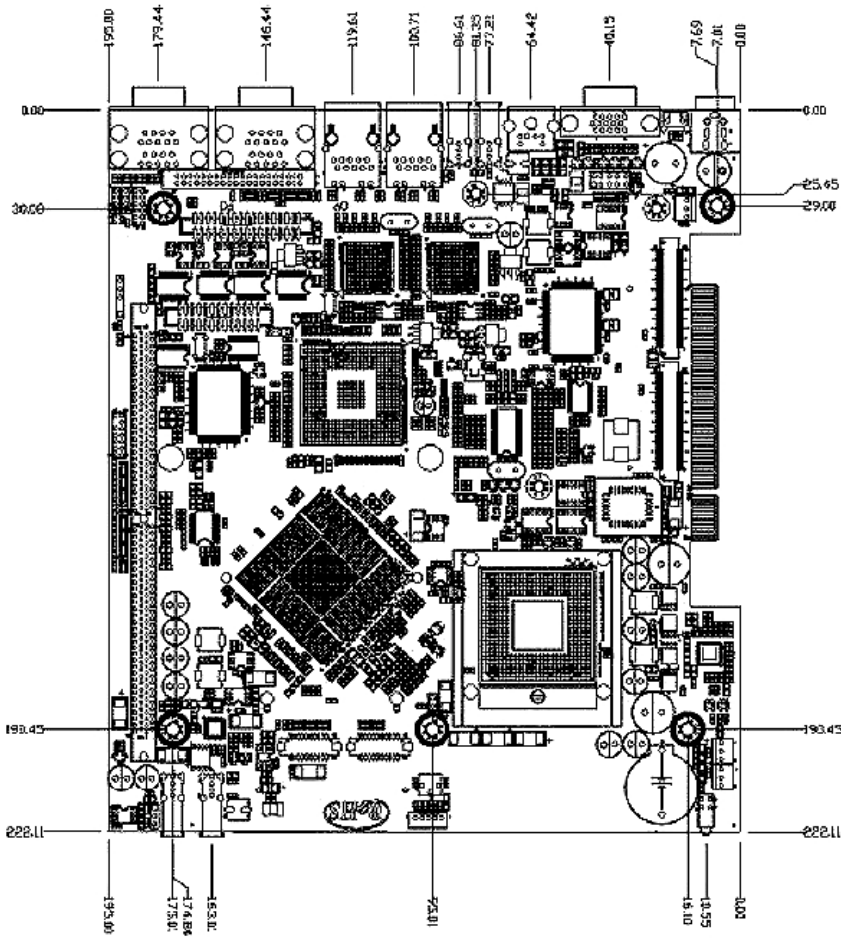




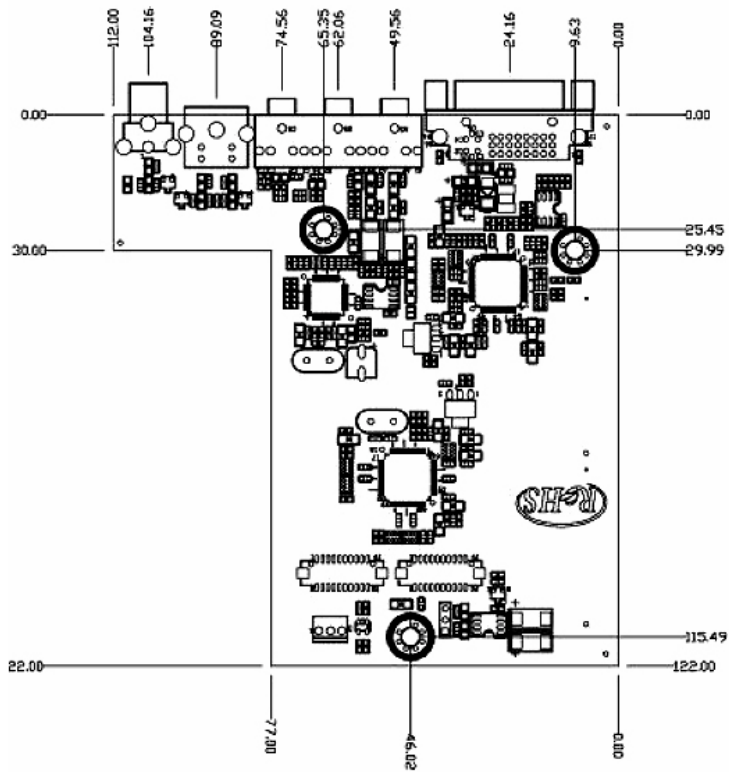
## 1-5 MB-73180 SBC



## 1-6 MB-73180 SBC Dimensions



## MIO Module Dimensions (mm)



## Chapter 2 Connector/Jumper Setting

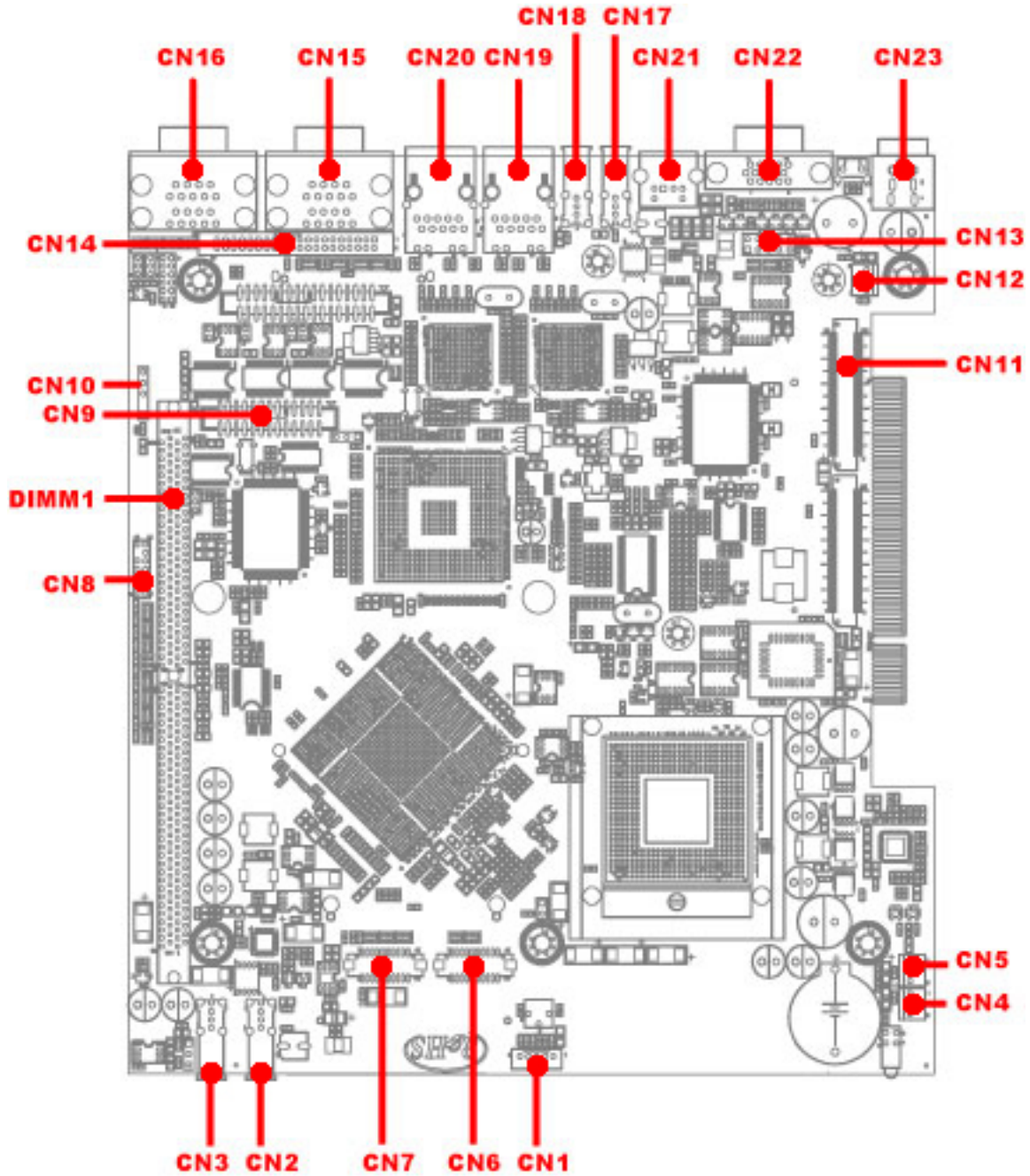
### 2-1 List of Connectors and Jumper settings for the MB-73180 board

Item	Description	Item	Description
CN1	LVDS Inverter Connector	CN2	USB Connector
CN3	USB Connector	CN4	FAN Connector
CN5	FAN Connector	CN6	LVDS Connector Pair 2
CN7	LVDS Connector Pair 1	CN8	Port 80
CN9	Printer Port Pin Header	CN10	IR Port Pin Header
CN11	MIO Connector	CN12	FAN Connector
CN13	GPIO Pin Header	CN14	Quartic Serial Port
CN15	Dual RS232 Connector	CN16	Dual RS232C Connector
CN17	USB Connector	CN18	USB Connector
CN19	RJ45 Ethernet Connector	CN20	RJ45 Ethernet Connector
CN21	PS/2 KB/MS Connector	CN22	VGA Connector
CN23	Power Jack	CN24	Mini PCI Slot
CN25	STAT Connector	CF1	CF Socket
DIMM1	DDR II DIMM socket		
JP1	LVDS inverter Voltage Select	JP2	CF Socket Select
JP4	Clear CMOS		
JP9	Serial Port Configuration	JP10	COM Port Select
JP11	422/485TX_EN	JP12	422RX_EN

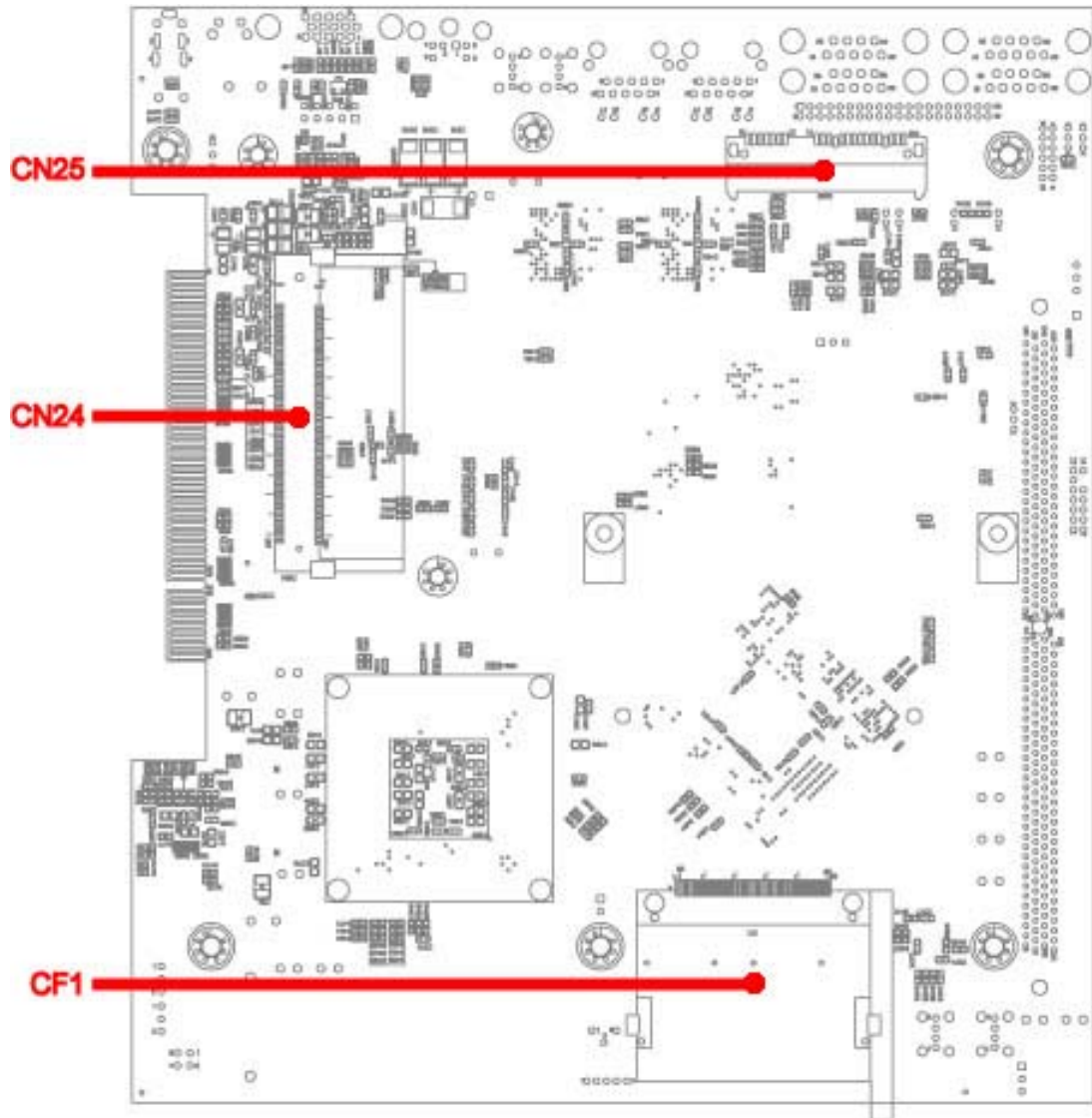
### 2-2 List of Connectors and Jumpers for the R093A MIO Module

Item	Description	Item	Description
CN1	FAN Connector	CN2	LVDS Connector Pair 1
CN3	LVDS Connector Pair 2	CN4	Audio Jack
CN5	S-Video	CN6	Composite Video
CN7	DVI Connector	JP1	LVDS inverter Voltage Select

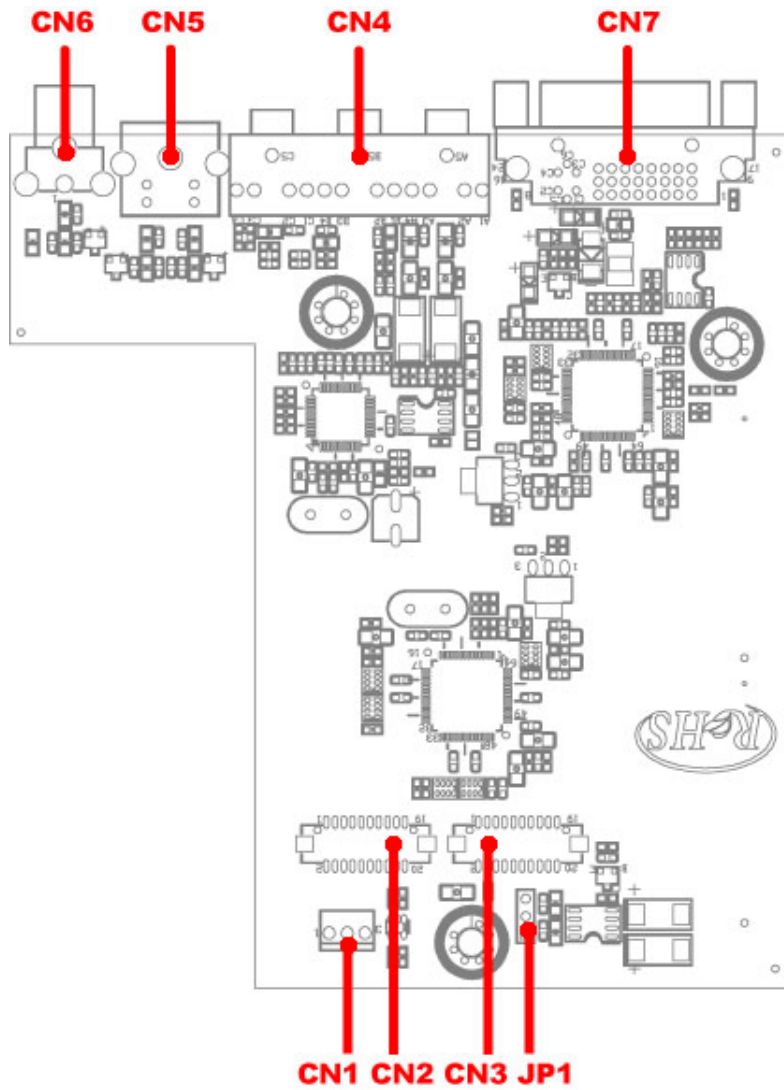
## 2-3 Location of Connectors and Jumpers



(Component Side)

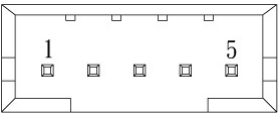


(Solder Side)

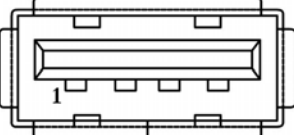


## 2-4 Connector Pin Assignments

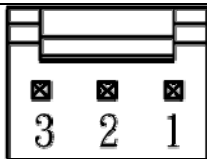
### CN1: LVDS Inverter Connector/Panel Voltage Connector

	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Pin</th> <th>Assignment</th> <th>Pin</th> <th>Assignment</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>+12V</td> <td>4</td> <td>VR; Backlight Adjust</td> </tr> <tr> <td>2</td> <td>Ground</td> <td>5</td> <td>+5V</td> </tr> <tr> <td>3</td> <td>LBKLT_CTRL</td> <td></td> <td></td> </tr> </tbody> </table>	Pin	Assignment	Pin	Assignment	1	+12V	4	VR; Backlight Adjust	2	Ground	5	+5V	3	LBKLT_CTRL		
Pin	Assignment	Pin	Assignment														
1	+12V	4	VR; Backlight Adjust														
2	Ground	5	+5V														
3	LBKLT_CTRL																

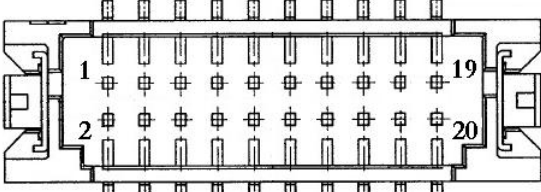
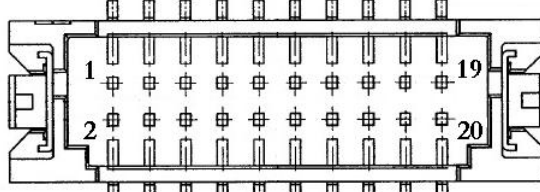
### CN2, CN3, CN17, CN18: USB Connector

	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Pin</th> <th>Assignment</th> <th>Pin</th> <th>Assignment</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>5VUSB0</td> <td>3</td> <td>USBDT0+</td> </tr> <tr> <td>2</td> <td>USBDT0-</td> <td>4</td> <td>Ground</td> </tr> </tbody> </table>	Pin	Assignment	Pin	Assignment	1	5VUSB0	3	USBDT0+	2	USBDT0-	4	Ground
Pin	Assignment	Pin	Assignment										
1	5VUSB0	3	USBDT0+										
2	USBDT0-	4	Ground										

### CN4, CN5, CN12 & CN1 on R093A(MIO): FAN Connector

	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Pin</th> <th>Assignment</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Ground</td> </tr> <tr> <td>2</td> <td>+12V</td> </tr> <tr> <td>3</td> <td>Sense</td> </tr> </tbody> </table>	Pin	Assignment	1	Ground	2	+12V	3	Sense
Pin	Assignment								
1	Ground								
2	+12V								
3	Sense								

### CN6, CN7; CN2 & CN3 on R093A(MIO): LVDS Connector

																																																																																																	
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="4">LVDS Connector pair 2</th> </tr> <tr> <th>Pin</th> <th>Assignment</th> <th>Pin</th> <th>Assignment</th> </tr> </thead> <tbody> <tr><td>1</td><td>RxEIN0-</td><td>2</td><td>RxEIN0+</td></tr> <tr><td>3</td><td>GND</td><td>4</td><td>RxEIN1-</td></tr> <tr><td>5</td><td>RxEIN1+</td><td>6</td><td>GND</td></tr> <tr><td>7</td><td>RxEIN2-</td><td>8</td><td>RxEIN2+</td></tr> <tr><td>9</td><td>RxECLKIN-</td><td>10</td><td>RxECLKIN+</td></tr> <tr><td>11</td><td>NC</td><td>12</td><td>NC</td></tr> <tr><td>13</td><td>GND</td><td>14</td><td>GND</td></tr> <tr><td>15</td><td>BLK_EN</td><td>16</td><td>NC</td></tr> <tr><td>17</td><td>GND</td><td>18</td><td>GND</td></tr> <tr><td>19</td><td>NC</td><td>20</td><td>NC</td></tr> </tbody> </table>	LVDS Connector pair 2				Pin	Assignment	Pin	Assignment	1	RxEIN0-	2	RxEIN0+	3	GND	4	RxEIN1-	5	RxEIN1+	6	GND	7	RxEIN2-	8	RxEIN2+	9	RxECLKIN-	10	RxECLKIN+	11	NC	12	NC	13	GND	14	GND	15	BLK_EN	16	NC	17	GND	18	GND	19	NC	20	NC	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="4">LVDS Connector pair 1</th> </tr> <tr> <th>Pin</th> <th>Assignment</th> <th>Pin</th> <th>Assignment</th> </tr> </thead> <tbody> <tr><td>1</td><td>VCC</td><td>2</td><td>VCC</td></tr> <tr><td>3</td><td>GND</td><td>4</td><td>GND</td></tr> <tr><td>5</td><td>RxOIN0-</td><td>6</td><td>RxOIN0+</td></tr> <tr><td>7</td><td>GND</td><td>8</td><td>RxOIN1-</td></tr> <tr><td>9</td><td>RxOIN1+</td><td>10</td><td>GND</td></tr> <tr><td>11</td><td>RxOIN2-</td><td>12</td><td>RxOIN2+</td></tr> <tr><td>13</td><td>GND</td><td>14</td><td>RxOCLKIN-</td></tr> <tr><td>15</td><td>RxOCLKIN+</td><td>16</td><td>GND</td></tr> <tr><td>17</td><td>NC</td><td>18</td><td>NC</td></tr> <tr><td>19</td><td>LVDS_DATA</td><td>20</td><td>LVDS_CLK</td></tr> </tbody> </table>	LVDS Connector pair 1				Pin	Assignment	Pin	Assignment	1	VCC	2	VCC	3	GND	4	GND	5	RxOIN0-	6	RxOIN0+	7	GND	8	RxOIN1-	9	RxOIN1+	10	GND	11	RxOIN2-	12	RxOIN2+	13	GND	14	RxOCLKIN-	15	RxOCLKIN+	16	GND	17	NC	18	NC	19	LVDS_DATA	20	LVDS_CLK
LVDS Connector pair 2																																																																																																	
Pin	Assignment	Pin	Assignment																																																																																														
1	RxEIN0-	2	RxEIN0+																																																																																														
3	GND	4	RxEIN1-																																																																																														
5	RxEIN1+	6	GND																																																																																														
7	RxEIN2-	8	RxEIN2+																																																																																														
9	RxECLKIN-	10	RxECLKIN+																																																																																														
11	NC	12	NC																																																																																														
13	GND	14	GND																																																																																														
15	BLK_EN	16	NC																																																																																														
17	GND	18	GND																																																																																														
19	NC	20	NC																																																																																														
LVDS Connector pair 1																																																																																																	
Pin	Assignment	Pin	Assignment																																																																																														
1	VCC	2	VCC																																																																																														
3	GND	4	GND																																																																																														
5	RxOIN0-	6	RxOIN0+																																																																																														
7	GND	8	RxOIN1-																																																																																														
9	RxOIN1+	10	GND																																																																																														
11	RxOIN2-	12	RxOIN2+																																																																																														
13	GND	14	RxOCLKIN-																																																																																														
15	RxOCLKIN+	16	GND																																																																																														
17	NC	18	NC																																																																																														
19	LVDS_DATA	20	LVDS_CLK																																																																																														



### CN8: PORT80 pin header

	Pin	Assignment	Pin	Assignment
	1	VCC+3.3V	2	LPC_AD0
	3	LPC_AD1	4	LPC_AD2
	5	LPC_AD3	6	LPC_FRAME#
	7	PLT_RST#	8	VCC+5V
	9	CLK_SIO1PCI	10	LPC_PME#
	11	Ground	12	NC
	13	SERIRQ	14	LDRQ#0

### CN9: Printer Port Pin Header/LPT Connector

Pin	Assignment	Pin	Assignment
1	PT_STB#	14	PTAFD#
2	PT_D0	15	PTERROR#
3	PT_D1	16	PTINT#
4	PT_D2	17	PTSLIN#
5	PT_D3	18	Ground
6	PT_D4	19	Ground
7	PT_D5	20	Ground
8	PT_D6	21	Ground
9	PT_D7	22	Ground
10	PTACK#	23	Ground
11	PTBUSY	24	Ground
12	PTPE	25	Ground
13	PTSLCT	26	Ground

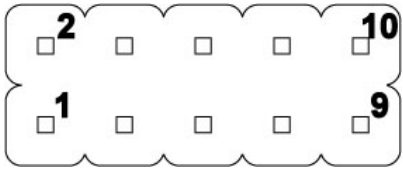
### CN10: IR Port pin header

	Pin	Assignment
	1	Vcc
	2	Key Pin
	3	IR Receiver
	4	Ground
5	IR Transmitter	

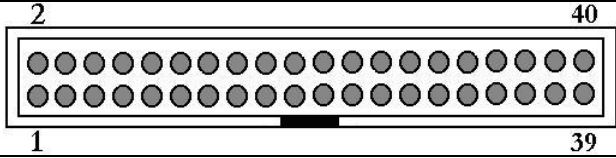
The IR is a special serial interface for wireless and remote connection. It's setup by the BIOS SETUP UTILITY on SuperIO Configuration section. Use the 'OnBoard CIR Port' to setup the

IR interface.

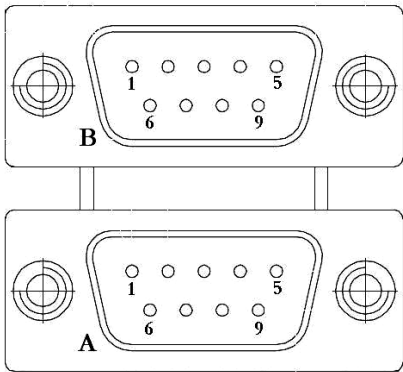
### CN13: GPIO Pin Header

	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Pin</th> <th>Assignment</th> <th>Pin</th> <th>Assignment</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>GPII0</td> <td>2</td> <td>GPO4</td> </tr> <tr> <td>3</td> <td>GPII1</td> <td>4</td> <td>GPO5</td> </tr> <tr> <td>5</td> <td>GPII2</td> <td>6</td> <td>GPO6</td> </tr> <tr> <td>7</td> <td>GPII3</td> <td>8</td> <td>GPO7</td> </tr> <tr> <td>9</td> <td>GND</td> <td>10</td> <td>VCC</td> </tr> </tbody> </table>	Pin	Assignment	Pin	Assignment	1	GPII0	2	GPO4	3	GPII1	4	GPO5	5	GPII2	6	GPO6	7	GPII3	8	GPO7	9	GND	10	VCC
Pin	Assignment	Pin	Assignment																						
1	GPII0	2	GPO4																						
3	GPII1	4	GPO5																						
5	GPII2	6	GPO6																						
7	GPII3	8	GPO7																						
9	GND	10	VCC																						

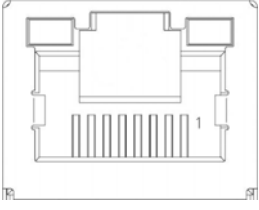
### CN14: Serial Ports Pin header

							
Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment
1	NDCD#1	11	COM2_PIN1	21	NDCD#3	31	NDCD#4
2	NDSR#1	12	COM2_PIN2	22	NDSR#3	32	NDSR#4
3	NRXD1	13	COM2_PIN3	23	NRXD	33	NRXD4
4	R_NRTS#1	14	COM2_PIN4	24	R_NRTS#3	34	R_NRTS#4
5	R_NTXD1	15	COM2_PIN5	25	R_NTXD3	35	R_NTXD4
6	NCTS#1	16	COM2_PIN6	26	NCTS#3	36	NCTS#4
7	R_NDTR#1	17	COM2_PIN7	27	R_NDTR#3	37	R_NDTR#4
8	NRI#1	18	COM2_PIN8	28	NRI#3	38	NRI#4
9	Ground	19	Ground	29	Ground	39	Ground
10	N/C	20	N/C	30	N/C	40	N/C

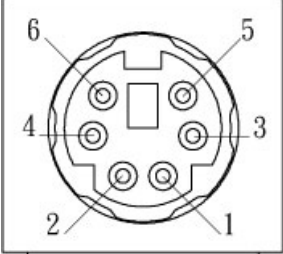
### CN15, CN16: Dual Serial/COM port

	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Pin</th> <th>Assignment</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>DCD</td> </tr> <tr> <td>2</td> <td>RXD</td> </tr> <tr> <td>3</td> <td>TXD</td> </tr> <tr> <td>4</td> <td>DTR</td> </tr> <tr> <td>5</td> <td>Ground</td> </tr> <tr> <td>6</td> <td>DSR</td> </tr> <tr> <td>7</td> <td>RTS</td> </tr> <tr> <td>8</td> <td>CTS</td> </tr> <tr> <td>9</td> <td>RI</td> </tr> </tbody> </table>	Pin	Assignment	1	DCD	2	RXD	3	TXD	4	DTR	5	Ground	6	DSR	7	RTS	8	CTS	9	RI
Pin	Assignment																				
1	DCD																				
2	RXD																				
3	TXD																				
4	DTR																				
5	Ground																				
6	DSR																				
7	RTS																				
8	CTS																				
9	RI																				

## CN19, CN20: RJ45 Ethernet Connector

	Pin	Assignment
	1	TX+
	2	TX-
	3	RX+
	4	Ground
	5	Ground
	6	RX-
	7	Ground
8	Ground	

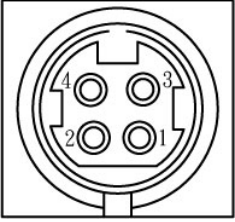
## CN21: PS/2 KB/MS Connector

	Pin	Assignment
	1	Data
	2	NC
	3	Ground
	4	+5V
	5	Clock
6	NC	

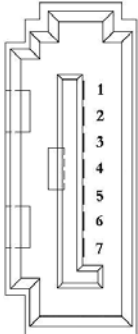
## CN22: VGA Connector

	Pin	Assignment	Pin	Assignment	Pin	Assignment
	1	Red	6	Ground	11	MONID1
	2	Green	7	Ground	12	DDC Data
	3	Blue	8	Ground	13	H-Sync
	4	MONID0	9	+5V	14	V-Sync
	5	Ground	10	Ground	15	DDC Clock

## CN23: Power Jack

	Pin	Assignment
	1	+12V
	2	+12V
	3	Ground
4	Ground	

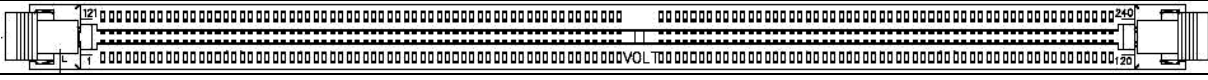
## CN25: STAT Connector

	Pin	Assignment
	1	Ground
	2	TXP
	3	TXN
	4	Ground
	5	RXN
	6	RXP
7	Ground	

## CNF1: CF Interface

Pin	Assignment	Pin	Assignment
1	Ground	26	NC
2	D03	27	D11
3	D04	28	D12
4	D05	29	D13
5	D06	30	D14
6	D07	31	D15
7	CS	32	CS
8	Ground	33	NC
9	Ground	34	IOR
10	Ground	35	IOW
11	Ground	36	WE
12	Ground	37	RDY/BSY
13	VCC	38	VCC
14	Ground	39	SCSE
15	Ground	40	NC
16	Ground	41	RESET
17	Ground	42	ORDY
18	A02	43	DREG
19	A01	44	DACK
20	A00	45	LED
21	D00	46	BVD
22	D01	47	D08
23	D02	48	D09
24	WP	49	D10
25	NC	50	Ground

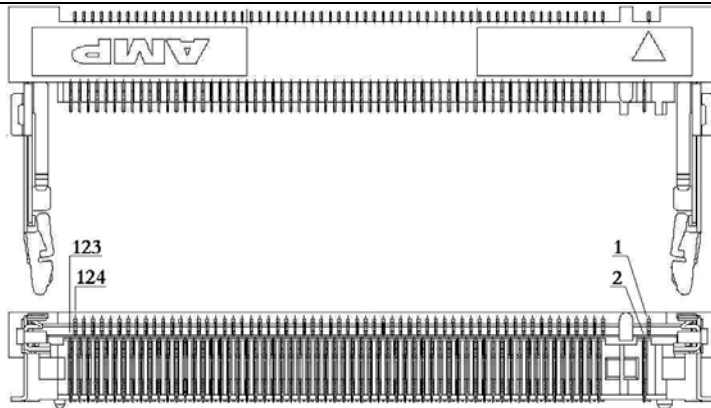
## DIMM1: DDR II DIMM Socket



Front					Back						
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	41	VSS	81	DQ33	121	VSS	161	CB4	201	VSS
2	VSS	42	CB0	82	VSS	122	DQ4	162	CB5	202	DM4/DQS13
3	DQ0	43	CB1	83	DQS4#	123	DQ5	163	VSS	203	NC/DQS13#
4	DQ1	44	VSS	84	DQS4	124	VSS	164	DM8/DQS17	204	VSS
5	VSS	45	DQS8#	85	VSS	125	DM0/DQS9	165	NC/DQS17#	205	DQ38
6	DQS0#	46	DQS8	86	DQ34	126	NC/DQS9#	166	VSS	206	DQ39
7	DQS0	47	VSS	87	DQ35	127	VSS	167	CB6	207	VSS
8	VSS	48	CB2	88	VSS	128	DQ6	168	CB7	208	DQ44
9	DQ2	49	CB3	89	DQ40	129	DQ7	169	VSS	209	DQ45
10	DQ3	50	VSS	90	DQ41	130	VSS	170	VDDQ	210	VSS
11	VSS	51	VDDQ	91	VSS	131	DQ12	171	CKE1	211	DM5/DQS14
12	DQ8	52	CKE0	92	DQS5#	132	DQ13	172	VDD	212	NC/DQS14#
13	DQ9	53	VDD	93	DQS5	133	VSS	173	NC	213	VSS
14	VSS	54	NC/BA2	94	VSS	134	DM1/DQS10	174	NC	214	DQ46
15	DQS1#	55	ERR_OUT	95	DQ42	135	NC/DQS10#	175	VDDQ	215	DQ47
16	DQS1	56	VDDQ	96	DQ43	136	VSS	176	A12	216	VSS
17	VSS	57	A11	97	VSS	137	RFU	177	A9	217	DQ52
18	RESET#	58	A7	98	DQ48	138	RFU	178	VDD	218	DQ53
19	NC	59	VDD	99	DQ49	139	VSS	179	A8	219	VSS
20	VSS	60	A5	100	VSS	140	DQ14	180	A6	220	RFU
21	DQ10	61	A4	101	SA2	141	DQ15	181	VDDQ	221	RFU
22	DQ11	62	VDDQ	102	NC	142	VSS	182	A3	222	VSS
23	VSS	63	A2	103	VSS	143	DQ20	183	A1	223	DM6/DQS15
24	DQ16	64	VDD	104	DQS6#	144	DQ21	184	VDD	224	NC/DQS15#
25	DQ17	65	VSS	105	DQS6	145	VSS	185	CK0	225	VSS
26	VSS	66	VSS	106	VSS	146	DM2/DQS11	186	CK0#	226	DQ54
27	DQS2#	67	VDD	107	DQ50	147	NC/DQS11#	187	VDD	227	DQ55
28	DQS2	68	PAR_IN	108	DQ51	148	VSS	188	A0	228	VSS
29	VSS	69	VDD	109	VSS	149	DQ22	189	VDD	229	DQ60
30	DQ18	70	A10/AP	110	DQ56	150	DQ23	190	BA1	230	DQ61
31	DQ19	71	BA0	111	DQ57	151	VSS	191	VDDQ	231	VSS
32	VSS	72	VDDQ	112	VSS	152	DQ28	192	RAS#	232	DM7/DQS16
33	DQ24	73	WE#	113	DQS7#	153	DQ29	193	S0#	233	NC/DQS16#
34	DQ25	74	CAS#	114	DQS7	154	VSS	194	VDDQ	234	VSS
35	VSS	75	VDDQ	115	VSS	155	DM3/DQS12	195	ODT0	235	DQ62
36	DQS3#	76	S1#	116	DQ58	156	NC/DQS12#	196	NC/A13	236	DQ63
37	DQS3	77	ODT1	117	DQ59	157	VSS	197	VDD	237	VSS
38	VSS	78	VDDQ	118	VSS	158	DQ30	198	VSS	238	VDDSPD
39	DQ26	79	VSS	119	SDA	159	DQ31	199	DQ36	239	SA0
40	DQ27	80	DQ32	120	SCL	160	VSS	200	DQ37	240	SA1

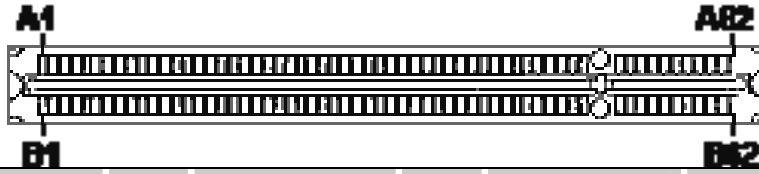
*Caution: When the board operates under 667MHz, the DIMM module shouldn't be the double side rank.*

## CN24: Mini PCI Slot



Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment
1	TIP	32	GROUND	63	3.3V	94	AD[02]
2	RING	33	AD[31]	64	FRAME#	95	AD[03]
3	8PMJ-3	34	PME#	65	CLKRUN#	96	AD[00]
4	8PMJ-1	35	AD[29]	66	TRDY#	97	5V
5	8PMJ-6	36	RESERVED	67	SERR#	98	RESERVED_WIP5
6	8PMJ-2	37	GROUND	68	STOP#	99	AD[01]
7	8PMJ-7	38	AD[30]	69	GROUND	100	RESERVED_WIP5
8	8PMJ-4	39	AD[27]	70	3.3V	101	GROUND
9	8PMJ-8	40	3.3V	71	PERR#	102	GROUND
10	8PMJ-5	41	AD[25]	72	DEVSEL#	103	AC_SYNC
11	LED1_GRNP	42	AD[28]	73	C/BE[1]#	104	M66EN
12	LED2_YELP	43	RESERVED	74	GROUND	105	AC_SDATA_IN
13	LED1_GRNN	44	AD[26]	75	AD[14]	106	AC_SDATA_OUT
14	LED2_YELN	45	C/BE[3]#	76	AD[15]	107	AC_BIT_CLK
15	CHSGND	46	AD[24]	77	GROUND	108	AC_CODEC_ID0#
16	RESERVED	47	AD[23]	78	AD[13]	109	AC_CODEC_ID1#
17	INTB#	48	IDSEL	79	AD[12]	110	AC_RESET#
18	5V	49	GROUND	80	AD[11]	111	MOD_AUDIO_MON
19	3.3V	50	GROUND	81	AD[10]	112	RESERVED
20	INTA#	51	AD[21]	82	GROUND	113	AUDIO_GND
21	RESERVED	52	AD[22]	83	GROUND	114	GROUND
22	RESERVED	53	AD[19]	84	AD[09]	115	SYS_AUDIO_OUT
23	GROUND	54	AD[20]	85	AD[08]	116	SYS_AUDIO_IN
24	3.3VAUX	55	GROUND	86	C/BE[0]#	117	SYS_AUDIO_OUT GND
25	CLK	56	PAR	87	AD[07]	118	SYS_AUDIO_IN GND
26	RST#	57	AD[17]	88	3.3V	119	AUDIO_GND
27	GROUND	58	AD[18]	89	3.3V	120	AUDIO_GND
28	3.3V	59	C/BE[2]#	90	AD[06]	121	RESERVED
29	REQ#	60	AD[16]	91	AD[05]	122	MPCIACT#
30	GNT#	61	IRDY#	92	AD[04]	123	VCC5VA
31	3.3V	62	Ground	93	RESERVED	124	3.3VAUX

## PCI1: PCI Slot



Pin	Assignment	Pin	Assignment	Pin	Assignment	Pin	Assignment
A1	TRST	A32	AD16	B1	-12V	B32	AD17
A2	+12V	A33	+3.3V05	B2	TCK	B33	C/BE2
A3	TMS	A34	FRAME	B3	GND	B34	GND13
A4	TDI	A35	GND14	B4	TDO	B35	IRDY
A5	+5V	A36	TRDY	B5	+5V	B36	+3.3V06
A6	INTA	A37	GND15	B6	+5V	B37	DEVSEL
A7	INTC	A38	STOP	B7	INTB	B38	GND16
A8	+5V	A39	+3.3V07	B8	INTD	B39	LOCK
A9	RESV01	A40	SDONE	B9	PRSNT1	B40	PERR
A10	+5V	A41	SBO	B10	RES	B41	+3.3V08
A11	RESV03	A42	GND17	B11	PRSNT2	B42	SERR
A12	GND03	A43	PAR	B12	GND	B43	+3.3V09
A13	GND05	A44	AD15	B13	GND	B44	C/BE1
A14	RESV05	A45	+3.3V10	B14	RES	B45	AD14
A15	RESET	A46	AD13	B15	GND	B46	GND18
A16	+5V	A47	AD11	B16	CLK	B47	AD12
A17	GNT	A48	GND19	B17	GND	B48	AD10
A18	GND08	A49	AD9	B18	REQ	B49	GND20
A19	RESV06			B19	+5V	B50	(OPEN)
A20	AD30			B20	AD31	B51	(OPEN)
A21	+3.3V01	A52	C/BE0	B21	AD29	B52	AD8
A22	AD28	A53	+3.3V11	B22	GND	B53	AD7
A23	AD26	A54	AD6	B23	AD27	B54	+3.3V12
A24	GND10	A55	AD4	B24	AD25	B55	AD5

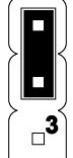

## User's Manual

A25	AD24	A56	GND21	B25	+3.3V	B56	AD3
A26	IDSEL	A57	AD2	B26	C/BE3	B57	GND22
A27	+3.3V03	A58	AD0	B27	AD23	B58	AD1
A28	AD22	A59	+5V	B28	GND	B59	VCC08
A29	AD20	A60	REQ64	B29	AD21	B60	ACK64
A30	GND12	A61	VCC11	B30	AD19	B61	VCC10
A31	AD18	A62	VCC13	B31	+3.3V	B62	VCC12

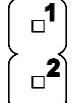
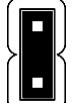


## 2-5 Jumper Setting



### JP1: LVDS inverter Voltage Select

	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Assignment</th> </tr> </thead> <tbody> <tr> <td>1-2 close</td> <td>+3.3V</td> </tr> <tr> <td>2-3 close</td> <td>+5V</td> </tr> </tbody> </table>	Status	Assignment	1-2 close	+3.3V	2-3 close	+5V	
Status	Assignment							
1-2 close	+3.3V							
2-3 close	+5V							

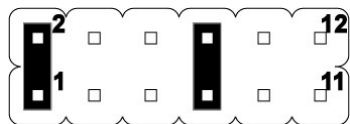
### JP2: CF Select

<b>OPEN</b> 	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Assignment</th> </tr> </thead> <tbody> <tr> <td>Close</td> <td>Slave</td> </tr> <tr> <td>Open</td> <td>Master</td> </tr> </tbody> </table>	Status	Assignment	Close	Slave	Open	Master	 <b>Close</b>
Status	Assignment							
Close	Slave							
Open	Master							

### JP4: Clear CMOS

	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Assignment</th> </tr> </thead> <tbody> <tr> <td>1-2 close</td> <td>Keep CMOS</td> </tr> <tr> <td>2-3 close</td> <td>Clear CMOS</td> </tr> </tbody> </table>	Status	Assignment	1-2 close	Keep CMOS	2-3 close	Clear CMOS	
Status	Assignment							
1-2 close	Keep CMOS							
2-3 close	Clear CMOS							

### JP10: COM Port Select (Fixed Default Setting)

	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">Pin</th> <th style="background-color: #cccccc;">Assignment</th> </tr> </thead> <tbody> <tr> <td>1-2</td> <td>Close</td> </tr> <tr> <td>7-8</td> <td>Close</td> </tr> </tbody> </table>	Pin	Assignment	1-2	Close	7-8	Close
Pin	Assignment						
1-2	Close						
7-8	Close						

## JP9, JP11, JP12: RS232/422/485 selector for the CN16 B connector

Jumper				
JP9				
Pin	Assignment			
	RS232	RS422	RS485(2 wire)	RS485(4 wire)
1	DCD	TX-	TX-/RX-	TX-
2	RXD	TX+	TX+/RX+	TX+
3	TXD	RX+		RX+
4	DTR	RX-		RX-
5	GND	GND	GND	GND
6	DSR	RTS-		
7	RTS	RTS+		
8	CTS	CTS+		
9	RI	CTS-		
10	NC	NC		

## 3-0 Cooling Considerations

### 3-1 Proper Cooling

The PL-60590 is designed to operate fanlessly and without moving parts whilst still allowing safe cooling for the internal components, however, the following considerations and requirements **must** be observed to ensure warranty viability and safe operation.

#### **It is up to the integrator to house this devices in it's proper location.**

The processor of the PL-60590 is thermally connected to the top cover, and thus the surrounding "skin" of the chassis. Once the CPU reaches its optimum operating peaks in terms of performance, the thermals of the chassis will rise accordingly.

It is recommended that you monitor the thermal properties of the chassis as the skin may rise to an uncomfortably hot temperature, depending on CPU type, and usage, the external area of the chassis can reach up to ~55C! (131F) and be quite painful to the touch. The following rules for safe operation should be considered:

#### • **EXTERNAL TEMPERATURE MONITORING**

Monitoring the surface ("skin") temperature of the unit, at least before handling, is recommended, though not required.

#### • **INTERNAL TEMPERATURE MONITORING**

Due to the fanless nature of this device, components can reach very high temperatures easily. The BIOS is set to monitor CPU and ambient system temperatures. These should stay below 80C for maximum CPU life.

Monitoring system temperatures is good practice for any industrial or business PC.

#### **The nature of the PL-6059A/B's operation is such that component temperature monitoring is HIGHLY recommended.**

Most off-the-shelf temperature monitoring software should work with this device.

WIN does *not* provide this software.

#### • **CPU COOLING:**

The platform is designed to operate with Intel Mobile CPUs, including certain Intel® Celeron M and Core 2 Processors.

When using a processor with a TDP in excess of 25W it is recommended that you allow

proper cooling to the top of the chassis. An 80mm fan or larger rated at 20CFM (Cubic Feet per Minute) positioned to blow across the longest axis to dissipate heat rising from the cooling fins is the WIN Recommended solution.

### • **COOLING FOR STORAGE:**

Safe operating temperatures for storage (CF, HDD, SSD) will vary.

Consult the manual or website for your storage medium for safe operating temperatures.

Most magnetic HDDs will require operating temperatures to remain under 60C for safe and continuous operation. This is particularly important for fast HDDs, such as 7200rpm devices.

Most modern Hard Drives, have S.M.A.R.T. capability that allows it's temperatures to be monitored via the I2C or SMBUS. WIN recommends you make use of this feature and enable software that is capable of monitoring this. WIN does not provide this software.

Direct airflow *underneath* the chassis, across the HDD/storage location is recommended in instances of:

- Magnetic storage, especially above 7200rpm (1Amp or greater on 5V rail)
- Heavy device usage
- Higher than 25C ambient temperatures

Note: The HDD is located *under* the PL-60590 and sits nearly flush against the chassis skin. Most of the heat that will effect the HDD will come from the chassis itself. If it is being *actively* cooled and it's skin temperature remains low, additional HDD cooling (such as described above) may not be necessary.

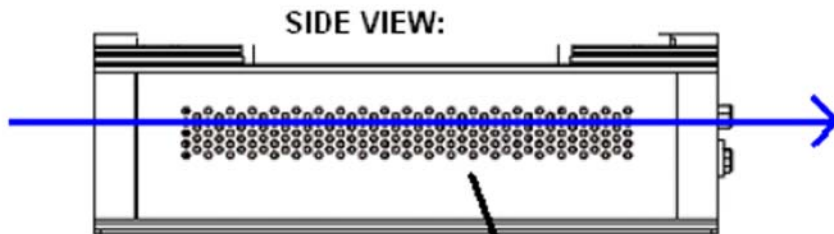
### • **COOLING FOR OPERATION IN HOT ENVIRONMENT (40C MAX)**

The PL-60590 will operate safely in environments up to 40C.

The stability and longevity of the device depends on whether or not there is sufficient airflow to dissipate the heat from the metal skin of the chassis.

Direct airflow of 20CFM is recommended *around* the chassis itself for the safest of operation. Proper airflow across, or directly into the *sides* of the unit (where the vent holes are located) is required to more easily pull the hot ambient air from within the unit and keep the ICH: 945GME. (SEE BELOW)

**NOTE: THIS IS IN ADDITION TO COOLING FOR CPU AND STORAGE, IF YOUR CPU AND STORAGE REQUIRES IT.**



**VENT HOLES TO  
DISPERSE INTERNAL HEAT**

Position external fans at the front or back of the unit or directly toward the vent holes on the side to remove stagnant air. This is required for operation of over 25°C.

## OVERALL COOLING

When operating the unit with CPUs rated for 25W or higher TDP, the unit is required to have at least ~10CFM constant airflow across the top heat-dissipating fins.

Air is best blown laterally, across the top in either direction across its longest dimension.

However an appropriate 40mm or 60mm fan attached to the top of the unit blowing downwards is also acceptable.

When using a magnetic HDD, it is recommended that ~10CFM of airflow be allowed to blow across the bottom of the chassis.

This is especially important and may be REQUIRED for 7200rpm or faster drives. Be sure to safely monitor your HDD temperatures.

In environments exceeding 25C Side-cooling, either laterally (as shown) or directly into the vents at ~10CFM is required.

###