2 chip stack 8G-Bit

W29N08GV
NAND FLASH MEMORY

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1. GENERAL DESCRIPTION

The W29N08GV (8G-bit) NAND Flash memory provides a storage solution for embedded systems with limited space, pins and power. It is ideal for code shadowing to RAM, solid state applications and storing media data such as, voice, video, text and photos. The device operates on a single 2.7V to 3.6V power supply with active current consumption as low as 25mA and 10uA for CMOS standby current.

The memory array totals 1,107,296bytes, and organized into 8,192 erasable blocks. Each block consists of 64 programmable pages of 2,112-bytes (1056 words) each. Each page consists of 2,048-bytes (1024 words) for the main data storage area and 64-bytes (32words) for the spare data area (The spare area is typically used for error management functions).

The W29N08GV is double chip stack of W29N04GV. Then, this document shows specified features, functions of W29N08GV. Detail functions, commands operation, AC, DC characteristics and restrictions refer to W29N04GV datasheet.

2. PACKAGE TYPES AND PIN CONFIGURATIONS

2.1 W29N08GVSIAA Pin assignment 48-pin TSOP1

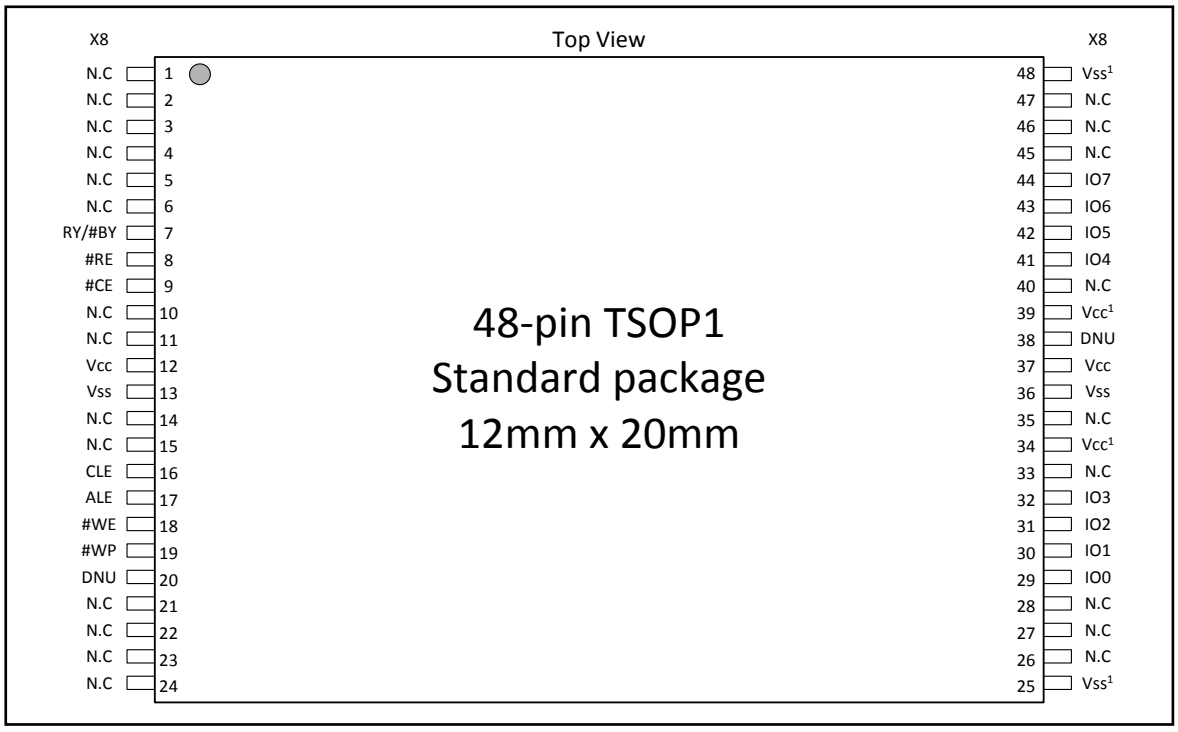


Figure 1 Pin Assignment 48-pin TSOP1 1CE Type (Package code S)

2.2 W29N08GVSIAD Pin assignment 48-pin TSOP1

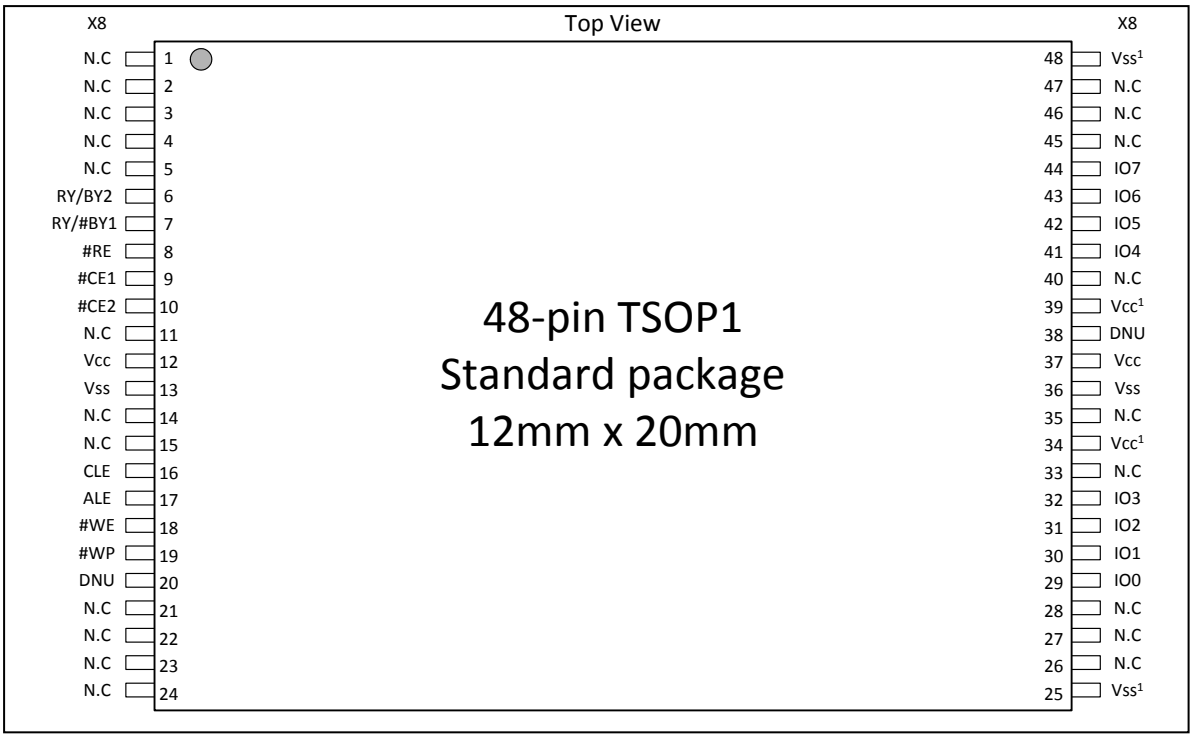


Figure 2 Pin Assignment 48-pin TSOP1 2CE Type (Package code S)

Note:

1. **These pins might not be connected in the package. Winbond recommends connecting these pins to the designed external sources for ONFI compatibility.**

2.3 W29N08GVBIAA Ball assignment 63-ball VFBGA63

Top View, ball down

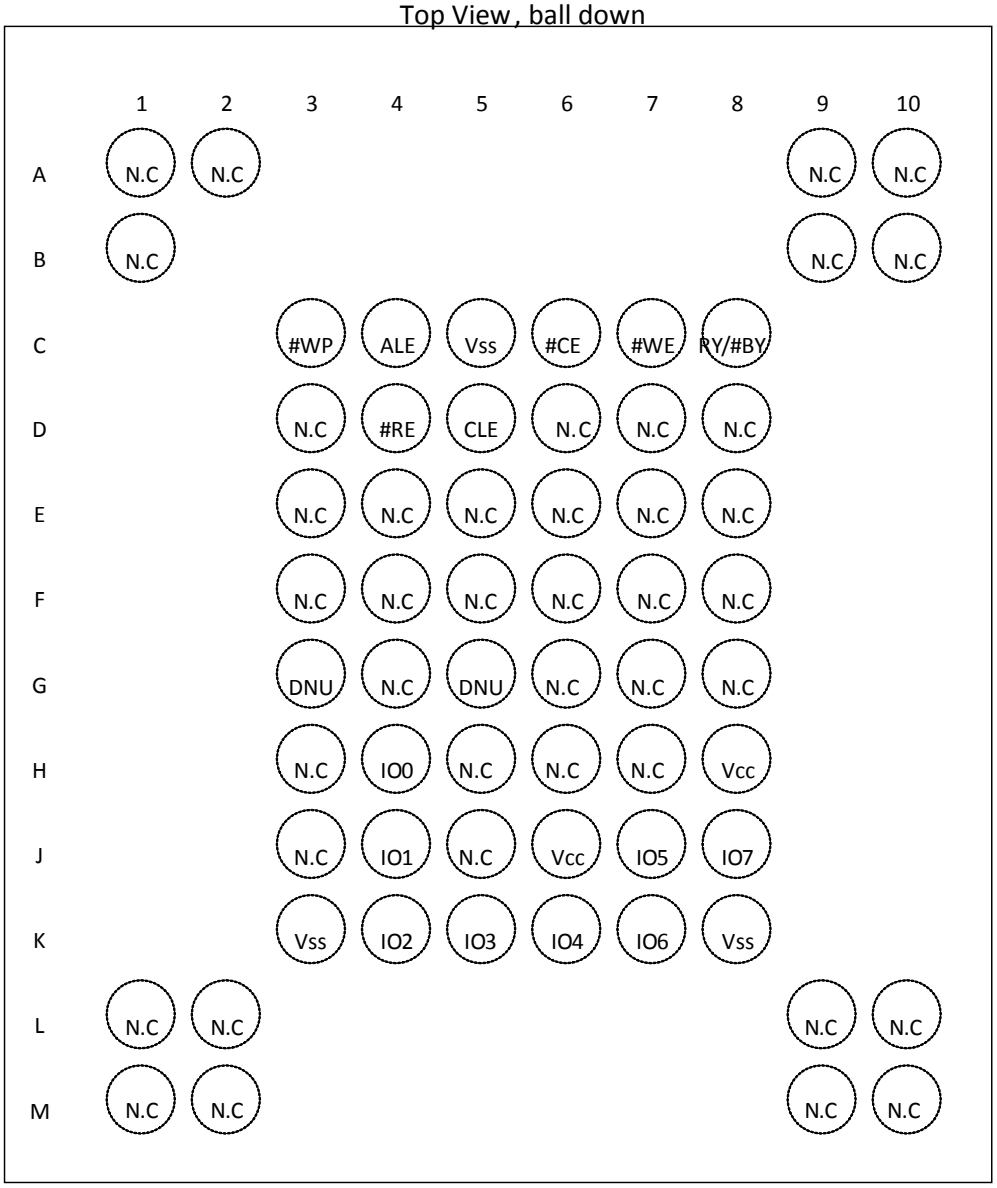


Figure 3 Ball Assignment 63-ball FBGA 1CE Type (Package code B)

2.4 W29N08GVBIAD Ball assignment 63-ball VFBGA63

Top View, ball down

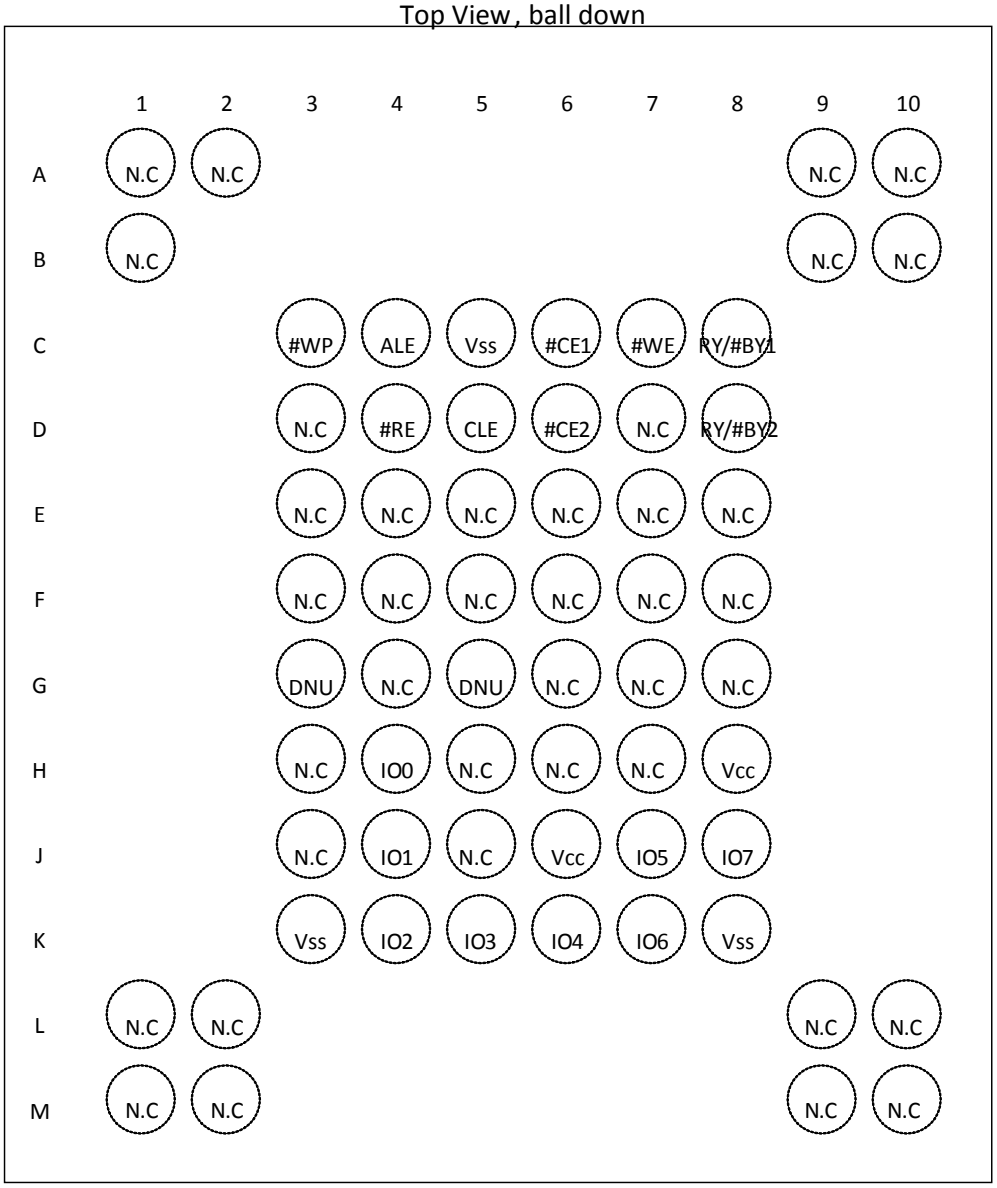


Figure 4 Ball Assignment 63-ball FBGA 2CE Type (Package code B)

3. MEMORY ARRAY ORGANIZATION

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st cycle	A7	A6	A5	A4	A3	A2	A1	A0
2nd cycle	L	L	L	L	A11	A10	A9	A8
3rd cycle	A19	A18	A17	A16	A15	A14	A13	A12
4th cycle	A27	A26	A25	A24	A23	A22	A21	A20
5th cycle	L	L	L	L	L	A30[4]	A29	A28

Table 1 Addressing

Notes:

1. **"L" indicates a low condition, which must be held during the address cycle to insure correct processing.**
2. **A0 to A11 during the 1st and 2nd cycles are column addresses. A12 to A30 during the 3rd, 4th and 5th cycles are row addresses, A18 is plane address,A19 to the last address are block addresses.**
3. **The device ignores any additional address inputs that exceed the device's requirement.**
4. **The last address of W29N08GVxIAA (8Gb-1CE type) is A30.**

4. DEVICE ID

Parts #	# of CE	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle	5th Byte/Cycle
W29N08GVxIAA	1	EFh	D3h	91h	95h	58h
W29N08GVxIAD	2	EFh	DCh	90h	95h	54h
Description		MFR ID	Device ID	Cache Programming Supported	Page Size:2KB Spare Area Size:64b BLK Size w/o Spare:128KB Organized:x8 or x16 Serial Access:25ns	

"x" means package code. S :TSOP48, B : BGA63

Table 2 Device ID and configuration codes for Address 00h

5. DC ELECTRICAL CHARACTERISTICS

5.1 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	

Sequential Read current	Icc1	tRC= tRC MIN
		#CE=VIL
		IOUT=0mA
			-	25	35	mA

Program current	Icc2	-	-	25	35	mA
Erase current	Icc3	-	-	25	35	mA
Standby current (TTL)	ISB1	#CE=VIH #WP=0V/Vcc	-	-	1	mA
Standby current (CMOS)	ISB2	#CE=Vcc – 0.2V #WP=0V/Vcc	-	20	100	µA
Input leakage current	ILI	VIN= 0 V to Vcc	-	-	±10	µA
Output leakage current	ILO	VOUT=0V to Vcc	-	-	±10	µA
Input high voltage	VIH	I/O15~0, #CE,#WE,#RE, #WP,CLE,ALE,RY/#BY,	0.8 x Vcc	-	Vcc + 0.3	V
Input low voltage	VIL	-	-0.3	-	0.2 x Vcc	V
Output high voltage(1)	VOH	IOH=-400µA	2.4	-	-	V
Output low voltage(1)	VOL	IOL=2.1mA	-	-	0.4	V
Output low current	IOL(RY/#BY)	VOL=0.4V	8	10		mA

Table 3 DC Electrical Characteristics

Note:

1. **VOH and VOL may need to be relaxed if I/O drive strength is not set to full.**
2. **IOL (RY/#BY) may need to be relaxed if RY/#BY pull-down strength is not set to full**

6. INVALID BLOCKS

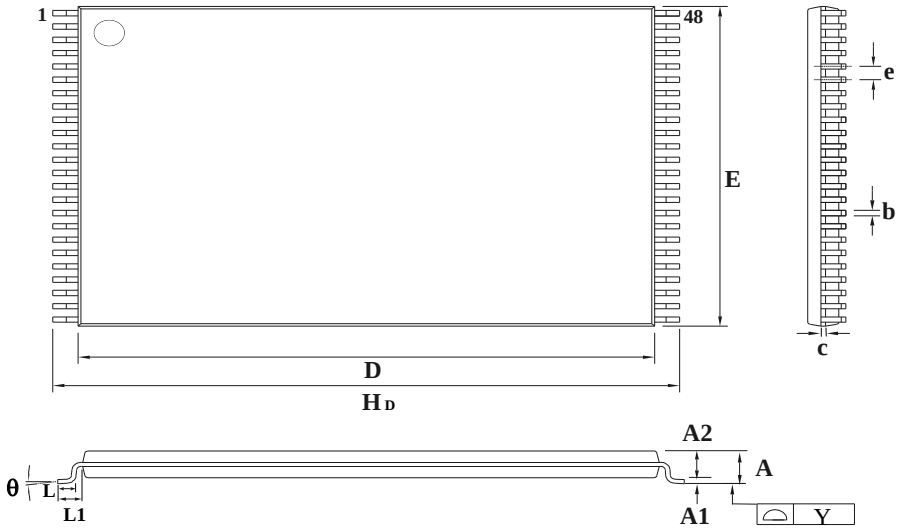
The W29N08GV may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks (See Table 5). An invalid block is defined as blocks that contain one or more bad bits. Block 0, block address 00h is guaranteed to be a valid block at the time of shipment.

Parameter	Symbol	Min	Max	Unit
Valid block number	Nvb	8032	8192	blocks

Table 4 Valid Block Number

7. PACKAGE DIMENSIONS

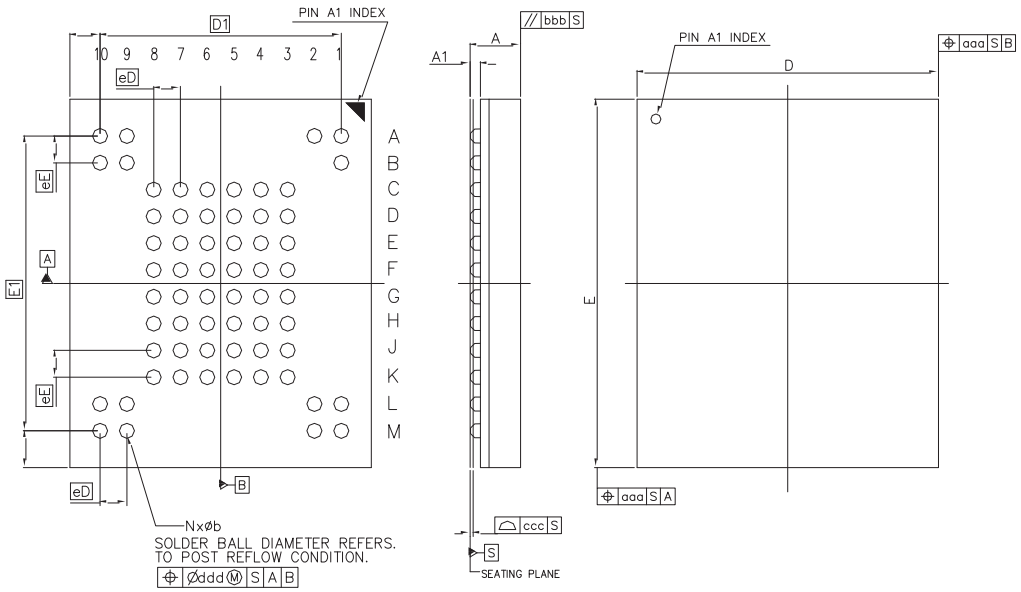
7.1 TSOP 48-pin 12x20



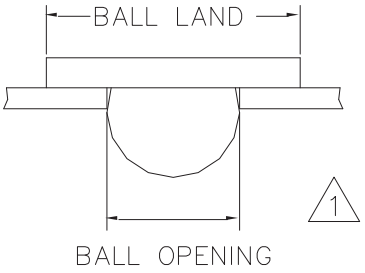
Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	—	0.002	—	—
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	18.3	18.4	18.5	0.720	0.724	0.728
H_D	19.8	20.0	20.2	0.780	0.787	0.795
E	11.9	12.0	12.1	0.468	0.472	0.476
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	—	0.21	0.004	—	0.008
e	—	0.50	—	—	0.020	—
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	—	0.80	—	—	0.031	—
Y	—	—	0.10	—	—	0.004
θ	0	—	5	0	—	5

Figure 5 TSOP 48-PIN 12X20mm

7.2 Fine-Pitch Ball Grid Array 63-ball



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	---	---	1.00
A1	0.25	---	0.40
b	0.40	0.45	0.50
D	8.90	9.00	9.10
E	10.90	11.00	11.10
D1	7.20 BSC		
E1	8.80 BSC.		
eD	0.80 BSC.		
eE	0.80 BSC.		
aaa	0.15		
bbb	--	--	0.10
ccc	--	--	0.10
ddd	--	--	0.20
N	63		



Note:
1. Ball land:0.5mm, Ball opening:0.4mm,
PCB Ball land suggested 0.4mm

Figure 6 Fine-Pitch Ball Grid Array 63-Ball

8. ORDERING INFORMATION

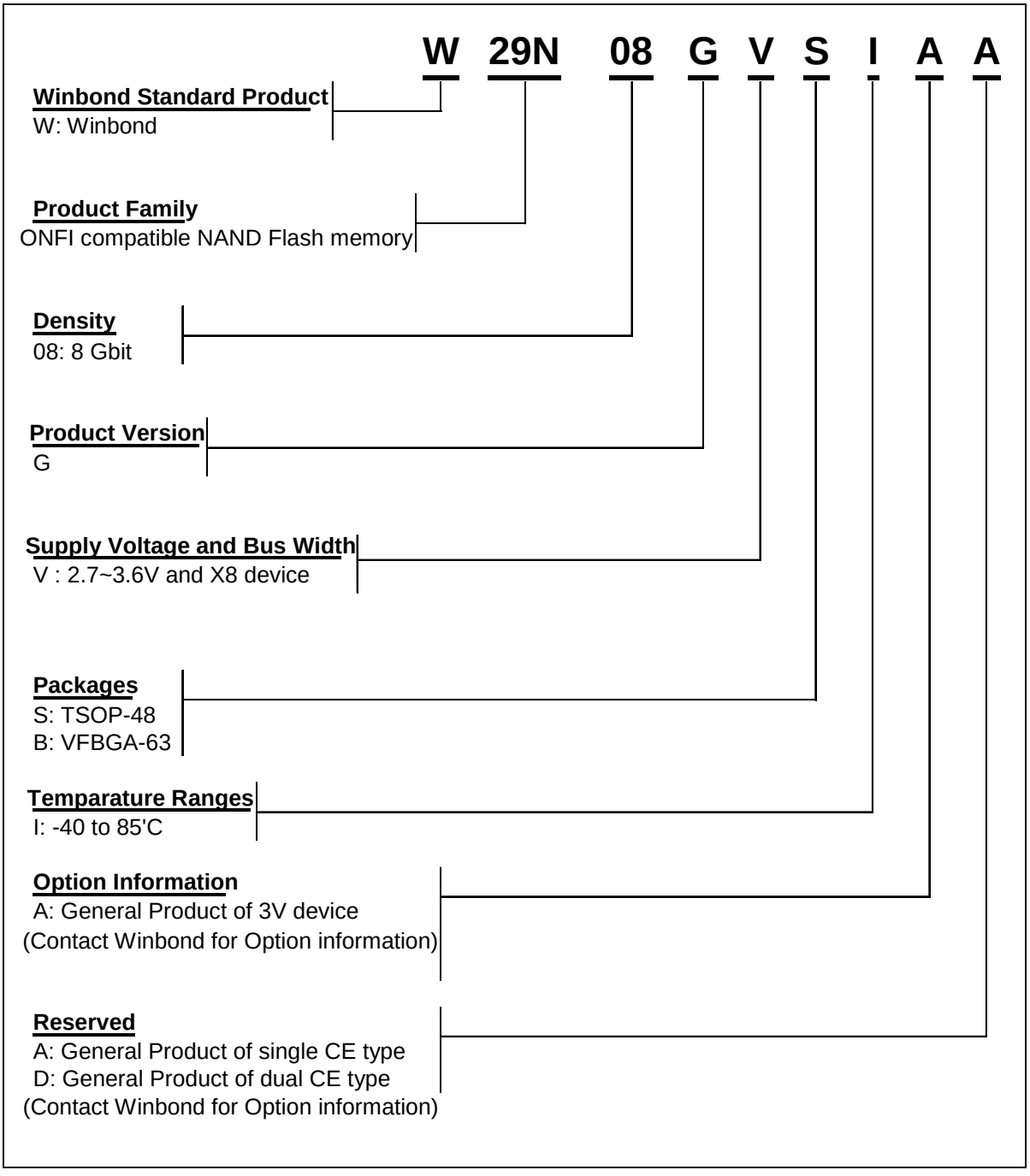


Figure 7 Ordering Part Number Description

9. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	08/26/16		New Create

Table 5 History Table

Trademarks

Winbond is trademark of *Winbond Electronics Corporation.*
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