TERASPEED® CONSULTING

SIGNAL INTEGRITY TRAINING

TERASPEED® CONSULTING, A Division of Samtec, delivers signal integrity training by professionals with years of real-life experience in the engineering and implementation of high-performance systems. We have presented at various companies and venues, to thousands of participants with resounding results.

Our classes are tailored for beginners to advanced users. Standard programs are one to three days, and custom classes may be arranged from one day to one week in duration.

Practical examples based upon actual experience are used to provide intuitive learning for both simple and advanced theoretical concepts. Participants leave our presentations with answers and new insights.

For more information on our current classes, contact us at inquire@teraspeed.com or +1-844-483-7773.

FAST EDGES
POWER & SIGNAL INTEGRITY TRAINING BY THE EXPERTS AT TERASPEED® CONSULTING

SIGNAL INTEGRITY EXPERTISE: FROM SILICON-TO-SILICON

Learn from the experts, with topics including:

- Multi-gig system design
- Advanced package modeling and simulation
- Testing issues: equipment, probes, test points
- SERDES and PLL jitter measurement & analysis
- Simulation and modeling methods
- Printed Circuit Boards
- Differential system routing, design and crosstalk
- Layout & routing strategies for high speed systems
- Advanced ultra-high speed design
- Connector pinouts for high speed return & crosstalk
- Power integrity: planes, capacitors, location
- Termination, topology, timing, parasitics
- S-parameters
- Vias: stub lengths, stack-up, impedance
- Basic & advanced IBIS training

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SIGNAL / POWER INTEGRITY & HIGH SPEED METHODOLOGY

Signal / Power Integrity & High Speed Methodology will familiarize you with signal integrity analysis at the board level. The lecture's modules address transmission lines and their effects on digital circuitry and printed circuit boards. The course will present detailed examples from real-world designs to demonstrate the necessity of understanding signal integrity issues and applying sound signal integrity principles to your PCB Design.

This course will provide an understanding of:

- Digital Design Engineers
- Printed circuit boards: drivers, receivers, Zo, Zdiff, stackup
- Termination, topology, timing, parasitics
- Differential pair routing, timing, crosstalk, common mode, terminating, multi-GHz
- Understanding and preventing Crosstalk: microstrip vs stripline, forward and reverse, timing and jitter
- Power integrity: planes, capacitors – ESL, size, location, mounting inductance
- Reference planes: ground, power, return currents, splits, crosstalk, stitch caps
- Vias: reference changes, stub lengths, stackup and impedance
- Connectors: pinouts for high speed return current and crosstalk
- High speed layout: vias, connectors, capacitors, PCB losses, planes
- S parameters
- Testing issues: equipment, probes and test points
- Models: IBIS, drivers, receivers, simulators and accuracy

This course is ideal for:

- Digital Design Engineers
- ECAD Designers with some high speed experience
- Technicians with high speed experience
- Those who would like to further their knowledge of Printed Circuit Board signal integrity issues
- Those with knowledge of general engineering principles (no advanced math is needed)

> "I attended your recent course at our Philips, Semiconductors site. I have found this to be one of the best training courses I have attended (and believe me I have attended quite a few). The presentation style, material and making use of real life examples made this much more informative and useful."

COURSE AGENDA

WHAT IS A TRANSMISSION LINE?	What causes transmission lines Avoiding transmission line problems
TRANSMISSION LINE EFFECTS	Undershoot and Overshoot – can destroy boards Ringback, monotonicity, crosstalk, timing
PRINTED CIRCUIT BOARDS	Stackup Making controlled Zo not controlled distance
DRIVERS, RECEIVERS, ZO	Strength and speed Incident vs reflected wave switching
BOARD INTERCONNECT DELAY	Receiver input C, driver output Rs, PCB Zo, etc. Reflected vs incident wave switching
TERMINATION	Placement and stub length Parallel, series, Zo matching, driver Rs matching
TOPOLOGIES	When are topologies important How do topologies affect signal integrity & timing
PACKAGE PARASITICS	Transmission lines in packages Capacitive loading on transmission lines
DIFFERENTIAL PAIR	Noise and EMI Weak vs strong coupling Skew affects on signal integrity and timing Routing rules
CROSSTALK	What causes crosstalk Microstrip vs Stripline - different FEXT vs NEXT Differential pair crosstalk Fixing crosstalk
PCB POWER INTEGRITY	Planes Bypass capacitors
REFERENCE PLANES	Vias, layer changes and references Controls routing and stackup
CONNECTORS	Reference consistency How many grounds & Vccs - return currents
VIAS	Stub lengths Blind and buried vias Pads, antipads, hole diameter
AC LOSSES	Skin effect Dielectric loss - Df Microstrip vs stripline
FIBER WEAVE EFFECT - FWE	Different weaves, different spacing Routing for skew - angles and spacing
TRACE SURFACE ROUGHNESS	Additional losses
S PARAMETERS	Frequency dependent descriptors Discontinuities, connectors, packages
TESTING ISSUES	How to test faster boards What equipment and how fast
IBIS MODELS	Drivers and receivers Repairing and modifying
LAYOUT ISSUES	What tools are needed for high speed boards Why signal integrity issues must be included

MASTERING HIGH SPEED SERIAL DATA TECHNOLOGY

Mastering High Speed Serial Data Technology teaches engineers how to master new concepts in signal integrity, equalization and hardware debug, helping digital engineers confront their analog roots and RF engineers face their digital fears. At multi-gigabit per second rates, trouble comes in many forms and we cover every one: signal distortion, random jitter, and noise at the transmitter to when or whether to switch from NRZ to PAM4 signaling, inter-symbol interference and crosstalk on circuit boards, backplanes and cables; and clock recovery, equalization, FEC and signal decoding at the receiver.

Using examples from cutting edge serial technologies – PCIe, OIF-CEI, sATA, Fiber Channel, 100 Gigabit Ethernet – this intense two day course delivers a complete technical understanding of potential trouble spots in high speed components and systems, compliance, diagnostics and functional testing, and how the standards attempt to insure interoperability.

With this course, you will:

- Master high speed serial-data technologies
- Design functional, compliance and manufacturing test systems
- Determine the sources of digital errors and how to correct them
- Master the dual-Dirac model, Q-scale, bathtub plots and total jitter defined at a BER
- Understand the advantages / disadvantages of embedded and distributed clocks
- Know when to switch from NRZ to PAM4
- Identify the sources of RJ, DJ, DDJ, ISI, SJ, PJ, HPBJ, DCD, BUJ, and E/OJ
- Devise transmitter pre/de-emphasis and receiver equalization schemes to improve BER
- Distinguish embedding and de-embedding and how effective they can be
- Appreciate the role of FEC and its limitations
- Understand emerging high data rate PHY specifications

This course is ideal for:

- Research, design, manufacturing, system and test engineers
- Digital and RF engineers
- Scientists and university students in electrical engineering and physics

Course organization:

The complete syllabus shown here composes a three day (8 hours per day) intensive course. It can easily be customized to a one or two day intensive course designed to meet your specific needs.

> Ransom's presentations are clear, to the point and entertaining.
>
> *- Megan Chura, Keysight Technologies*

COURSE AGENDA

Introduction to High Speed Systems	Differential signaling Embedded vs distributed clocks
Waveforms, Digits and Degradation	The digital myth and analog reality Dispersion, skin effect and inter-symbol interference Electromagnetic interference and periodic jitter
Errors, Jitter and Noise	The Bit Error Ratio (BER) In search of peak-to-peak jitter Distinguishing phase noise and jitter Measuring jitter: RJ, DJ, and the jitter alphabet soup Total jitter at a Bit Error Ratio, eye height & eye width The Dual-Dirac Model Bathtub plots and Q-Scale Eye closure and BER-contours Channel operating margin (COM)
Clocks and Clock Recovery	Effects of CDR bandwidth on measurements and systems Effect of data coding and scrambling on CDR technology CDR technologies Spread spectrum clocking
Equalization and Crosstalk	Pre/de-emphasis CTLE, FFE, DFE, and adaptive equalization Crosstalk in differential systems Equalization problems with crosstalk
High Speed Standards Compliance & Diagnostic Testing	Overview of HSS standards: 2.5-10 Gb/s, 25+ Gb/s technology, 100G, 400G, 1T - PCIe, USB, HDMI, SAS/sATA, OIF-CEI, 100 GbE - Tips on how to read standard specifications BER analysis on oscilloscopes and BERTs What you need to know about FEC Test patterns for better and worse PAM4 vs NRZ 100 GbE's COM Eye diagrams and transmitter testing Receiver tolerance testing Integrated crosstalk noise and interference tolerance testing What to expect from emerging standards

> Ransom is that teacher, the one who makes you wish you never left school.
>
> *- Andy Martwick, Intel*

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ABOUT THE SPEAKERS

Rod Strange is a registered engineer (PE) and holds a BSEE, MSEE, and a BS in Psychology, as well as one patent.

Rod has more than 20 years experience as a signal integrity engineer. He spent seven years as SI consultant for Intel, who contracted him to write a SI class for their engineers.

Since then, Rod has presented his signal integrity classes to more than 50 companies throughout the world.

Rod consults as a signal integrity engineer for seven months of the year, and presents for the other five months. After each high speed consulting project he incorporates the design issues into his classes so the material always stays up to date.

Past clients include Nokia, Lucent (US, Europe, Brazil), IBM, Philips, Tektronix, Boeing, Rockwell, Dell, HP, Motorola, Samsung (Korea), Siemens, NSA, BAE Systems, Barco, Northrop Grumman, Intel, RIM, EADS and more.

Ransom Stephens, Ph.D. is the author of more than 300 articles in the electronics industry, science journals and magazines on subjects ranging from the analysis of electrodynamics in high rate digital systems to fiber optics to quantum physics.

As a research physicist and professor, he worked on experiments at universities and laboratories across the US and Europe making precise measurements of messy signals.

After being awarded tenure, he shifted to private enterprise where he has expanded the field of signal integrity analysis of electrical and fiber optic systems and invented knew jitter measurement techniques and methods for extracting signals from noise.

He has also served on the electrical working groups for several high data rate standards including PCIe and OIF-CEI. Ransom is an entertaining teacher with a legendary reputation for delivering a clear understanding of complex topics.

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