0.6 µm Process Family:

XT06

0.6 Micron Modular Trench Isolated SOI CMOS Technology

MIXED-SIGNAL FOUNDRY EXPERTS

DESCRIPTION

The XT06 Series completes X-FAB's 0.6 Micron Modular Mixed Signal Technology.
XT06 uses dielectric isolation on SOI wafers. This allows unrestricted 60 V high and low side operation of all devices. The process offers reduced parasitics which results in smaller crosstalk, reduced noise and better EMC characteristics. Thus XT06 allows innovative circuit design with reduced circuit complexity. CMOS as well as Bipolar Transistors are available with breakdown voltages up to 110V. The 5 V CMOS core is compatible in design rules and transistor performance with state of the art 0.6 µm CMOS processes.
For analog applications several capacitor and resistor devices are realized, using the double-poly architecture. Full PDK support for major EDA vendors, extensive device characterization and modeling, comprehensive analog, digital, and memory IPs.

KEY FEATURES OVERVIEW

- 0.6-micron single poly, double metal 6-inch p-type SOI wafer basic process
- Triple metal option for high density circuits
- Thick 3rd layer metal for higher drive currents
- Different medium and high voltage options with 8 to 40 V DC operating conditions for NMOS and PMOS transistors
- Extended high-voltage modules up to 60V DC operating conditions - NMOS, PMOS and DMOS
- XT06 unique devices:
  - forward diodes
  - unrestricted 60V high and low side operation of all devices
  - reduced parasitics and crosstalk, better EMC
- Handle Wafer Contact module, Light Shield module, ROM, EEPROM module
- Bulk-isolated MV PMOS, scalable Schottky diode, HV rectifier diode
- option of arraying HV NMOS devices
- Protection diodes
- Double Poly-Si capacitor
- Linear poly capacitor module
- High-resistive Poly-Si resistor
- High precision BSIM3V3 SPICE models for CMOS and Gummel Poon model for bipolars
- Excellent analog performance with accurate device matching
- Different digital core cell libraries optimized for speed, low power, low noise or , inherited power connection concept
- High density RAM, DPRAM and ROM blocks
- About 2500/4500 effective gates per mm^2 (2ML/3ML)
- Pad-limited 5V I/O cell libraries with CMOS / TTL interfacing capability
- Optional ESD module for higher ESD protection
- OPTO module with optical window for improved transparency
- OTP option: Zener zap, Poly fuse
- Improved matching device models

APPLICATIONS

- Automotive electronics, communication, industrial and consumer market
- Low-power mixed signal circuits
- High precision mixed signal circuits
- Power management circuits
- Mixed signal embedded systems; systems on a chip (SOC)
- Analog front ends for sensors
- Circuits with integrated high voltage I/O's and voltage regulators

QUALITY ASSURANCE

X-FAB spends a lot of effort to improve the product quality and reliability and to provide competent support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, QS 9000, VDA 6, ISO TS 16949 and other standards.

DELIVERABLES

- PCM tested wafers
- Optional engineering services: Multi Project Wafer (MPW) and Multi Layer Mask Service (MLM)
- Optional design services: feasibility studies, Place & Route, synthesis, custom block development

LOGIC LIBRARIES

- Foundry-specific optimized libraries
- 3.3V or 5.0V operations
- Standard core library for high speed digital blocks
- Low-power library, 50% less power, 40% less area
- Low-noise library with separate bulk contacts for reduced substrate noise
- IEEE 1365 Verilog simulation models
- IEEE 1076.4 VHDL-VITAL simulation models
- Synthesis libraries
- Macrofunction and IP's on request
- RAM, DPRAM, ROM

ANALOG LIBRARIES

- Operational Amplifiers
- Bandgaps
- Bias Cells
- Comparators
- Power-On-Reset
- ADC / DAC
- RC / Crystal Oscillators
- Charge Pumps

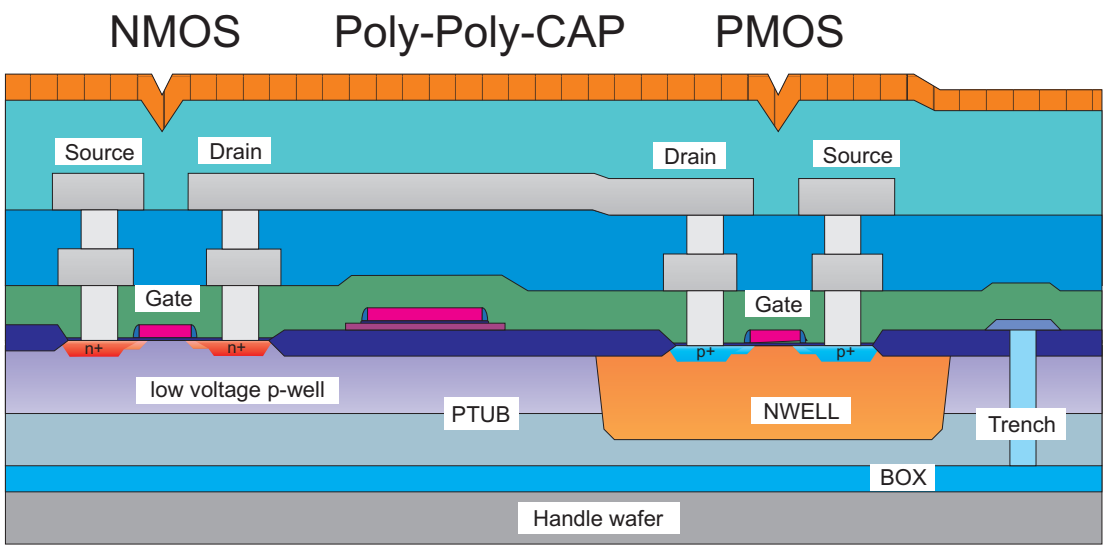
PRIMITIVE DEVICES

- NMOS/PMOS Transistors (5V to 60V)
- Bipolar Transistors
- Diodes, forward and reverse operation mode
- PIP, linear and sandwich capacitors
- Poly silicon and diffusion resistors

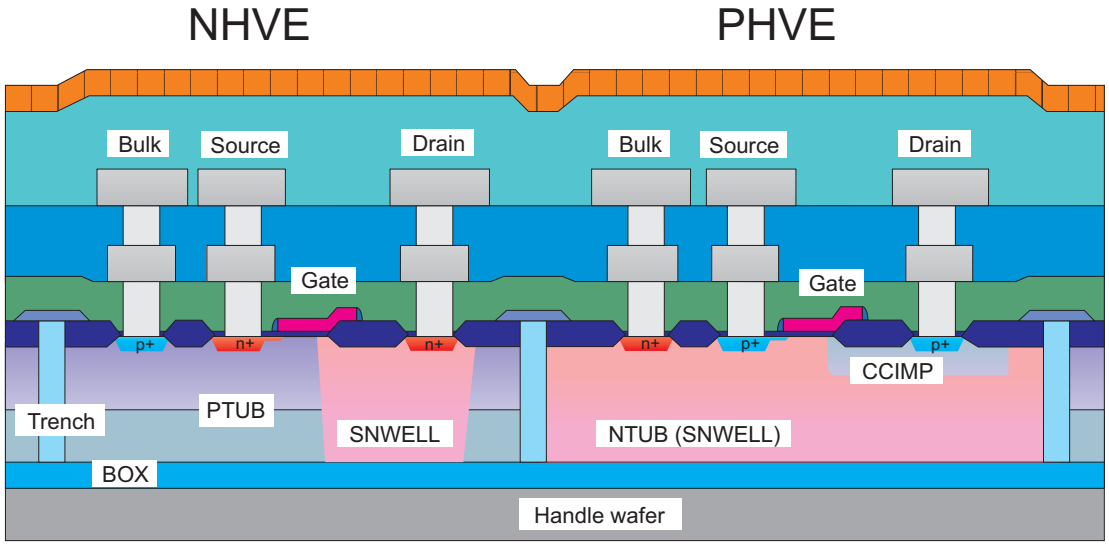
XT018 PROCESS FLOW

Core Module	Additional Modules	
Wafer Start		
TRENCH etch and refill		
TCOVER		
	HV N-well	HVS
	HV P-well	HVE
N-well		
Low voltage P-well		
	Trench etch and refill	HWCONT
Active area		
	Lighty doped HV P-well	PHVE
Field implant		
	Tunnel implant	ROM/EEPROM
	Tunnel Oxide	EEPROM
	Poly 0	CAPRES
	Linear poly cap implant	LINC
	ONO layer	CAPRES
	MV/HV Vt adjust implant	PMV
5V NMOS transistor implant	5V Tr Vt adjust implant	MIDOX
	Depletion implant	DEPL
	5V Tr Vt adjust implant	MIDOX
Poly 1 layer		
	ESD implant layer	ESD
	MV NMOS graded drain implant	NGD
NLDD implant		
	No PLDD implant	SCHOTTKY
PLDD implant		
2nd PLDD implant		
N+ implant		
P+ implant		
Contact		
Metal 1		
Via		
Metal 2		
	Via 2 / Metal 3	METAL3
	Via L / Thick Metal 3	THKMET
	Optical area etch	OPTO
Pads		
	Black resist	LIGHTSLD
	PIMIDE mask	PIMIDE
Back side grinding (on customer request)		
		mask steps

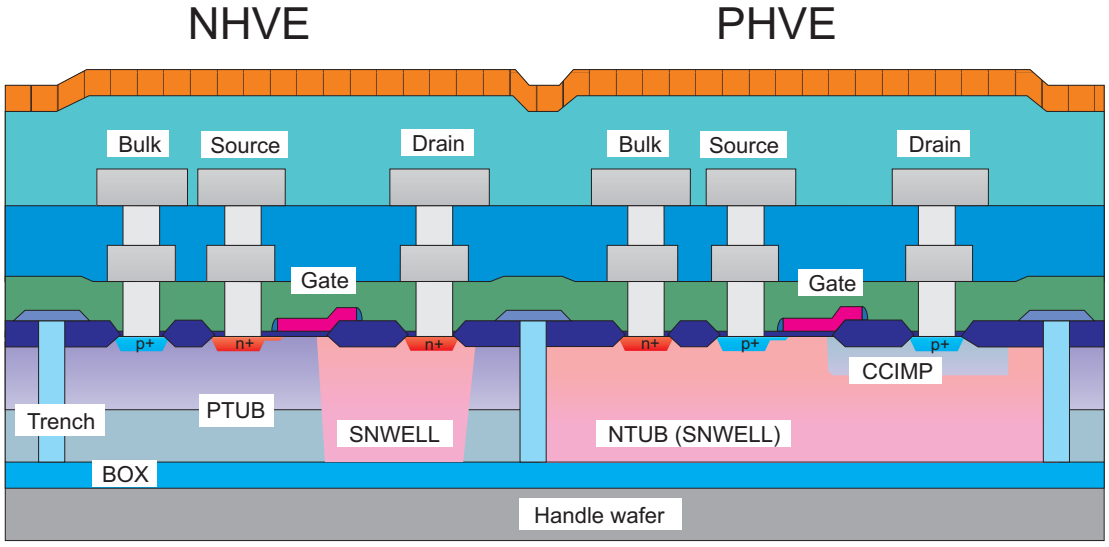
XT06 DEVICES SCHEMATIC CROSS SECTION



5V devices and poly-poly capacitor



Medium-voltage graded drain devices



Extended High-Voltage devices

XT06 CORE MODULE

Module Name	Descriptions	Masks No.
CORE	1.8/5.0V CORE module	14

XT06 ADDITIONAL MODULES

Module Name	Descriptions	Masks No.
ESD	ESD implant module	1
MIDOX	Mid-oxide module	2
PMV	Medium voltage p-channel module	1
NGD	Extended medium voltage n-channel module	1
DEPL	Medium/ high voltage depletion NMOS module	1
HVS	High voltage module	1
HVE	Extended high voltage module	1
PHVE	Extended high voltage PMOS module	1
CAPRES	Capacitor/ resistor module	2
LINC	Linear capacitor module	1
SCHOTTKY	Schottky diode module	1
ROM	ROM module	1
EEPROM *	EEPROM module	2
OPTO	Optical window module	1
METAL3	Triple metal module	2
THKMET	Thick third metal module	2
PIMIDE	Polyimide module	1
LIGHTSLD	Light shield module	1
HWCONT	Handle wafer contact module	1

* EEPROM module includes the ROM module

XT06 RESTRICTIONS FOR MODULE COMBINATIONS

Module name	Use of the module also requires use of the following module(s)	Use of the module is not available with the use of the following module(s)
PMV	MIDOX	
NGD	MIDOX	
DEPL	MIDOX	
HVS	MIDOX	
HVE	MIDOX	
PHVE	MIDOX, HVS	
LINC	CAPRES	
ROM		EEPROM
EEPROM	MIDOX, PMV, NGD, CAPRES	ROM, THKMET, LIGHTSLD
OPTO		THKMET
METAL3		THKMET
THKMET		OPTO, METAL3, LIGHTSLD, EEPROM
PIMIDE		LIGHTSLD
LIGHTSLD		THKMET, PIMIDE, EEPROM

CORE, MEDIUM-VOLTAGE AND HIGH-VOLTAGE MODULES - COMBINATION EXAMPLES

Technology Combiner	Recommendation
CORE	• 5V CMOS, • 5V PNP bipolar, • PTUB: all devices can be placed in oxide-isolated tubs and, therefore, are fully capable of up to 60V high side and low side operation
CORE+MIDOX	mid-oxide module is the base for all elements with higher than 5V operating voltage • 8V and 30V MOSFETs
CORE+MIDOX+PMV	• PMOS for 8V and 12V operation
CORE+MIDOXNGD	• NMOS for up to 12V operation
CORE+MIDOX+HVS	• PMOS for up to 40V operation, • NMOS for up to 60V operation, • bulk isolated 5V PMOS without parasitic vertical PNP
CORE+MIDOX+HVS+HVE	• NDMOS for up to 60V operation, • NPN bipolar, up to 20V operation
CORE+MIDOX+HVS+PHVE	• PMOS for up to 60V operation
SCHOTTKY+HVS	• Scaleable Schottky diode

XT06 BASIC DESIGN RULES

Mask	width [µm]	Spacing [µm]
Trench	2.0	6.0
Standard N-well	4.0	2.0 *
HV N-well	10.0	3.0 *
HV P-well	6.0	8.5
Active Area	0.6	1.2
Poly-Silicon Gate	0.6	0.8
Contact	0.6	0.6
Metal 1 /2	0.9	0.8
Via 1 / 2	0.7	0.6
Metal 3	1.2	1.0
Via L	0.7	0.7
Metal L	2.5	2.5

* Seperated by Trench

Active Devices

XT06 LV MOS TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	BVDS [V]	Max. VDS [V]	Max VGS [V]
low voltage NMOS	nmos4	CORE	0.87	470	13	5.5	5.5
low voltage PMOS	pmos4	CORE	0.90	230	12	5.5	5.5
NMOS with ESD implant	nesd	ESD	0.90	460	11.5	5.5	5.5
bulk isolated PMOS	pmosdi	HVS	0.94	220	12	5.5	5.5

XT06 MV MOS TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	RON @VGS [kΩ.µm]	BVDS [V]	Max. VDS [V]	Max VGS [V]
MV NMOS	nmv	MIDOX	0.90	160	7.4 @5V	16	8	18
MV NMOS low doped drain	ngmv	NGD	0.88	160	4.5@12V	22	12	18
MV NMOS low doped source/drain	ngmmv	NGD	0.88	150	5.3 @12V	22	12	18
MV PMOS	pmv	PMV	0.88	58	33 @5V	13	8	18
MV PMOS low doped drain	pgmv	PMV	0.90	53	20 @12V	18	12	18
MV PMOS low doped source/drain	pgmmv	PMV	0.90	44	26 @12V	18	12	18
bulk isolated MV PMOS	pmvdi	PMV+HVS	1.25	45	34 @5V	13	8	18
bulk isolated MV PMOS	pmvdia	HVS	0.77	75	15 @12V	16	8	18

XT06 HV MOS TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	RON @VGS [kΩ.µm]	BVDS [V]	Max. VDS [V]	Max VGS [V]
HV NMOS	nhv	MIDOX	0.82	95	19 @12V	60	30	18
HV PMOS	phv	HVS	0.82	56	39 @12V	70	37	18
extended HV NMOS	nhve	HVS	0.72	110	23 @12V	80	60	18
extended HV PMOS	phve	PHVE	0.78	50	50 @12V	80	57	18
extended HV NDMOS	ndhe	HVS+HVE	1.10	60	28 @12V	110	60	18

XT06 DEPLETION MOS TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	RON @VGS [kΩ.µm]	BVDS [V]	Max. VDS [V]	Max VGS [V]
MV depletion NMOS	nmvd	DEPL	1.1	28	5.6 @5V	16	8	18
HV depletion NMOS	nhvd	DEPL	1.25	13	16 @12V	60	30	18

XT06 BIPOLAR TRANSISTORS

Device	Name	Available	BETA	VA [V]	VBE [mV]	max. VCE [V]
vPNP (collector on PTUB)	qpv5	CORE	15 @10µA	>100 @100nA	700 @10µA	5.5
vNPN	qnve	HVS+HVE	60 @0.5µA	>100 @5nA/µm	657 @0.5µA/µm	20

Passive Devices

XT06 DIFFUSION RESISTORS

Device	Name	Available with module	RS[Ω/□]	Temp. Coeff. [10^{-3}/K]	Max |VTB| [V]
N+ diffusion in P-sub	rdiffn3	CORE	57	1.5	8
P+ diffusion in N-well	rdiffp3	CORE	115	1.3	8
P+ resistor in deep N-well	rdiffpsnw3	HVS	115	1.3	8

XT06 POLY RESISTORS

Device	Name	Available with module	RS [Ω/□]	Temp. Coeff. [10^{-3}/K]	Max VTB [V]
Poly1	rpoly1	CORE	17	1.1 / 1.0*	60
Low T.C. poly0	rpoly0	CAPRES	610	-0.26 / 1.15*	60
High resistive poly0	rpolyh	CAPRES	3500	-3.3 / 10.9*	60

* linear / quadratic temperature coeffecient

XT06 METAL RESISTORS

Device	Name	Available with module	RS [Ω/□]	Thickness [µm]	Max J/W [mA/µm]	Temp. Coeff. [10^{-3}/K]	Max VTB [V]
Metal 1	rm1	CORE	0.08	0.67	1.0	3.3	60
Metal 2	rm2	CORE METAL3/THKMET	0.045 0.075	1.0 0.8	1.3	3.3	60
Metal 3	rm3	METAL3	0.045	1.0	1.3	3.3	60
Thick metal	rmtpl	THKMET	0.012	2.45	7.0	3.7	60

XT06 PIP CAPACITORS

Device	Name	Available with module	Area Cap [fF]	Perimeter Cap.[fF/µm]	Max VTB [V]
Poly0/poly1	cpoly	CAPRES	1.87	0.15	20
Linear poly0/poly1	cpolylin	LINC	1.02	0.12	30

XT06 SANDWICH CAPACITORS

Device	Name	Available with module	Area Cap [fF]	Perimeter Cap.[fF/µm]	Max VTB [V]
SNWELL/P1/M1/M2	csandw	HVS	0.13	0.075	60
Poly1/M1/M2	csandwt	CORE	0.07	0.05	60
Poly1/M1/M2/M3	csandwtm	METAL3	0.10	0.07	60
Poly1/M1/M2/THKMET	csandwtml	THKMET	0.10	0.08	60

XT06 POD CAPACITORS

Device	Name	Available with module	Area Cap [fF]	Perimeter Cap.[fF/µm]	Max VTB [V]
poly1/tunnel implant with mid-oxide in P-sub	ctm	ROM+MIDOX	0.80	0.10	8
poly1/tunnel implant with mid-oxide in N-well	ctmw	ROM+MIDOX	0.80	0.10	40
tunnel implant/poly0/poly1in P-sub	ctp0p1	ROM+CAPRES	2.58	0.50	8
tunnel implant/poly0/poly1 in N-well	ctp0p1a	ROM+CAPRES	2.58	0.50	40
poly1/tunnel implant with mid-oxide in N-well	ctp0p1b	ROM+CAPRES+HVS	2.58	0.50	60

Passive Devices *(Continued)*

XT06 PROTECTION DIODES

Device	Name	Available with module	BV [V]	Max BD current [µA/µm]
5V N-type protection	dprot	CORE	4.7	0.5
18V N-type protection	dnsp18	HVS	24	5
30V N-type protection	dnsp30	HVS	36	5
40V N-type protection	dnsp40	HVS	46	5

XT06 RECTIFIER DIODES

Device	Name	Available with module	Vforward [V]	Max If [µA/µm]	Max Vr [V]
NDIFF/PTUB rectifier	dfwdn	CORE	0.75	0.3	10
Field imp/NTUB HV rectifier	dfwdph	HVS	0.75	0.3	50
CCIMP/NTUB HV rectifier	dfwdcc	PHVE	0.75	0.3	60

XT06 SCHOTTKY DIODES

Device	Name	Available with module	VForward [V]	IForward [µA]	BV [V]	I leak [nA]
Scalable schottky diode*	dsdi	SCHOTTKY+HVS	0.34 @10µA	100 @0.6V	21	< 2

* Fixed length (L), stretchable width (W). Device parameters @ 2x2 µm²

XT06 DIFFUSION DIODES

Device	Name	Available with module	Area junc. cap. [fF/µm²]	BV [V]	Max Vreverse
NDIFF/PTUB	dn	CORE	0.31	15	10
PDIFF/NWELL	dp	CORE	0.53	14	10
NWELL/PTUB	dnw	CORE	0.10 @Vnw = 60V	33	20
NWELL/PTUB (HV area)	dnwh	MIDOX	0.10 @Vnw = 60V	61	50
SNWELL/PTUB	dsnw	HVS	0.25 @Vnw = 60V	110	60
PDIFF/SNWELL	dpsnw	HVS	0.28	23	13
PDIFF/NWELL/SNWELL	dpdi	HVS	0.56	15	10
Field implant/SNWELL	dph	HVS	0.21	65	50
PWELL/SNWELL	dpws	HVS+HVE	0.05 @Vnw = 60V	80	40
CCIMP/SNWELL	dcsnw	PHVE	0.29	80	60

Non-Volatile-Memory

XT06 POLY FUSE

Device	Name	Available with module	R unprog. [Ω]	R prog. [Ω]	Max Vread unprog. [V]	Max Vread prog. [V]
Poly fuse	pfuse	CORE	150	> 10M	1	5.5

XT06 ZENER DIODES

Device	Name	Available with module	Vzapp [V]	|BV| [V]	I leak [nA]	Max Iread [mA]
Zener Zap	dzap	CORE	0.7	4.3	1000	0.2

Non-Volatile-Memory *(Continued)*

XT06 ROM

Device	Name	Available with module	Drain current @ 0V [µA]	Max VGS [V]	Max VDS [V]
Implantation programmed ROM cell	rom	ROM	350	5.5	5.5

XT06 EEPROM

Parameters	Values
Memory size	Up to 32 Kbit (0.44mm2 for 64 x 8 bit, with internal charge pump)
Supply voltage	1.8 ... 6.0V
Current consumption	< 120 µA (typical)
Number of erase/write cycle	1 x 104 @ 25 °C 1 x 103 @ 125 °C
Temperature range	-40 ... +125 °C (for read, write/erase)
Access time	< 0.8µs (Read) min. 4 ms (Erase/Write)
Data retention	10 years @ 85 °C

Digital Standard Cells Libraries

XT06 LOGIC LIBRARIES

Device	Library feature	Voltage range	Application benefits
D_CELLS	standard	3.3V / 5.0V	high speed
D_CELLS_B	standard, low noise	3.3V / 5.0V	high speed, seperated bulk supply for nmos, pmos
D_CELLSL	low power	3.3V / 5.0V	low power
D_CELLSL_B	low power, low noise	3.3V / 5.0V	low power, seperated bulk supply for nmos, pmos

I/O Libraries

XT06 I/O LIBRARY

Device	Library Feature	V_{CORE} *	V_{IO} *	ESD Level	Application benefits
IO_CELLS_E	Standard, V_{CORE}=V_{IO} single supply voltage, ESD Implant	5.0V	5.0V	4kV HBM	Pad limited
IO_CELLS_FE	Standard, V_{CORE}=V_{IO} single supply voltage, ESD Implant	5.0V	5.0V	4kV HBM	Core limited

* Please refer to the library databook for details about available PVT ranges

HV Libraries

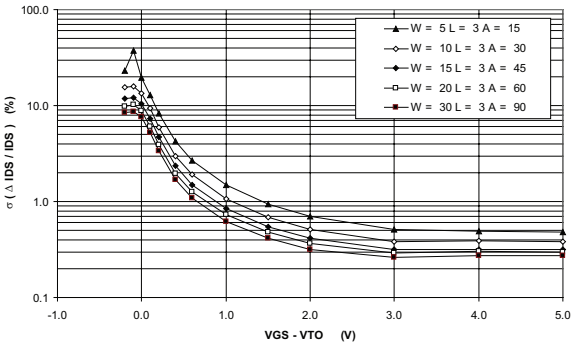
XT06 HV LIBRARY

Device	Library Feature	Voltage range	ESD Level	Application benefits
HV_CELLS	Special MV supply pads, operating voltage specific HV ESD protection cells	MV, ± 7V-46V	4kV-8kV HBM	Customized I/O design

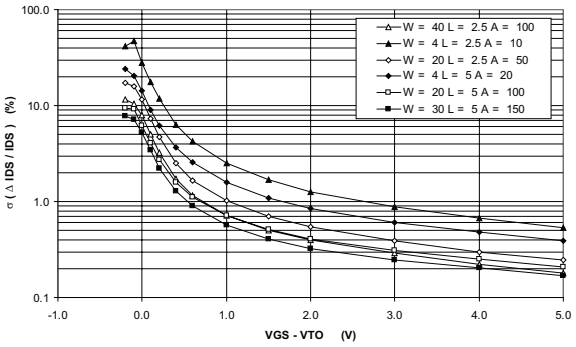
ANALOG LIBRARIES

XT06 A_CELLS ANALOG LIBRARY			
Library	**Cell Name**	**Operating conditions**	**Required module**
Operational Amplifier	aopac01 aopac09 aopac10 aopac11 aopac12	VDD: 4.5V to 5.5V; T: -40...85°C	CORE
Operational Amplifier	aopac02 aopac03 aopac06 aopac07 aopac08	VDD: 4.5V to 5.5V; T: -40...85°C	CORE CAPRES
Comparators	acmpc01 acmpc02 acmpc03 acmpc04 acmpc06	VDD: 4.5V to 5.5V; T: -40...85°C	CORE
Bandgap	abgpc01	VDD: 4.0V to 5.5V; T: -40...85°C	CORE
Bandgap	abgpc02 abgpc03 abgpc04	VDD: 4.0V to 5.5V; T: -40...85°C	CORE, CAPRES
Bias Cells	abaic01 abiac02 abiac03	VDD: 4.5V to 5.5V; T: -40...85°C	CORE
Bias Cells	acsoc05 acsoc06	VDD: 4.5V to 5.5V; T: -40...85°C	CORE, CAPRES
ADC	aadcc01 aadcc02 aadcc03	VDDA: 4.5V to 5.5V; T: -40...85°C	CORE, CAPRES
DAC	adacc01 adacc03	VDDA: 4.5V to 5.5V; T: -40...85°C	CORE, CAPRES
DAC	adacc02	VDDA: 4.5V to 5.5V; T: -40...85°C	CORE
RC Oscillators	arcoc01 arcoc02 arcoc04 arcoc05 arcoc06 arcoc07 arcoc08 arcoc09	VDD: 4.5V to 5.5V; T: -40...85°C	CORE, CAPRES
RC Oscillators	arcoc03	VDD: 4.5V to 5.5V; T: -40...85°C	CORE
Crystal Oscilators	axtoc01 axtoc02 axtoc03	VDD: 3.5V to 5.5V; T: -40...85°C	CORE, CAPRES
Power-On-Reset	aporc01 aporc02 aporc03	VDD: 4.5V to 5.5V; T: -40...85°C	CORE
Charge Pumps	achpc01	VDD: 4.5V to 5.5V; T: -40...85°C	CMOS, CAPRES

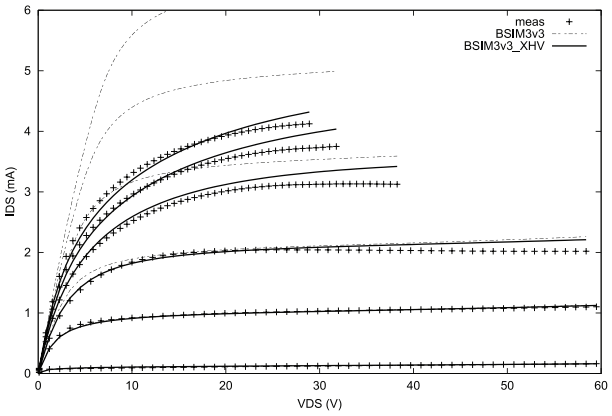
EXAMPLES FOR MEASURED AND MODELED PARAMETER CHARACTERISTICS



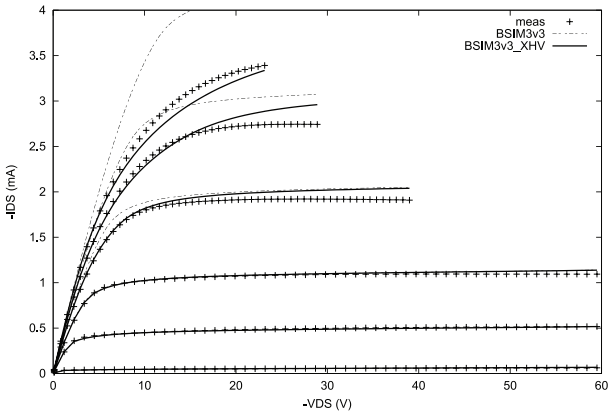
Device nhve : drain current matching vs. Vgs (typical value). legends show the drawn transistor lengths and widths



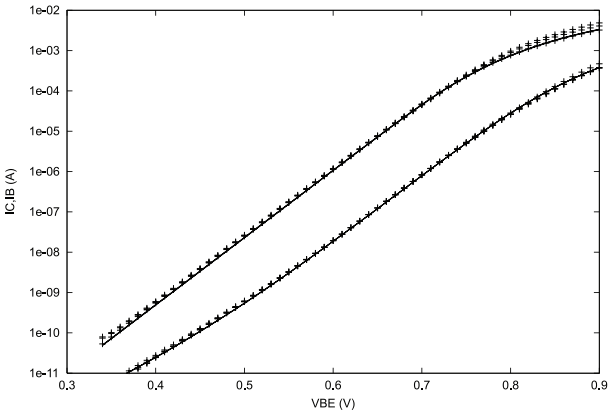
Device phve : drain current matching vs. Vgs (typical value). legends show the drawn transistor lengths and widths



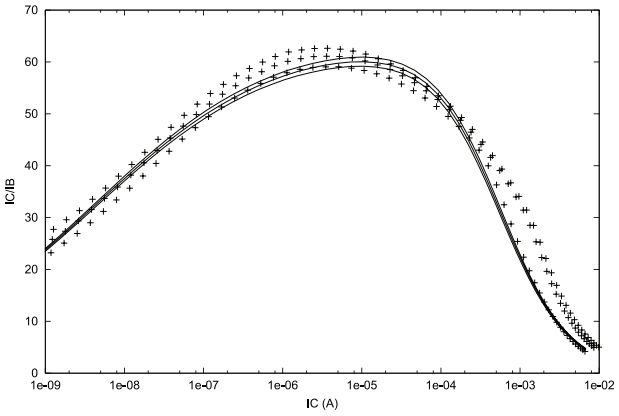
Device nhve: Ouput characteristic for a typical wafer. W/L = 20/3, VGS = 1.4, 3.2, 5.0, 7.33, 9.67, 12.0V, VSB = 0V, + = measured, dotted line = BSIM3v3 model, solid line = BSIM3v3_ XHV model



Device phve: Ouput characteristic for a typical wafer W/L=20/2.5, -VGS = 1.4, 3.2, 5.0, 7.33, 9.67, 12.0V, VSB = 0V, + = measured, dotted line = BSIM3v3 model, solid line = BSIM3v3_ XHV model

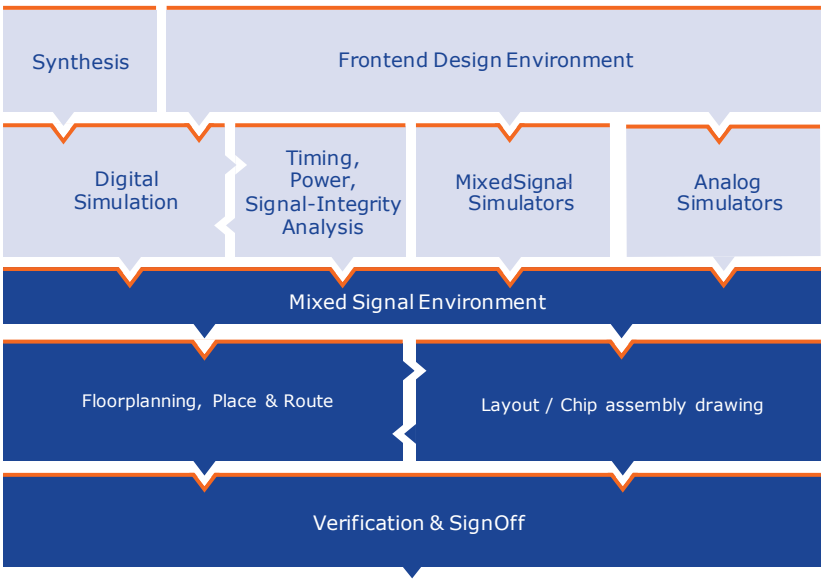


Device qnve: Gummel plot of vertical PNP bipolar transistor for typical wafer, LE = 20 µm, VCB = 0, 5, 10V, + = measured, solid line = SPICE model



Device qnve: Current gain of vertical NPN bipolar transistor for a typical wafer, LE = 20 µm, VCB = 0, 5, 10V, + = measured, solid line = SPICE model

XT06 SUPPORTED EDA TOOLS



Note: Diagram shows overview of reference flow at X-FAB. Detailed information of suported EDA tools for major vendors like Cadence, Mentor and Synopsys can be found on X-FAB's online technical information center X-TIC.

X-FAB'S IC DEVELOPMENT KIT "THEKIT"

The X-FAB IC Development Kit is a complete solution for easy access to X-FAB technologies. TheKit is the best interface between standard CAE tools and X-FAB's processes and libraries. TheKit is available in two versions, the Master Kit and the Master Kit Plus. Both versions contain documentation, a set of software programs and utilities, digital and I/O libraries which contain full front-end and back-end information for the development of digital, analog and mixed signal circuits. Tutorials and application notes are included as well. The Master Kit Plus additionally provides a set of general purpose analog functions mentioned in section "Analog Library Cells" and is subject to a particular license.

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