

1.0 μm CMOS Process

> XC10



One Micron Modular Mixed Signal Technology

> Description

The XC10 Series is X-FAB's One-Micron Modular Mixed Signal Technology. Main target applications are standard cell, semi-custom and full custom designs for Automotive, Consumer, Industrial and Telecommunication products. The process enables mixed-signal systems on one chip by its non-volatile memory and sensor integration capabilities. Based on a state of the art very cost effective single poly single metal 1.0-micron minimum feature size N-well process for mixed-signal and high voltage applications, various process modules are

available for high performance analog and high voltage circuits. Using the non-volatile memory modules integration of EEPROM, OTP or NV latches is possible.

Technology variants for integrated MEMS are available.

Reliable design rules, precise SPICE models, cell libraries, IP's and development kits support the process for major CAE vendors.

> Key Features

- Cost effective one micron single poly, single metal N-well core process on P epi
- High voltage (100 V) N-MOS transistors available in the core process (no additional mask)
- Double poly module for resistors and capacitors
- High-voltage (50 V) option for P-MOS transistors
- Low-voltage option (1.5 V instead of 5 V operating voltage)
- Special devices:
 - depletion and zero transistors
 - Schottky and Zener diodes
 - high-ohmic resistors
 - bipolars
- Double metal option
- Power metal option
- High precision BSIM3V3 SPICE models
- Excellent analog performance with accurate device matching
- Digital core cell library with typical 600 effective gates per mm^2
- Typical gate delays (digital) of 3.5 ns
- I/O cell library
- Electrostatic discharge (ESD) protection in accordance with MIL-STD
- Memories: RAM, ROM, EPROM, EEPROM
- Parameter trimming by poly-fuses or non-volatile latches
- Development kits for major EDA tools
- Megafunctions and IP's available
- Optional ESD layer for higher ESD protection
- Optical window module

> Applications

- Mixed signal embedded systems; systems on a chip (SOC) with NV memories
- Integrated sensors and sensor interfaces
- Low voltage / low power
- High precision mixed signal circuits
- Circuits with integrated high voltage I/O's and voltage regulators
- Instrumentation
- AD/DA Converters
- Communications, automotive & industrial markets

> Quality Assurance

X-FAB spends a lot of effort to improve the product quality and reliability and to provide competent support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by

strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, QS 9000, VDA 6, ISO TS 16949 and other standards.

> Deliverables

- PCM tested wafers
- Optional Engineering services: Multi Project Wafer (MPW) and Multi Layer Mask Service (MLM)
- Optional Design services; e.g. feasibility studies, place & route, synthesis, custom block development
- Internal second source availability

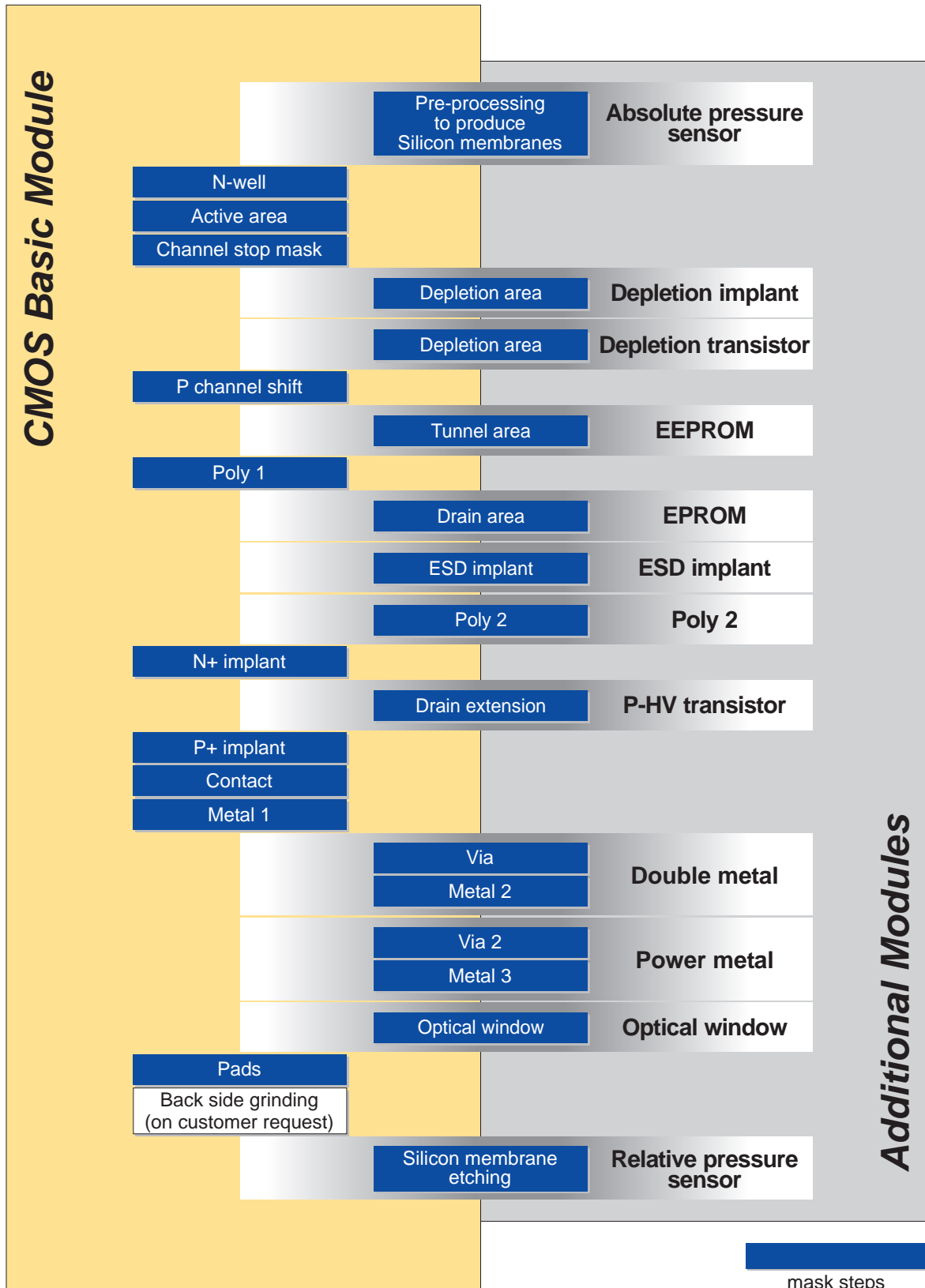
> Digital Libraries	<ul style="list-style-type: none"> - Foundry-specific optimized library - IEEE 1364 Verilog simulation models - IEEE 1076.4 VHDL-VITAL simulation models - PSPICE simulation models - Synthesis libraries - Macrofunction and IP's on request - RAM, ROM, EPROM, EEPROM, NV latches on request
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> Primitive Devices	<ul style="list-style-type: none"> - Standard NMOS/PMOS, Zero- and Depletion NMOS Transistors - Mid Voltage NMOS/PMOS Transistors (12 V) - High Voltage NMOS/PMOS and Depletion NMOS Transistors (up to 100 V) - NPN/PNP Bipolar Transistors - Diodes - Zener and Schottky Diodes - Capacitors - Poly Silicon and Diffusion Resistors - Poly Fuses
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> Process Options

Module name	No. of masks	Remarks
CMOS basic module	9	P-epi wafer, single poly, single metal, operating voltage > 5V
Low voltage module	9	Features of basic module retain, operating voltage > 1.5V
To get the available technology options, each of these two main modules can be combined with one or more of the following additional modules:		
Module name	No. of additional masks	Remarks
Depletion implant	1	for ROM programming and/or capacitors
Depletion transistor	1	depletion transistor
Poly2	1	poly1-poly2 capacitors and/or resistors
P-HV transistor	1	p-channel high voltage transistors
ESD implant b)	1	ESD implant to improve ESD robustness at 5V I/O's
Double metal	2	metal 2
Power metal a, c, d)	2	thick metal 3
EEPROM a)	1	EEPROM cell
EPROM a)	1	EPROM cell
Optical window d)	1	optical applications
Relative pressure sensor	max. 3	for 0.1bar, 0.5bar and 3.0bar pressure cells
Absolute pressure sensor	3	pre-processing to produce Silicon membranes
Notes: a) This module requires the addition of other modules as listed in the below table. b) The combination of ESD implant module and low voltage module is not allowed. c) The combination of low voltage module and power metal module is not offered. d) The combination of power metal module and optical window module is not offered.		
Module name	Usage of the module also requires the use of following modules	
Power metal	Double metal	
EEPROM	Depletion implant	
EPROM	Depletion implant	

> Main Process Flow



> Schematic Cross Sections

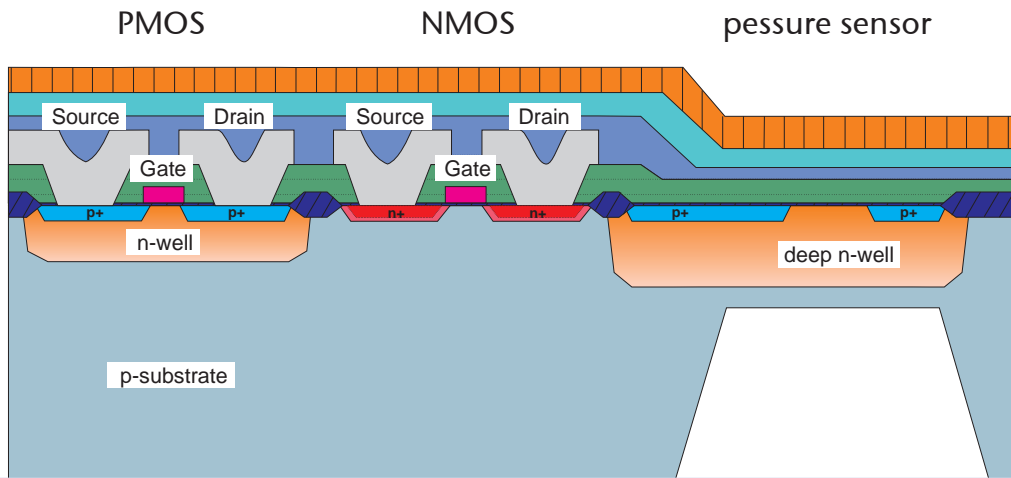


Figure 1: MOS Transistors and Pressure Sensor

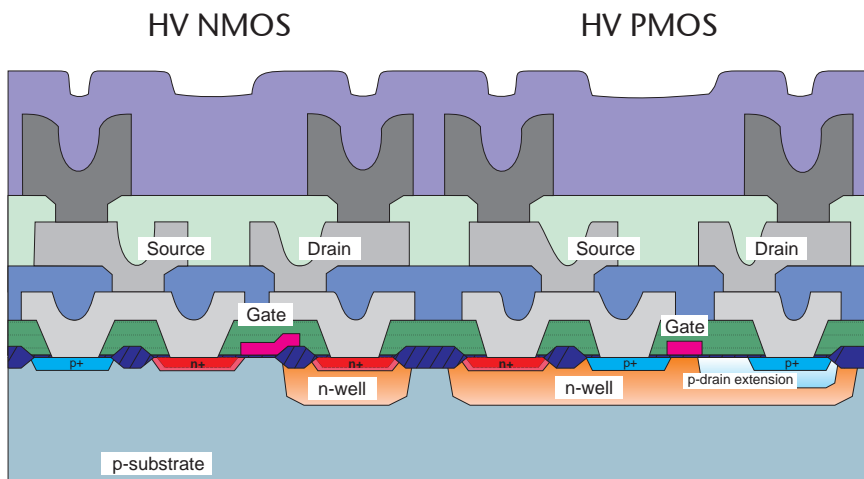


Figure 2: High Voltage Transistors

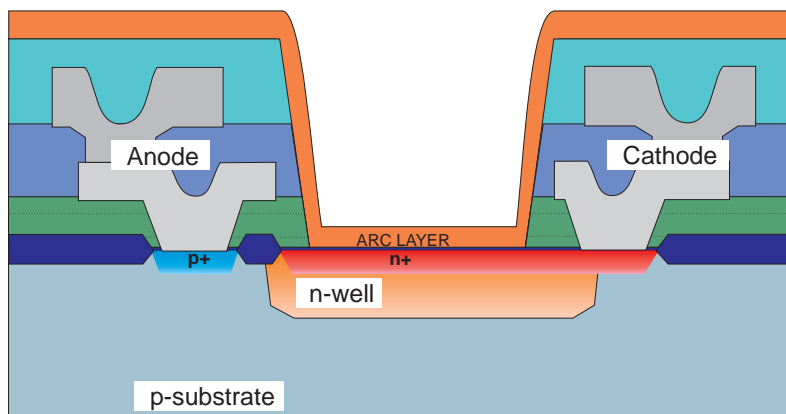


Figure 3: Optical Diode

Basic Design Rules		
Mask	Width [μm]	Spacing [μm]
N-well	3.2	14.0
Active Area	0.8	2.0
Poly-Silicon Gate	1.2 / 1.3	1.2
Contact	1.2	1.0
Metal 1	1.1	1.5
Via 1	1.7	1.6
Metal 2	1.4	1.7

> Device Parameters

The following devices can be used for circuit designs. They are well characterized and part of a primitive device library. The device names correspond with the SPICE model names. They all have been qualified. Different stress tests gave the maximum allowed operating conditions.

Note: The values in brackets denote absolute maximum ratings. See also the availability with different options.

Active Devices (typical data)

Unipolar Transistors						
Device	Name	Available only with	VT [V]	IDS [$\mu\text{A}/\mu\text{m}$]	BVDSS [V]	Max. VDS [V]
N Channel Enhancement Transistor	NE		0.8	175	> 13	5.5 (7)
N Channel Medium Voltage Transistor	NE5		0.8	55	> 14	7 (8)
P Channel Enhancement Transistor	PE		-0.9	-70	< -13	5.5 (7)
P Channel Medium Voltage Transistor	PE2		-0.9	-52	< -14	12 (14)
N Channel Natural Transistor	NN		-0.1	90	> 14	12 (14)
N Channel Drain High Voltage Transistor 100 V	NGD		0.70	240	> 95	80 (85)
N Channel Drain High Voltage Transistor 50 V	NGDM		0.65	220	> 45	30 (35)
N Channel Source/Drain High Voltage Transistor 100 V	NGDS		0.75	125	> 95	80 (85)
N Channel Source/Drain High Voltage Transistor 50 V	NGDSM		0.75	115	> 45	30 (35)
N Channel Natural Drain High Voltage Transistor 100 V	NGDN		-0.2	235	> 95	80 (85)
N Channel Natural Drain High Voltage Transistor 50 V	NGDNM		-0.2	210	> 45	30 (35)
N Channel Natural Source/Drain High Voltage Transistor 100 V	NGDSN		-0.2	150	> 95	80 (85)
N Channel Natural Source/Drain High Voltage Transistor 50 V	NGDSNM		-0.22	145	> 45	30 (35)
P Channel Drain High Voltage Transistor 50 V	PGD	P-HV	-0.90	-110	< -45	40 (45)
P Channel Drain High Voltage Transistor 40 V	PGDM	P-HV	-0.90	-180	< -35	30 (35)
P Channel Source/Drain High Voltage Transistor 50 V	PGDS	P-HV	-0.85	-70	< -45	40 (45)
P Channel Source/Drain High Voltage Transistor 40 V	PGDSM	P-HV	-0.85	-115	< -35	30 (35)
N Channel Depletion Transistor	ND	Depl. Tr.	-1.1	115	> 13	11 (13)
N Channel Depletion Drain High Voltage Transistor 50 V	NGDDM	Depl. Tr.	-1.2	115	> 45	40 (45)
N Channel Depletion Source/Drain High Voltage Transistor 50 V	NGDSDM	Depl. Tr.	-1.15	50	> 45	40 (45)

Note: Maximum gate to bulk voltage of all MOS devices is 20 (22) V

Bipolar Transistors						
Device	Name	Available only with	Max. Vce [V]	Max. Veb [V]	Ic/Ib	Vce0 [V]
Vertical PNP	SBIP		5.5 (7)	5.5 (7)	> 20	
Vertical NPN	NPN	P-HV	6 (8)	20 (22)	> 500	> 10

> Device Parameters (continued)

Active Devices (typical data) (continued)

Special Diodes				
Device	Name	Available only with	Zener breakdown voltage [V] min / typ / max	
Zener Diode	DZE		4.6 / 4.9 / 5.2	
Device	Name	Available only with	Forward Bias [V] min / typ / max	Leakage Current [nA] min / typ / max
Schottky Diode	DSB	Not with power metal	0.4 / 0.6 / 0.8	- / 0.5 / 10

Passive Devices (typical data)

Resistors						
Device	Device Name	Avail. only with module	Max Vterm-Bulk [V]	max. J/W [mA/μm]	RS [Ω/□]	TC [10 ⁻³ /K]
N well resistor	RW		95 (100)		1300	6.4
N+ Resistor	RDN		13 (15)		25	1.3
P+ Resistor	RDP		13 (15)		125	1.0
N+ Poly 1 Resistor	RP		95 (100)	0.6	27	0.75
P high resistive Poly 2 Resistor	RP2	Poly 2	95 (100)	0.04	20,000	- 5.0
P+ Poly 2 Resistor with low TC	RP20	Poly 2	95 (100)	0.4	355	- 0.2

Capacitors						
Device	Device Name	Avail. only with module	Max Vterm [V]	C [ff/μm ²]	TC [10 ⁻³ /K]	Linearity [ppm/V]
Poly1 - N+ Depletion Capacitor	CD	Depletion Implant	20 (22)	0.69	0.03	
Poly1 - Poly2 Capacitor	CPP	Poly 2	15 (22)	0.43	0.07	250

Misc. Devices

Memory Blocks	
EEPROM (Example)	
Memory Size	256 Byte (128 x 16)
Area	1.7 mm ² (with internal charge pump)
Power supply range	3.5 - 6V
Current consumption	< 100 μA (typical)
Temperature range	-55 to +125 °C
Read Access Time	< 4 μs
Programming Time	4 ms
Endurance	30,000 cycles @ 85 °C
Data retention	10 years @ 85 °C
OTP EPROM (Example)	
Memory Size	8 Kbytes: (Program: 2Kx32, Read: 4Kx16)
Area	7.1 mm ²
Supply Voltage	3 ... 5.5 V
Supply Current	500 μA
Temperature Range	-40 ... +125 °C (Read) +20 ... +40 °C (Program)
Read Access Time	250 ns @ 5 V
Data Retention	10 Years @ 85 °C

Note: General characteristics. For detailed values check the datasheet of the available blocks

> Digital Core Library Cells

X-FAB provides process specific digital core cell libraries. The libraries can be used both for double layer metal and power layer metal designs.

- The **standard library** is optimized for the best trade-off between speed, area and power consumption. It is characterized both for 5.0V and 3.3V VDD range.
- The **low voltage library** uses the low voltage process which is provided for applications in the 1.5V range. It is also possible to use the low voltage library in the 3.3V range. Due to the lower threshold voltages of this process the power consumption is higher compared to the standard library with the standard process.

Name	Category	Density ¹⁾	@ r_factor ²⁾
XC10 D_CELLS	standard	ML2: 0.6	ML2: 3.3
XC10LV D_CELLS	low voltage	ML2: 0.6	ML2: 3.3

¹⁾ average value: kGE/mm² (GE = NAND2 Gate Equivalent)
ML2: 2 metal layer routing
²⁾ average value: r_factor = Routing_factor
Place&Route_area = Cell_area * Routing_factor

> Digital I/O Cells

Two I/O ring systems are available for pad-limited and for core limited designs. Pad-limited cell height is 506 µm with 204 µm bond pad pitch. I/O cells for core limited design have 270µm height with variable bond pad pitch (192 µm ... 402 µm).

Name	Description	Size [µm x µm]
BPIA	Analog input	276 x 270
BPIAPU	Analog input with pull up	287 x 270
BPIAPD	Analog input with pull down	287 x 270
BPIC	C-MOS input	300 x 270
BPICPU	C-MOS input with pull up	315 x 270
BPICPD	C-MOS input with pull down	315 x 270
BPIT	TTL-compatible input	306 x 270
BPISCH	C-MOS Schmitt trigger input	306 x 270
BPISCHPU	BPISCH, with pull up	315 x 270
BPISCHPD	BPISCH, with pull down	315 x 270
BPOC	Buffered output	348 x 270
BPOCS	Buffered output (small)	228 x 270
BPIOC	Bi-directional pad	402 x 270
BPOOSN	Open drain output	288 x 270
BPWEEDY	Weedy buffer	299 x 270
BPOUT	Output pad	276 x 270
BPPAD	Bonding pad	192 x 270
BPVDD	Supply pad	192 x 270
BPVSS	Ground pad	192 x 270
SPIA	Analog input	204 x 506
SPIAPU	Analog input with pull up	204 x 506
SPIAPD	Analog input with pull down	204 x 506
SPIC	C-MOS input	204 x 506
SPICPU	C-MOS input with pull up	204 x 506
SPICPD	C-MOS input with pull down	204 x 506
SPOCS	Buffered output (small)	204 x 506
SPWEEDY	Weedy buffer	204 x 506

> Analog Primitive Devices and Models

A very wide range of different analog primitives enable analog designers to develop sophisticated, high precision, reliable analog and high voltage circuits. See section "Device Parameters" for details.

High performance process modules, well-defined primitive devices and accurate device models are the key success factors for analog and mixed-signal design. Combined with X-FAB's CAE support kit "TheKit" and state of the art design methodologies first right analog mixed-signal designs are reality.

X-FAB supports BSIM3 models as the present SPICE model standard for MOS transistors. Bipolar transistors are modeled using the Gummel-Poon model for a given emitter size. Well resistors have

a non-linear terminal-voltage and bulk-voltage dependence. These resistances have to be simulated with the 3-terminal SPICE JFET model.

Model sets for most popular analog simulators, e.g. Spectre, HSPICE and PSpice are provided.

The same characterization and modeling effort is spent for parasitic devices and 3rd order parameters, which are usually very important for analog design.

The matching behavior of MOS transistors, bipolar transistors, resistors and capacitors is very intensively investigated and characterized. Final matching parameters are extracted for all active and most of passive elements.

> Examples for measured and modeled parameter characteristics

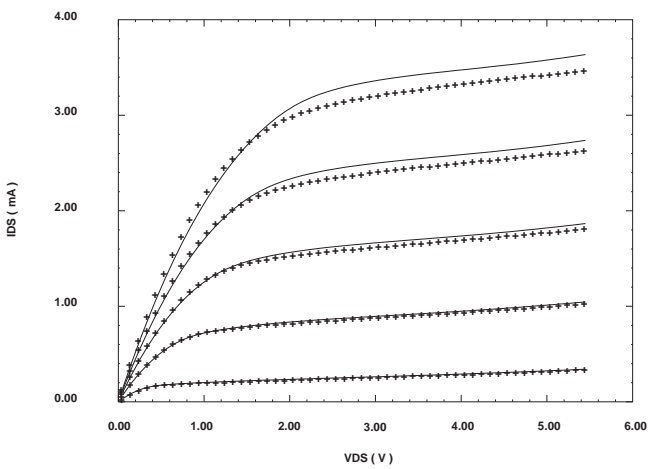


Figure 4: NE output characteristic
 $W/L = 20/1.2$, $V_{GS} = 1.4, 2.3, 3.2, 4.1, 5\text{ V}$
 $V_{SB} = 0\text{ V}$, + = measured, solid line = BSIM3v3 model

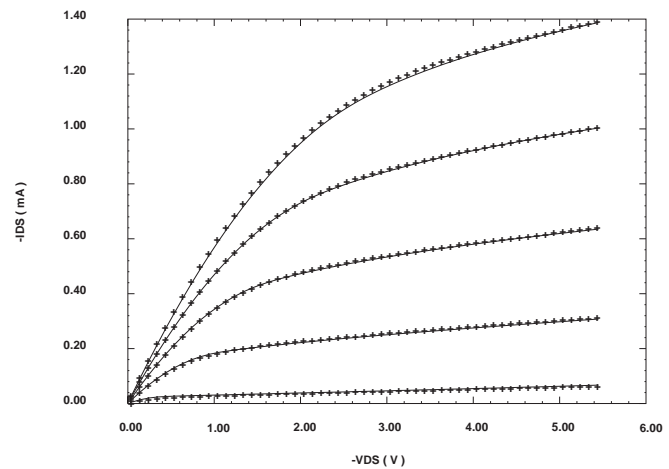


Figure 5: PE output characteristic
 $W/L = 20/1.3$, $-V_{GS} = 1.4, 2.3, 3.2, 4.1, 5\text{ V}$
 $V_{SB} = 0\text{ V}$, + = measured, solid line = BSIM3v3 model

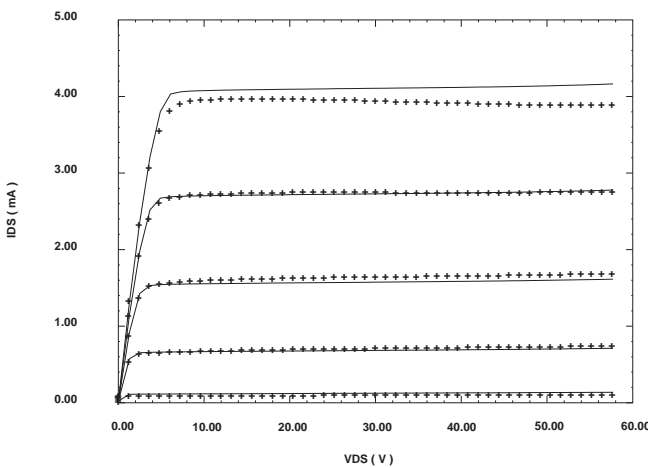


Figure 6: NGD output characteristic
 $W/L = 40/6$, $V_{GS} = 1.4, 2.55, 3.7, 4.85, 5\text{ V}$
 $V_{SB} = 0\text{ V}$, + = measured, solid line = BSIM3v3 model

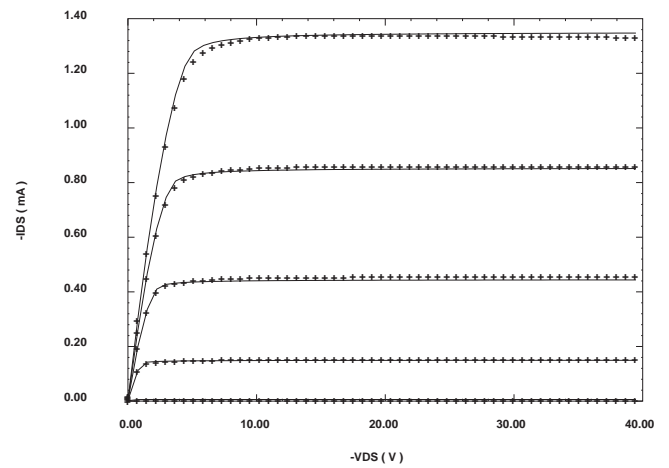


Figure 7: PGD output characteristic
 $W/L = 40/5$, $-V_{GS} = 1.2, 2.4, 3.6, 4.8, 5\text{ V}$
 $V_{SB} = 0\text{ V}$, + = measured, solid line = BSIM3v3 model

> Examples for measured and modeled parameter characteristics (continued)

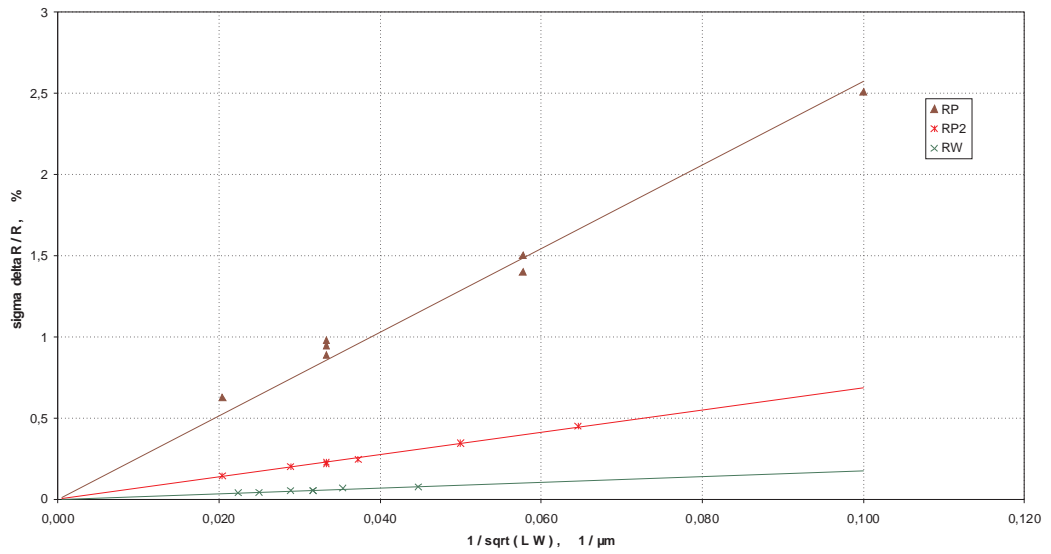


Figure 8: Resistor matching

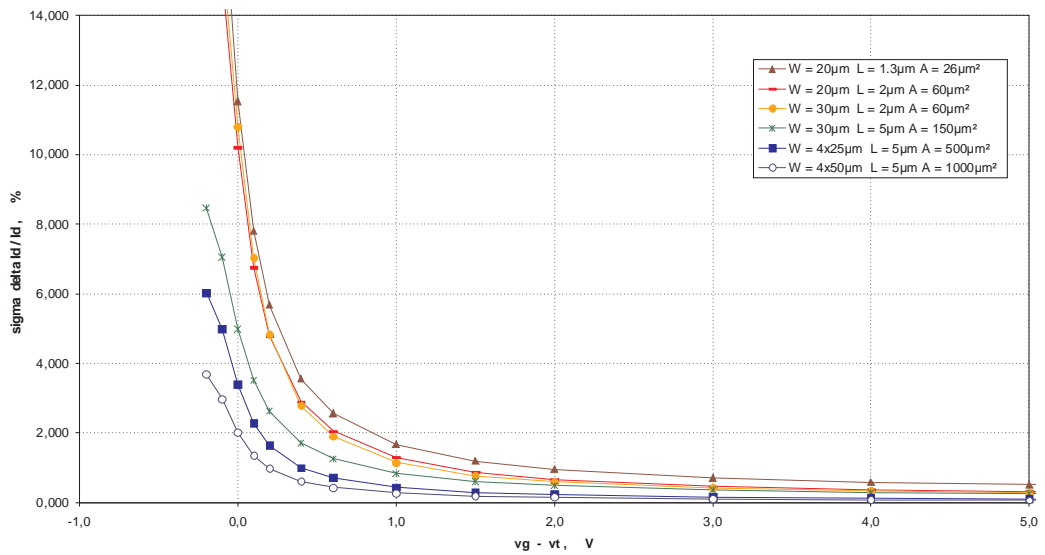


Figure 9: Drain current matching NE

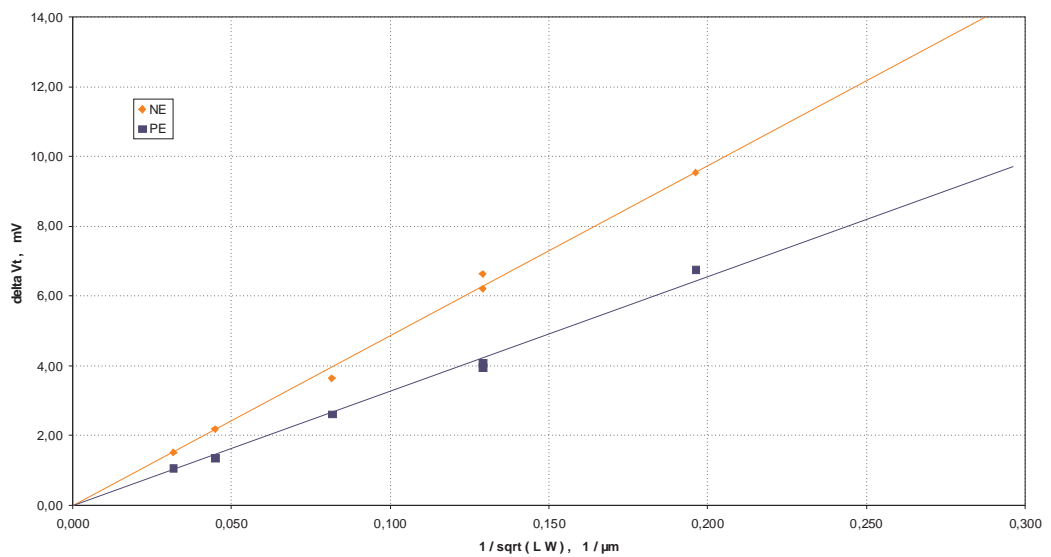


Figure 10: Threshold voltage matching

> Analog Library Cells

Many analog and mixed-signal design projects are started in old technologies because designers want to re-use existing analog cells.

For easy migration to X-FAB's high performance XC10 process an increasing number of general purpose analog cells are provided.

Operational Amplifiers											
Name	V _{OL} [V]	V _{OH} [V]	V _{ICR} [V]	V _{IO} [mV]	A _{VD} [dB]	B ₁ [kHz]	SR [V/μs]	PHM [°]	I _{DD} [μA]	max. Load	Required Module
aopac01	0.1	V _{DD} -1.6	0.3...V _{DD} -1.4	<10	86	400	0.37/0.39	60	21	50pF/1000kΩ	Poly2
aopac02	0.1	V _{DD} -0.1	0.3...V _{DD} -0.3	<10	80	1000	0.85/0.85	68	180	50pF/100kΩ	Poly2
aopac03	0.8	V _{DD} -0.05	1.4...V _{DD} -0.5	<10	81	2850	3.0/2.80	60	170	20pF/30kΩ	Poly2
aopac04	0.01	V _{DD} -0.05	0.4...V _{DD} -1.5	<10	83	700	1.2/1.4	63	52	30pF/1000kΩ	Poly2
aopac05	0.05	V _{DD} -0.05	0.4...V _{DD} -1.5	<10	82	6400	8.2/11	65	585	30pF/10kΩ	Poly2, Metal2
aopac06	0.1	V _{DD} -0.2	0.4...V _{DD} -0.4	<10	107	3000	6.2/5.73	65	345	20pF/10kΩ	Poly2, Metal2
aopac07	0.12	V _{DD} -0.2	0.4...V _{DD} -1.5	<15	87	774	1.1/1.1	61	50	35pF/1000kΩ	Poly2

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Opamps feature a standby mode.

Comparators								
Name	V _{ICR} [V]	T _{PD} for 50mV Overdrive [ns] L → H / H → L	T _{PD} for 500mV Overdrive [ns] L → H / H → L	Conditions C _L [pF]; R _L [kΩ]	Input Offset Voltage [mV]	Supply Current [μA]	Required Process Module	
acmpc01	0.3...V _{DD} -1.5	140 / 140	85 / 85	1.0; 1000	< 10	17	Basic	
acmpc03	1.2...V _{DD} -0.2	710 / 310	-	1.0; 1000	< 10	7	Basic	
acmpc04	0.2...V _{DD} -1.5	340 / 930	-	1.0; 1000	< 10	7	Basic	

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Comparators feature a standby mode.

Bandgaps				
Name	Bandgap Voltage (unloaded) [V]; T=30°C min / typ / max	Temperature Coefficient [ppm / °C]	Supply Current [μA]	Required Process Module
abgpc01	- / 1.269 / -	+100; T= 25°C to T= 85°C	52	Poly2
abgpc02	- / 1.253 / -	-90; T= 24°C to T= 85°C	70	Poly2, Metal2
abgpc03	- / 1.253 / -	-90; T= 24°C to T= 85°C	70	Poly2

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C

Bias Cells						
Name	Current through VBP stage [μA]; @V _{DD} =5V, T=25°C	Temperature Coefficient IVBP [ppm / °C]	Current through VBN stage [μA]; @V _{DD} =5V, T=25°C	Temperature Coefficient IVBN [ppm / °C]	Supply Current [μA]	Required Process Module
abiac01	2.3	-2000; T=25°C to T=85°C	2.5	-2000; T=25°C to T=85°C	12	Poly2
abiac02	0.255	4000; T=25°C to T=85°C	0.270	4000; T=25°C to T=85°C	1.4	Poly2

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Bias Cells feature a standby mode.

Charge Pumps				
Name	Clock Frequency [MHz] min / typ / max	Output Voltage [V]	Supply Current [μA]	Required Process Module
achpc01	0.25 / 1.0 / 2.0	8.75; I _{load} = 0 μA 8.20; I _{load} = 10 μA 7.60; I _{load} = 20 μA	18; I _{load} = 0 μA 34; I _{load} = 10 μA 51; I _{load} = 20 μA	Poly2
achpc02	0.50 / 1.0 / 2.0	18.1; I _{load} = 0 μA 16.4; I _{load} = 2 μA 15.2; I _{load} = 4 μA	15; I _{load} = 0 μA 25; I _{load} = 2 μA 34; I _{load} = 4 μA	Depletion Transistor

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C

> Analog Library Cells (continued)

RC Oscillators				
Name	Frequency [kHz]	Conditions	Supply Current (specified @ $V_{DD}=5V$, $T=25^{\circ}C$) [μA]	Required Process Module
arcoc01	204	@ $V_{DD}=5V$; $T=25^{\circ}C$	55	Poly2
arcoc02	135 / 205 / 376	@ $V_{DD}=5V$; $T=25^{\circ}C$ digital code = 0000 / 1000 / 11111	60 digital code = 1000	Poly2
arcoc03	922	@ $V_{DD}=5V$; $T=25^{\circ}C$	70	Poly2
arcoc04	622 / 925 / 1632	@ $V_{DD}=5V$; $T=25^{\circ}C$ digital code = 0000 / 1000 / 11111	95 digital code = 1000	Poly2
arcoc05	10	@ $V_{DD}=5V$; $T=25^{\circ}C$	1.5	Basic
arcoc06	95	@ $V_{DD}=5V$; $T=25^{\circ}C$	40	Poly2, Metal2
Note: All Parameters are valid for V_{DD} : 4.5 V to 5.5V, T : -40 ...85 °C				

Crystal Oscillators				
Name	Frequency [kHz] min / max	Temperature Range [$^{\circ}C$]	Supply Current (specified @ $T=25^{\circ}C$, $C_{load}=1pF$, $V_{DD}=5V$) [μA]	Required Process Module
axtoc02	1 / 2	-20 ... 70	190 / 210	Metal2
axtoc03	1 / 4	-20 ... 70	405 / 430	Metal2
Note: All Parameters are valid for V_{DD} : 4.5 V to 5.5V, T : -40 ...85 °C				

Power-On-Reset					
Name	High Threshold Voltage [V] min / typ / max	Low Threshold Voltage [V] min / typ / max	Delay Time [μs] typical	Supply Current [μA]	Required Process Module
aporc01	1.56 / 194 / 2.34	-	4	0.02	Basic
aporc02	1.21 / 1.57 / 1.95	1.17 / 1.53 / 1.91	12	0.7	Basic
aporc04	1.92 / 2.37 / 2.88	1.62 / 2.01 / 2.45	14	1	Basic
apogc01	5.48 / 5.55 / 5.59	4.48 / 4.51 / 4.55	-	44	Basic
Note: All Parameters are valid for V_{DD} : 4.5 V to 5.5V, T : -40 ...85 °C					

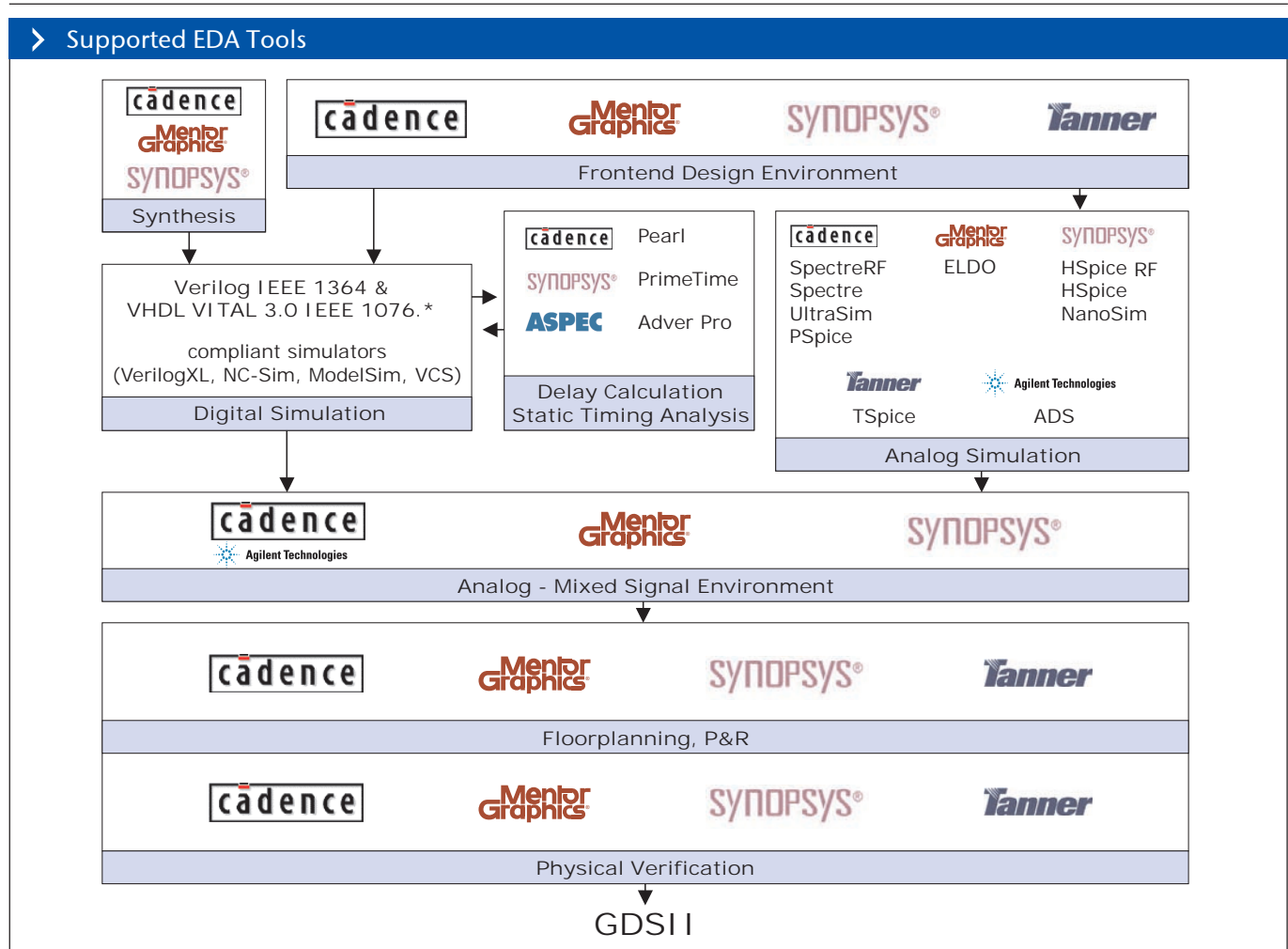
Digital-To-Analog Converters							
Name	Principle	Resolution [Bits]	Accuracy [LSB] INL / DNL	Conversion Time [μs]	High Reference Voltage V_{REFHI} [V] min / max	Low Reference Voltage [V] min	Required Process Module
adacc01	R-2R	8	$\pm 0.3 / \pm 0.3$	2.0; $C_{load}=10pF$	3.2 / V_{DD} ; @ $V_{DD}=5V$	V_{SS}	Poly2, Metal2
adacc02	R-2R	10	$\pm 0.6 / \pm 0.6$	2.0; $C_{load}=10pF$	3.2 / V_{DD} ; @ $V_{DD}=5V$	V_{SS}	Poly2, Metal2
adacc03	voltage-scaling	8	$\pm 0.5 / \pm 0.6$	-	3.2 / V_{DD} ; @ $V_{DD}=5V$	V_{SS}	Poly2, Metal2
Note: All Parameters are typical, V_{DD} : 4.5 V to 5.5V, T : -40 ... 85 °C							

Voltage Regulators							
Name	Output Voltage [V] min / typ / max	Output Current [mA] max	Line Regulation [mV/V]	Load Regulation [mV/mA]	Supply Current [μA]	Supply Voltage Range [V]	Required Process Module
aregc01	3.27 / 3.32 / 3.38	10	20; $I_{load}=0...10mA$	2.0; $I_{load}=0...10mA$	180	4.5 ... 6	Poly2, Metal2
aregc02	3.19 / 3.29 / 3.39	10	10; $I_{load}=0...5mA$	-	390	2.2 ... 3	Poly2, Metal2
Note: All Parameters are typical, V_{DD} : 4.5 V to 5.5V, T : -40 ... 85 °C							

> Analog Library Cells (continued)

Driver							
Name	Nominal Current [mA]	Load Supply Voltage [V] max	Output Resistance [Ω]	Frequency [kHz] max	Overshoot Voltage [V]	Load Inductance [H]	Required Process Module
adrvc01	12; $R_{load} = 1k\Omega$	12	25; $V_{DD} = 5V, T = 25^\circ C$	1.0; $L = 250mH$	25	0.25	Metal2
Note: All Parameters are typical, V_{DD} : 4.5 V to 5.5V, T: -40 ... 85 °C							

High-temperature Detectors							
Name	Threshold Temperature [°C] min / typ / max	Voltage Coefficient of Threshold Temperature [°C/V]	Low Output Voltage [V]	High Output Voltage [V]	Supply Voltage Range [V] min / typ / max	Supply Current [μA]	Required Process Module
atmpc01	139 / 144 / 148	3.4	VSSA	VDDA	4 / 5 / 6	35	Poly2
atmpc02	155 / 160 / 165	3.0	VSSA	VDDA	4 / 5 / 6	35	Poly2
Note: All Parameters are typical, V_{DD} : 4.5 V to 5.5V, T: -40 ... 85 °C							



> X-FAB's IC Development Kit "TheKit"

The X-FAB IC Development **Kit** is a complete solution for easy access to X-FAB technologies. TheKit is the best interface between standard CAE tools and X-FAB's processes and libraries. TheKit is available in two versions, the Master Kit and the Master Kit Plus. Both versions contain documentation, a set of software programs and utilities, digital and I/O libraries which contain full front-

end and back-end information for the development of digital, analog and mixed signal circuits. Tutorials and application notes are included as well. The Master Kit Plus additionally provides a set of general purpose analog functions mentioned in section "Analog Library Cells" and is subject to a particular license.

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