0.6 µm CMOS Process

XC06

MIXED-SIGNAL FOUNDRY EXPERTS

0.6 Micron Modular Mixed Signal Technology

Description

The XC06 Series completes X-FAB's 0.6 Micron Modular Mixed Signal Technology with embedded Non Volatile Memory and High Voltage options. EEPROM blocks up to 32 kbit as well as Flash memories up to 512 kbit can be integrated in standard cell, semi-custom and full custom designs for Industrial, Automotive and Telecommunication products.

MOS as well as Bipolar Transistors are available with Breakdown Voltages up to 100V.

The 5 V CMOS core is compatible in Design Rules and Transistor Performance with state of the art 0.6 µm CMOS Processes.

For analog applications several capacitor and resistor devices are realized, using the Double-Poly-Non-Volatile-Memory architecture.

Reliable design rules, precise SPICE models, analog and digital libraries, IP's and development kits support the process for major CAE vendors.

Key Features

- 0.6-micron single poly, double metal N-well CMOS basic process
- Triple metal option for high density circuits
- **NEW**: *Thick 3rd layer metal for higher drive currents*
- Different medium and high voltage options with 8 to 40 V DC operating conditions for NMOS and PMOS transistors
- Extended high-voltage modules upto 60V DC operating conditions - NMOS, PMOS and DMOS
- **NEW**: *HV devices with low RDSon*
- ***NEW**: SCHOTTKY diode module*
- ***NEW**: ISOMOSA module for isolated triple well 5V NMOS*
- ***NEW**: ROM module for implantation programmed ROM cells and certain capacitors*
- ***NEW**: PIN diode for high speed optical receivers*
- ***NEW**: MOS varactor diode*
- ***NEW**: dedicated JNFET for low noise applications*
- ***NEW**: additional protection diodes*
- Triple well isolated CMOS transistors
- Different bipolar transistors
- Double Poly-Si capacitor
- Linear poly capacitor module
- High-resistive Poly-Si resistor
- High precision BSIM3V3 SPICE models for CMOS and Gummel Poon model for bipolars
- Special high voltage models (BSIM3v3_XHV) for precise simulations in higher voltage ranges
- Excellent analog performance with accurate device matching
- embedded EEPROM with ready to use EEPROM blocks
- embedded Flash memory with ready to use Flash blocks
- Different digital core cell libraries optimized for speed, low power, low noise or , inherited power connection concept
- Junction insulated digital low power library (for 3.3V applications)
- High density RAM, DPRAM and ROM blocks
- Analog IP library
- About 2500/4500 effective gates per mm^2 (2ML/3ML)
- 5V I/O cell libraries with CMOS / TTL interfacing capability
- Electrostatic discharge (ESD) protection in accordance with MIL-STD
- Optional ESD layer for higher ESD protection
- Design kits for major EDA tools
- OPTO module to increase optical sensitivity of photo diodes
- ESD module to increase ESD performance
- Depletion module
- OTP option (zener zapping, fuses)

Applications

- Automotive electronics, communication, industrial and consumer market
- Low-power mixed signal circuits
- High precision mixed signal circuits
- Power Management circuits
- Mixed signal embedded systems; systems on a chip (SOC)
- Analog front ends for sensors
- Circuits with integrated high voltage I/O's and voltage regulators

Quality Assurance

X-FAB spends a lot of effort to improve the product quality and reliability and to provide competent support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, QS 9000, VDA 6, ISO TS 16 949 and other standards.

Deliverables

- PCM tested wafers
- Optional production services: wafer sort
- Optional Engineering services: Multi Project Wafer (MPW) and Multi Layer Mask Service (MLM)
- Optional Design services; e.g. feasibility studies, place & route, synthesis, custom block development

Digital Libraries

- Foundry-specific optimized libraries
- Standard core library for high speed digital blocks
- Low-power library, 50% less power, 40% less area
- Low-noise library with separate bulk contacts for reduced substrate noise
- IEEE 1365 Verilog simulation models
- IEEE 1076.4 VHDL-VITAL simulation models
- Synthesis libraries
- Macrofunction and IP's on request
- RAM, DPRAM, ROM
- Zener zaps

Analog Libraries

- Operational Amplifiers
- Comparators
- RC Oscillators
- Bandgaps
- Bias Cells
- Power-On-Reset
- Charge Pumps
- ADC / DAC

Primitive Devices

- NMOS/PMOS Transistors (5V to 60V)
- Bipolar Transistors
- Diodes
- Capacitors
- Poly silicon and diffusion resistors
- Optical diodes

Ready to use Memory Blocks

- ROM
- RAM
- DPRAM
- EEPROM
- Flash

Process Family

module name	no. of masks	remarks	typical primitive devices applications
CMOS core module	11	5V CMOS core module P-epi wafer, single poly, double metal	5V NMOS/PMOS, analog applications

This main module can be combined with one or more of the following additional modules:

module name	no. of add. masks	remarks	typical primitive devices applications
ESD	1	ESD implant module specific implant for ESD protection	5V ESD-NMOS 5V-I/O's with improved ESD robustness
MIDOX	2	mid-oxide module, additional thick gate oxide as base for all MV / HV elements	medium voltage NMOS (16V) and high voltage NMOS (60V), analog applications
PMV *)	1	medium voltage p-channel module p-channel MV/HV threshold implant	medium voltage PMOS with or without graded drain (up to 18V), analog applications
NGD *)	1	extended medium voltage n-channel module n-channel graded MV drain implant	medium voltage NMOS with graded drain (22V) analog applications
DEPL *)	1	medium/ high voltage depletion NMOS module, specific transistor implant	medium (16V) and high (60V) voltage depletion NMOS, analog applications
PGD *)	1	high voltage graded PMOS module PGD implant	high voltage graded PMOS (33V),additional bipolars, analog applications
HVS *)	1	high voltage modulehigh voltage shallow N-well	high voltage PMOS (70V) and extended high voltage NMOS (100V), additional bipolar, analog applications
HVE *)	2	extended high voltage modulehigh voltage deep N-well and P-well	extended high voltage DMOS (80V), additional bipolars, analog applications
PHVE *)	1	extended high voltage PMOS module, specific transistor implant	extended high voltage PMOS (100V), analog applications
ISOMOS **)	3	triple well isolated CMOS module, specific transistor implant	low voltage NMOS (3.3V) / PMOS (5V) with isolated bulk, low noise, digital or analog applications
ISOMOSA **)	2	triple well isolated CMOS module, specific transistor implant	low voltage NMOS/ PMOS (5V) with isolated bulk, analog applications
CAPRES	2	capacitor/ resistor moduledouble poly	double poly capacitor, poly0 resistors (high resistive and/or low TC) for analog applications
LINC *)	1	linear capacitor modulelinear capacitor implant	linear poly capacitor analog applications
SCHOTTKY	1	Schottky diode module process flow	Schottky diode
ROM	1	ROM specific implantation layer	implantation programmed ROM cell (no compiler available), additional capacitors
EEPROM *)***)	2	EEPROM module EEPROM cell	ready-to-use EEPROM memory blocks, implantation programmed ROM cell, additional capacitors
FLASH *)***)	3	Flash module, Flash cell	ready-to-use Flash memory blocks
OPTO	1	optical window module oxide window for photo diodes	optical applications
PIN *)	1	PIN diode module, use of special doped epi wafers	PIN diode (n+/p--/p+) for optical applications (3.3V/ 5V)
METAL3	2	triple metal moduleadditional metal layer	more complex wiring
THKMET	2	thick third metal module, additional thick metal routing	reduced internal resistance, capable for higher currents
PIMIDE	1	polyimide module resilient barrier layer on top of passivation	wafer overcoat for stress relief and passivation protection

*) Note: This module requires the addition of other sub modules as listed in the table below.
) Note: ***The number of additional masks for these modules depends on the combination with other modules.*
***) Note: For ready-to-use memory blocks and latches, refer to the memory block or latch specification regarding the process module combination which is required for the specific block or latch.

Process Family *(continued)*

Restrictions for Module Combinations

The following restrictions exist for module combinations:

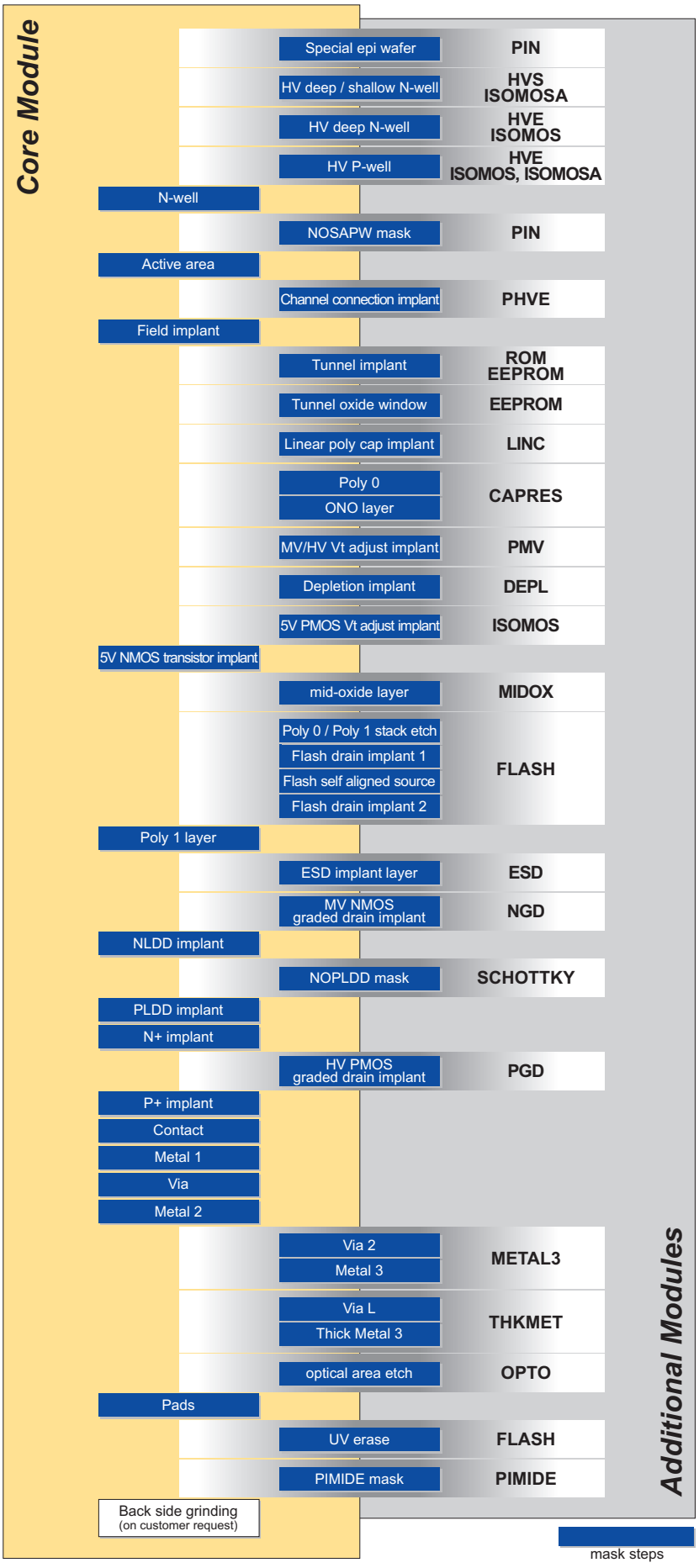
Module Name	use of the module also requires the use of following modules	use of the module is not available in combination with the following modules
ESD		PIN
MIDOX		PIN
PMV	MIDOX	PIN
NGD	MIDOX	PIN
DEPL	MIDOX	PIN
PGD	MIDOX, PMV	PIN
HVS	MIDOX	PIN
HVE	MIDOX	PIN
PHVE	MIDOX, HVS	PIN
ISOMOS		PIN
ISOMOSA		PIN
LINC	CAPRES	
SCHOTTKY		PIN
ROM		EEPROM *)
EEPROM	MIDOX, PMV, NGD, CAPRES	ROM *), PIN, THKMET
FLASH	MIDOX, PMV, NGD, CAPRES, EEPROM, METAL3	PIN, THKMET
OPTO		THKMET
PIN	OPTO	ESD, MIDOX, PMV, NGD, DEPL, PGD, HVS, HVE, PHVE, ISOMOS, ISOMOSA, SCHOTTKY, EEPROM, FLASH, THKMET
METAL3		THKMET
THKMET		EEPROM, FLASH, OPTO, PIN, METAL3

*) Note: The EEPROM module includes the ROM module. Therefore it is not possible to select both modules ROM and EEPROM simultaneously. To get the complete performance of both modules, the EEPROM module must be selected only.

Medium Voltage and High Voltage Modules: Application Recommendations

Technology option	Recommandation
MIDOX	mid-oxide module is the base for all elements with higher than 5V operating voltage it already delivers a 60V NHV transistor
MIDOX+PMV+NGD	are necessary for EEPROM / Flash (switch programming voltages up to 20V)
MIDOX+PMV+PGD	gives possibility for 14V automotive board net because 60V NHV, 33V PGHV and bipolars are available
MIDOX+HVS	gives 60V NHV and 70V PHV, 100V NHVE and extended high voltage qpvhea
MIDOX+HVS+HVE	gives 80V ndse, 85V ndsea for low and high side switches
MIDOX+HVS+HVE+PHVE	80V PHVEA
ISOMOS, ISOMOSA	gives the possibility for triple well isolated low voltage CMOS transistors

Main Process Flow



Schematic Cross Sections

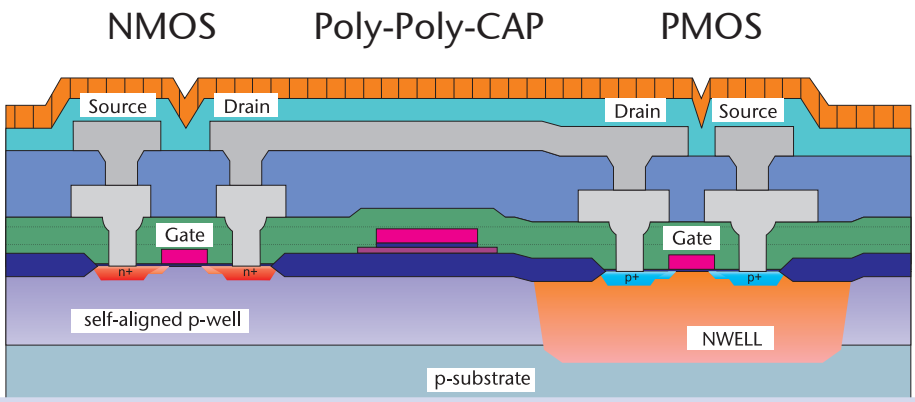


Figure 1: 5V devices

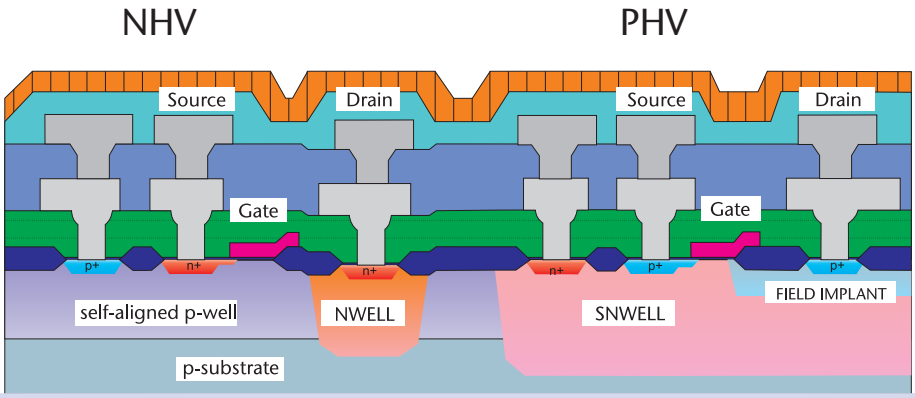


Figure 2: High Voltage devices

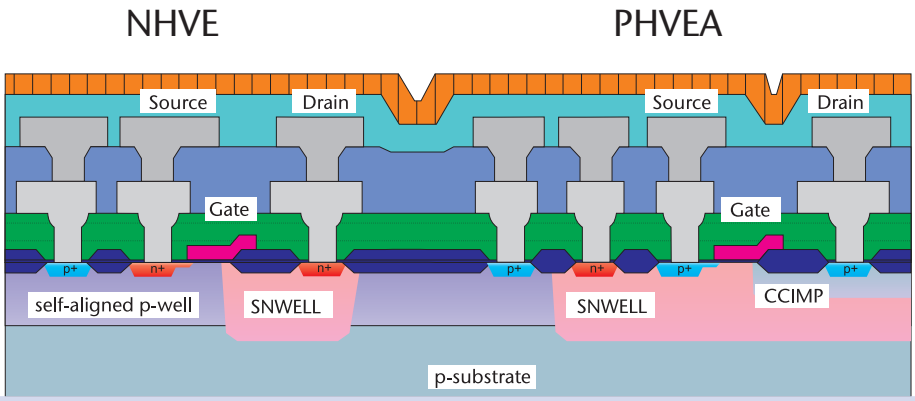


Figure 3: Extended High Voltage device NHVE and low RDSon device PHVEA

Basic Design Rules

Mask	Width [µm]	Spacing [µm]
Standard N-well	4	4.8
HV deep N-well	6	15
Isolated P-well	6	5
Active Area	0.6	1.2
Poly-Silicon Gate	0.6	0.8
Contact	0.6	0.6
Metal 1	0.9	0.8
Via 1	0.7	0.6
Metal 2	0.9	0.8
Via 2	0.7	0.6
Metal 3	1.2	1.0
ViaL	0.7	0.7
METL	2.5	2.5

Device Parameters

The following devices can be used for circuit designs. They are well characterized and part of a primitive device library. The device names correspond with the SPICE model names.

Different reliability tests gave the maximum allowed operating conditions; Values in brackets denote absolute maximum ratings. See also the availability with different options.

Active Devices (typical data)

MOS Transistors (selection)							
Device	Device Name	Avail. only with module	VT [V]	IDS@VGS [µA/µm@V]	|BVDSS| [V]	Max. |VDS| [V]	Max. |VGS| [V]
NMOS 5V	nmos4	CORE	0.87	470@5	13	5.5	5.5
PMOS 5V	pmos4	CORE	-0.90	230@5	12	5.5	5.5
NMOS with ESD implant	nesd	ESD	0.9	520@5	12	5.5	5.5
isolated NMOS	nmosi	ISOMOS	0.88	235@3.3	13	3.6	5.5
isolated NMOS, 5V	nmosia	ISOMOSA	0.92	420@5	14	5.5	5.5
isolated PMOS	pmosi	ISOMOS	-0.90	100@3.3	12	5.5	5.5
NMOS medium voltage	nmv	MIDOX	0.9	485@12	16	8	18
NMOS medium voltage low doped drain	ngmv	NGD	0.88	465@12	22	12	18
PMOS medium voltage	pmv	PMV	-0.90	185@12	13	8	18
PMOS medium voltage low doped drain	pgmv	PMV	-0.90	150@12	18	12	18
NMOS high voltage	nhv	MIDOX	0.82	230@12	62	30	18
NMOS high voltage depletion	nhvd	DEPL	-1.25	250@12	60	30	18
PMOS high voltage graded	pghv	PGD	-0.85	125@12	33	25	18
PMOS high voltage	phv	HVS	-0.86	155@12	75	40	18
Low RDSon, high voltage PMOS	phva	HVS	-0.85	190@12	60	40	18
NMOS extended high voltage	nhve	HVS	0.77	210@12	110	60	18
Low RDSon, extended high voltage NMOS	nhvea	HVS	0.77	220@12	80	60	18
PMOS extended high voltage	phve	PHVE	-0.93	105@12	100	60	18
extended high voltage PMOS, low on-resistance	phvea	PHVE	-0.85	155@12	80	60	18
Step-NDMOS extended high voltage	ndse	HVE	0.86	280@12	80	50	18
Low RDSon, extended HV Step-NDMOS	ndsea**)	HVS & HVE *)	0.80	230@12	85	35***)	18
High voltage junction FET	jnfet	HVS & HVE *)	4.3	950	65	40	5

*) Other module combinations possible.
**) Use ndsea only for digital applications.
***) For 20000 sec 50V.

Device Parameters *(continued)*

Active Devices (typical data) *(continued)*

MOS High Voltage Transistors - Comparison of RDSON				
Transistor	RON*A [1] [mΩ*mm²]	Transistor	RON*A [1] [mΩ*mm²]	RON reduction
NHV	118			
PHV	375	PHVA	205	45%
NHVE	205	NHVEA	142	30%
PHVE	691	PHVEA	284	59%
NDSE	207	NDSEA	146	30%

[1]) VGS = 18V, temperature = 21°C

Bipolar Transistors (selection)						
Device	Device Name	Avail. only with module	BETA	VA [V]	|BVCEO| [V]	|Max VCE| [V]
Vertical PNP	qpv5	CORE	12	> 100	>7	5.5
Lateral PNP	qpa	CORE	50	24	>7	5.5
Vertical NPN	qnvo	PGD	53	14	20	5.5
Vertical HV PNP (collector on psub)	qpvh	PGD	35	> 100	62	40
Vertical ext. HV NPN	qnve	HVE	230	13	14	5.5
Vertical ext. HV PNP (collector on psub)	qpvhe	HVE	80	> 150	100	60
Vertical ext. HV PNP (collector on psub)	qpvhea	HVS	220	> 70	90	60

Passive Devices (typical data)

Capacitors (selection)							
Device	Device Name	Avail. only with module	Area Cap [fF/µm²]	BV [V]	Voltage Coefficient [%/V]	Temp. Coefficient [10^{-3}/K]	Max VCC [V]
poly0/ poly1 cap	cpoly	CAPRES	1.87	20	2.5	0.1	8
linear poly0/ poly1 cap	cpolylin	LINC	1.02	30	0.0027	0.04	8
poly1/ metal1/ metal2 cap	csandwt	CORE	0.070				60
deep N-well/poly1/metal1/metal2 cap	csandw	HVE	0.13				60
poly1/metal1/metal2/metal3 cap	csandwtm	METAL3	0.10				60
poly1/ tunnel implant cap	ctm	EEPROM	0.80	40	0.8	0.04	18
poly1/ tunnel implant cap in N-well	ctmw	EEPROM	0.80	40	0.8	0.04	18
tunnel implant/poly0/poly1 cap	ctp0p1	EEPROM	2.58	20	2.5	0.1	8

Varactor					
Device	Device Name	Avail. only with module	Capacitance @ +1V, 100kHz [fF]	Capacitance @ -1V, 100kHz [fF]	Minimum Q-factor @ 500MHz
MOS Varactor	mosvc	CORE	52	15	25

Device Parameters *(continued)*

Passive Devices (typical data) *(continued)*

Resistors (selection)						
Device	Device Name	Avail. only with module	RS [Ω/□]	Thickness or junction depth [µm]	Temp. Coefficient [10^{-3}/K]	max VTB [V]
N+ resistor in p-substrate	rdiffn3	CORE	57	0.6	1.5	8
N+ resistor in P well	rdiffnpw3	HVE	57	0.6	1.5	3.6/5.5
P+ resistor in N well	rdiffp3	CORE	115	0.4	1.3	8
P+ resistor in deep N well	rdiffpdnw3	HVE	115	0.40	1.3	8
N-well resistor	rnwell3	CORE	900	3.5	6.8	20
poly1 resistor	rpoly1	CORE	17	0.45	1.1/1.0 *)	60
deep N-well resistor	rdnwell3	HVE	580	8	6.8	60
P-well resistor in deep N-well	rpwell3	HVE	5300	1.6	5.8	40
low temp. coefficient poly0 resistor	rpoly0	CAPRES	580	0.18	-0.20/0.80 *)	60
high resistive poly0 resistor	rpolyh	CAPRES	3500	0.18	-3.3/10.9 *)	60
Metal	rm1	CORE	0.085	0.67	3.3	>60
	rm2	CORE	0.045/0.075	1.0/0.8	3.3	>60
	rm3	CORE	0.045	1.0	3.3	>60
	rm3l	THKMET	0.012	2.45	3.7	>60

*) linear / quadratic temperature coefficient

Programmable Devices (selection)					
Device	Device Name	Available with module	Zener breakdown voltage [V]	max. Iread [mA] - un-zapped state-	max. Iread [mA] - zapped state -
Zener Zap	dzap	CORE	4.3	0.2	0.2
Device	Device Name		Un-programmed fuse resistance [Ω]	Programmed fuse resistance [MΩ]	Max. Vread [V] - un-programmed state -
Poly Fuse	pfuse	CORE	150	10	1

Diodes (selection)					
Device	Device Name	Available with module	Forward voltage [V]	max. forward current [mA]	max. reverse voltage [V]
Schottky diode	dsa	SCHOTTKY	0.38	2	12
Device	Device Name	Available with module	Area junction capacitance @2.5 V [fF/µm²]	Area dark current [fA/µm²]	Max. spectral sensitivity @ 760 nm [A/W]
Pin diode *)	dpin	PIN	0.015	0.02	0.36

*) Notes: The value is related to an antireflective coating (ARC layer). The adaption of the ARC layer to special customer requirements is possible and might cause parameter changes.

Protection Diodes (selection)					
Device	Element	Available with module	Breakdown voltage [V]	Leakage current [pA/µm]	max. breakdown current [µA/µm]
18V n+ protection diode	dnnw18	CORE	23	12	5
30V n+ protection diode	dnnw30	CORE	35	21	5
40V n+ protection diode	dnnw40	CORE	45	28	5
18V p+ protection diode	dpwd18	HVE or ISOMOS	-25	23	5
30V p+ protection diode	dpwd30	HVE or ISOMOS	-36	33	5
40V p+ protection diode	dpwd40	HVE or ISOMOS	-46	52	5

Device Parameters *(continued)*

Passive Devices (typical data) *(continued)*

Memory Blocks		
EEPROM		
Ready-to-use EEPROM blocks up to 32 kbit with internal charge pump for programming modes		
Power supply range:	1.8 to 6.0 V	
Current consumption:	< 120 µA (typical)	
Temperature range (read mode):	-40 to +150 °C	
Erase / write time:	min. 4 ms	
Number of erase / write cycles	min. 1 x 10^5 @ 25°C	
	min. 1 x 10^4 @ 125°C	
Data retention:	10 years @ 125°C	
Data access time:	< 0.8 µs	
Area (example): embedded block	256 x 16 bit:	0.60 mm² (incl. charge pump)
	1k x 32 bit:	2.27 mm² (incl. ECC)
Flash		
Ready-to-use Flash blocks up to 32k x 16 bit (512 kbit) with ECC logic to increase reliability		
Power supply range:	5.0 ± 0.5 V	
External programming voltages:	VGS = 12.0 ± 0.25V	
	VPD = 8.5 ± 0.25V	
Temperature range (read mode):	-40 to +125 °C	
Temperature range (erase and write mode):	0 to +70 °C	
Erase time (flash):	max. 50 pulses with 1ms each	
Write time (per word):	max. 30 pulses with 5µs each	
Number of erase / write cycles:	min. 1x10^3 (0 to +70 °C)	
Data retention:	10 years @ 85°C	
Data access time:	50 ns	
Embedded block area (examples):	32k x 16 (512kbit):	10.67 mm² (incl. ECC)
	8k x 16 (128kbit):	4.00 mm²
	(6k + 2k) x 16 (128kbit):	4.00 mm² (no ECC checking)
Note: General characteristics. For detailed values check the datasheet of the available blocks		

Flash: All Flash IP are available either with IEEE1149.1 TAP or IEEE P1500 WSP interface. By using the TAP interface, a Programmer ToolKit is available, which consists of programmer hard- and software. The hardware requires USB interface, the software is running under MS OS, like Windows2000 or WindowsXP. The Programmer ToolKit allows programming, debugging and testing of Flash IP's in the embedded environment.

Digital Core Library Cells

X-FAB provides five different core libraries optimized for most typical applications in mixed signal ASIC. The usage of these libraries achieves best in class results of area, spead, low power and low noise.

- The standard core library is optimized for best synthesis results in high speed applications.
- The standard library with separated bulk to achieve reduced noise induced by switching of digital gates.
- The low power library is designed to achieve best results for low power and small area.
- The fourth library is a low power library which uses separate bulk contact to reduce the influence of supply switching noise to substrate.
- The junction isolated library was developed to reduce supply noise inside the substrate and for use in higher digital voltage levels. It is a low power library.

Digital Core Library Cells *(continued)*

Name	Category	Density [1]	@ r_factor [2]	Main features
D_CELLS	standard	ML2: 1.9 ML3: 3.3	ML2: 2.86 ML3: 1.67	high speed
D_CELLS_B	standard / low noise	ML2: 1.6 ML3: 2.8	ML2: 2.86 ML3: 1.67	high speed, less noise
D_CELLSL	low power	ML2: 2.6 ML3: 4.6	ML2: 2.86 ML3: 1.67	min area, min power consumption
D_CELLSL_B	low power / low noise	ML2: 2.1 ML3: 3.6	ML2: 2.86 ML3: 1.67	min noise, min power consumption
D_CELLSL_JI	low power / low noise junction isolated	ML2: 2.1 ML3: 3.6	ML2: 2.86 ML3: 1.67	junction isolated, min noise, min power consumption [3]

1) average value: kGE/mm² (GE = NAND2 Gate Equivalent)
ML2: 2 metal layer routing
ML3: 3 metal layer routing

2) average value: r_factor = Routing_factor
Place&Route_area = Cell_area * Routing_factor

3) Additional xc06 process module ISOMOS is needed, only usable for VDD = 3.3V +/- 10% (related to the bulk NMOSI), bulk NMOSI can be connected to voltage supply 0V ... 55V

Digital I/O Cells

The digital I/O libraries contain a comprehensive range of I/O cells divided into distinct inputs, outputs and bidirectionals with variants for single voltage and dual voltage devices.

The digital I/O library has the following features:

- I/O cell libraries are available for pad-limited or core-limited designs and suitable for all available additional technology modules
- I/O cells are optimized for 5.0V operating voltage and are fully functional down to 3.3V with derated output current and speed.
- The TTL and CMOS level detection circuits use low noise power rails
- CMOS/TTL Schmitt trigger cells optimized for 5V or 3.3V operating voltage are available
- All input and output cells are non-inverting
- Inputs are available with gated pull-up, pull-down and hold option
- Cell height of pad-limited I/O cells is 430µm and minimum pitch is 110µm, cell height of core-limited I/O cells is 231.3µm and the pad pitch is variable
- Outputs are available with selectable speeds to maintain low noise independent from DC output drive and can be configured as tri-state, bi-state, open drain or open source

		Pad Limited I/O Cells	Core Limited I/O Cells
Input		CMOS or TTL Level	CMOS or TTL Level
Schmitt Trigger Cells CMOS/TTL		■/■	■/■
Input Option	Gated Pull-up / Gated Pull-down	■	■
	Input Hold	■	■
	Gated CMOS Input	■	
	NAND Tree	■	■
Output		Tri-state Output	Tri-state Output
	Output Drive	1, 2, 4, 8, 16, 20mA	1, 2, 4mA
	Slew Rate Control	■	
	Configurations	Bi-state Output Tri-state Output Open Drain Output Open Source Output	Bi-state Output Tri-state Output Open Drain Output Open Source Output
Cell Size	Cell Height	430.0µm	231.3µm
	Cell Width / Pad Pitch	110.0µm	Input cells 211.2µm Output and Bidirectional cells 292.8µm Special analog I/O cells 211.2µm
ESD Robustness		2kV (HBM)	2kV (HBM)

Analog Primitive Devices and Models

A very wide range of different analog primitives enable analog designers to develop sophisticated, high precision and reliable analog circuits.

High performance process modules, well defined primitives devices and accurate device models are key success factors for analog and mixed-signal design. Combined with X-FAB's CAE support kit "TheKit" and state of the art design methodologies first right mixed-signal designs are reality.

X-FAB supports BSIM3 models as the present SPICE model standard for MOS transistors. Bipolar transistors are modeled using the Gummel-Poon model. Well resistors have a non-linear terminal-voltage and bulk-voltage dependence. These resistances have to be simulated with the 3-terminal SPICE JFET model.

Model sets for most popular analog simulators, e.g. Spectre, HSPICE, ELDO and PSPICE are provided.

The same characterization and modeling effort is spent for parasitic devices and 3rd order parameters which are usually very important for analog design.

The matching behavior of MOS transistors, bipolar transistors, resistors and capacitors is very intensively investigated and characterized. Final matching parameters are extracted for all active and most of passive elements. These parameters are used at simulator model implementation for Monte Carlo simulation.

Examples for measured and modeled parameter characteristics

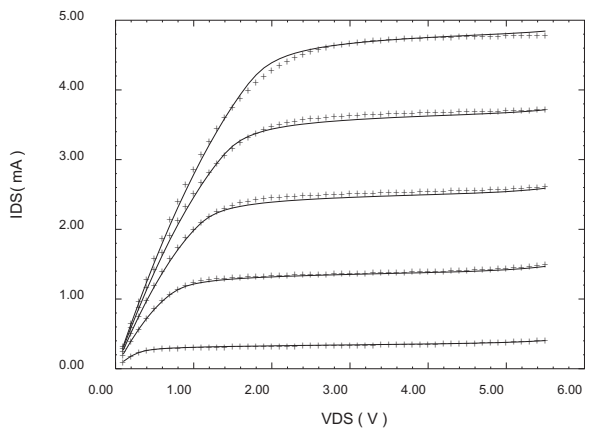


Figure 4: NMOS4 output characteristic of a typical wafer.
W/L = 10/0.6, VGS = 1.4, 2.3, 3.2, 4.1, 5 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

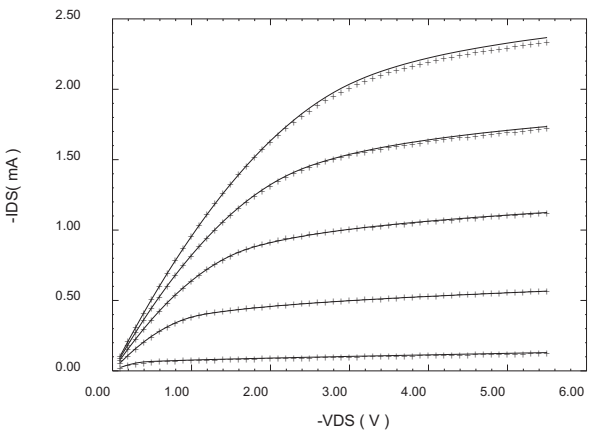


Figure 5: PMOS4 output characteristic of a typical wafer.
W/L = 10/0.6, -VGS = 1.4 ,2.3 ,3.2 ,4.1, 5 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

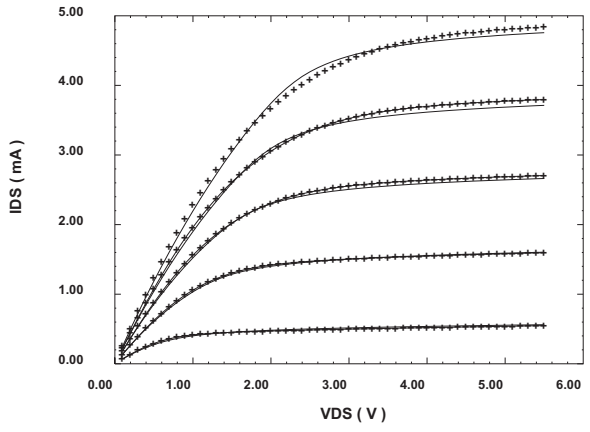


Figure 6: NMV output characteristic of a typical wafer.
W/L = 10/1.2, VGS = 2.67, 5, 7.33, 9.66, 12 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

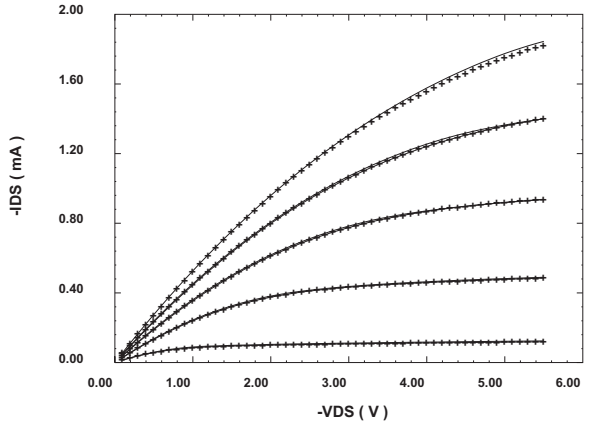


Figure 7: PMV output characteristic of a typical wafer.
W/L = 10/1.2, -VGS = 2.67, 5, 7.33, 9.66, 12 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

Examples for measured and modeled parameter characteristics *(continued)*

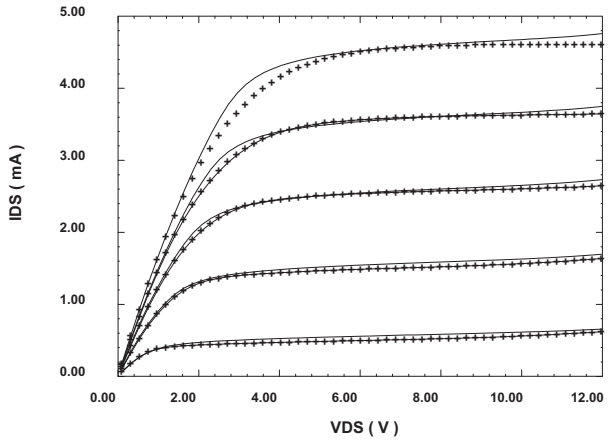


Figure 8: NGMMV output characteristic of a typical wafer.
W/L = 10/1.4, VGS = 2.67, 5, 7.33, 9.66, 12 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

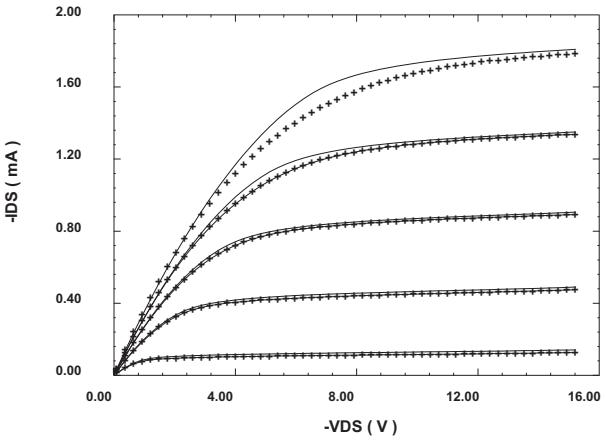


Figure 9: PGMMV output characteristic of a typical wafer.
W/L = 10/1.2, -VGS = 2.67, 5, 7.33, 9.66, 12 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

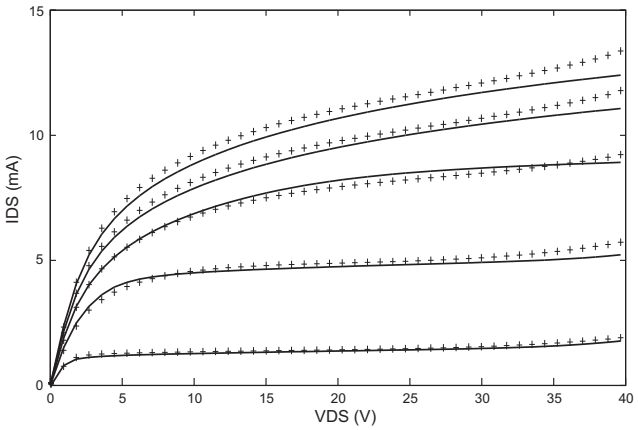


Figure 10: NHV output characteristic of a typical wafer.
W/L = 50/4, VGS = 2.67, 5, 7.33, 9.66, 12 V, VSB = 0 V,
+ = measured, solid line = BSIM3v3_XHV model

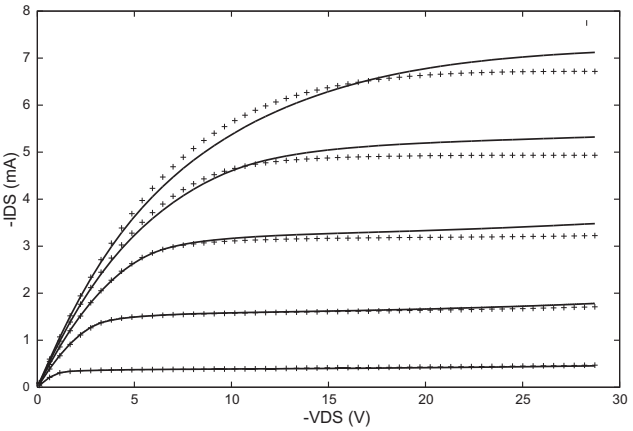


Figure 11: PGHV output characteristic of a typical wafer.
W/L = 50/5, -VGS = 1.4, 2.3, 3.2, 4.1, 5 V, VSB = 0 V,
+ = measured, solid line = BSIM3v3_XHV model

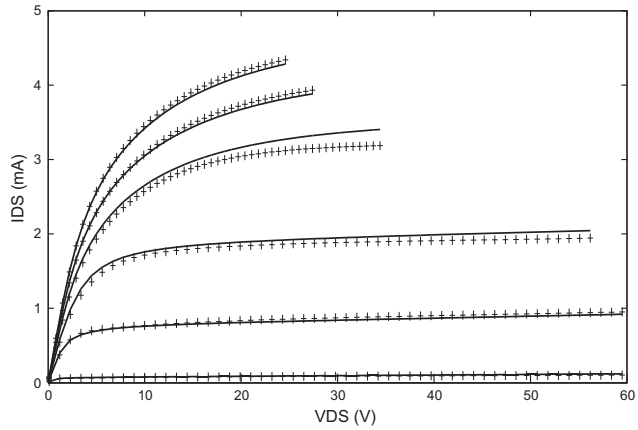


Figure 12: NHVE output characteristic of a typical wafer.
W/L = 20/3.5, VGS = 1.4, 3.2, 5, 7.33, 9.66, 12 V, VSB = 0 V,
+ = measured, solid line = BSIM3v3_XHV model

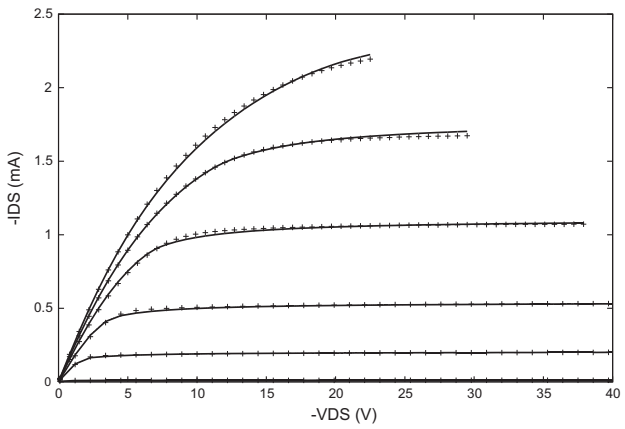


Figure 13: PHVE output characteristic of a typical wafer.
W/L = 20/4, -VGS = 1.4, 3.2, 5, 7.33, 9.66, 12 V, VSB = 0 V,
+ = measured, solid line = BSIM3v3_XHV model

Examples for measured and modeled parameter characteristics *(continued)*

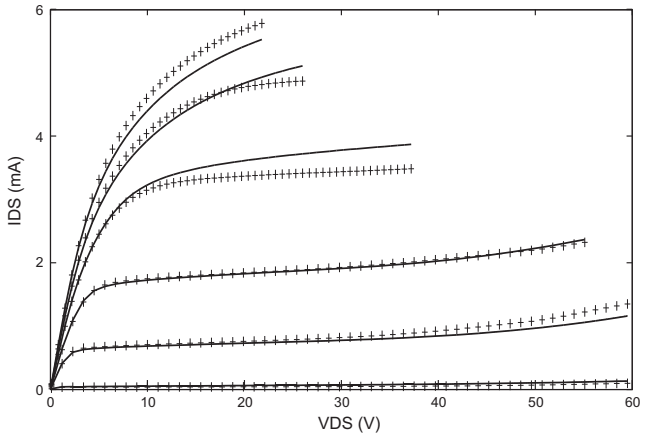


Figure 14: NDSE output characteristic of a typical wafer. W/L = 20/2, VGS = 1.4, 3.2, 5, 7.33, 9.66, 12 V, VSB = 0 V, + = measured, solid line = BSIM3v3_XHV model

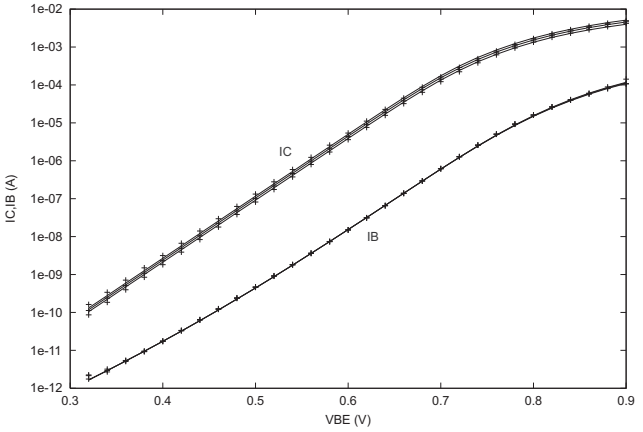


Figure 15: Gummel plot of vertical NPN bipolar transistor QNVE for a typical wafer. LE = 20µm, VCE= 1, 3, 5V, + = measured, solid line = SPICE model

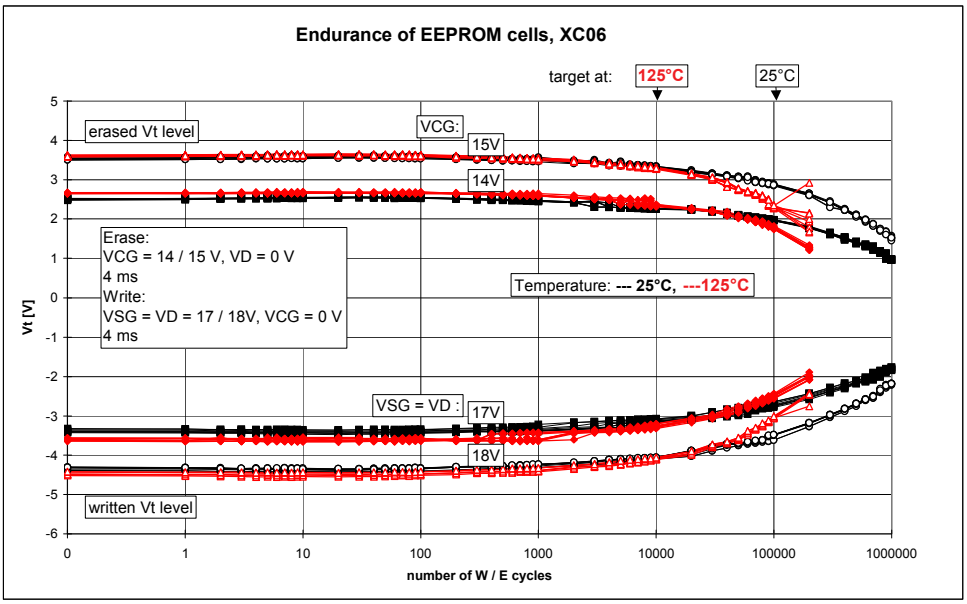


Figure 16: Endurance of EEPROM cells

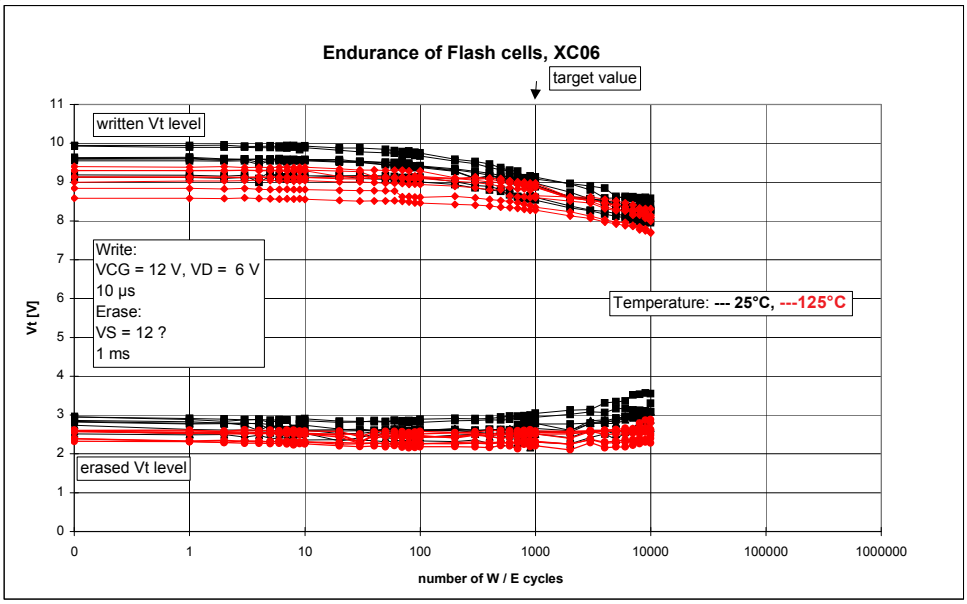


Figure 17: Endurance of Flash cells

Analog Library Cells

Many analog and mixed-signal design projects are started in old technologies because designers want to re-use existing analog cells.

For easy migration to X-FAB's high performance XC06 process an increasing number of general purpose analog cells are provided.

Operational Amplifiers

Name	V_{OL} [V]	V_{OH} [V]	V_{ICR} [V]	V_{IO} [mV]	A_{VD} [dB]	B_1 [kHz]	SR [V/µs]	PHM [°]	I_{DD} [µA]	max. Load	Required Module
aopac01	0.02	V_{DD}-1.8	0.1 ... V_{DD}-1.26	<10	107	131	0.1 / 0.1	60	15	100pF/1000kΩ	CORE
aopac02	0.05	V_{DD}-0.05	1.28 ... V_{DD}-0.26	<10	96	3350	5.4 / 5.6	65	530	50pF/50kΩ	CAPRES
aopac03	0.67	V_{DD}-0.05	1.19 ... V_{DD}-0.19	<10	99	2600	2.0 / 1.05	60	160	25pF/30kΩ	CAPRES
aopac06	0.05	V_{DD}-0.05	1.08 ... V_{DD}-0.2	<10	97	3360	2.8 / 2.7	70	350	50pF/100kΩ	CAPRES
aopac07	0.05	V_{DD}-0.05	0.12 ... V_{DD}-1.5	<10	99	2680	2.7 / 2.8	85	210	50pF/100kΩ	CAPRES
aopac08	0.05	V_{DD}-0.05	1.5 ... V_{DD}-0.2	<10	110	2300	2.0 / 2.0	70	350	50pF/50kΩ	CAPRES
aopac09	1.2	V_{DD}-0.6	1.2 ... V_{DD}-0.3	<10	100	7600	6.3 / 6.4	65	770	100pF/10kΩ	CORE
aopac10	0.05	V_{DD}-1.85	0.14 ...V_{DD}-1.36	<10	90	7100	6.6 / 7.9	69	520	100pF/10kΩ	CORE
aopac11	0.1	V_{DD}-2.0	0.08 ...V_{DD}-1.1	<10	95	79	0.04 / 0.04	63	7.0	100pF/1000kΩ	CORE
aopac12	1.2	V_{DD}-0.1	1.05 ...V_{DD}-0.1	<10	100	140	0.06 / 0.08	68	10	100pF/1000kΩ	CORE

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Opamps feature a standby mode.

Comparators

Name	V_{ICR} [V]	T_{PD} for 50mV Overdrive [ns] L->H / H->L	T_{PD} for 500mV Overdrive [ns] L->H / H->L	Conditions C_L [pF]; R_L [kΩ]	Input Offset Voltage [mV]	Supply Current [µA]	Required Process Module
acmpc01	1.0 ... V_{DD}-0.2	670 / 220	-	0.5; 1000	<10	3	CORE
acmpc02	0.1 ... V_{DD}-1.1	630 / 320	-	0.5; 1000	<10	3	CORE
acmpc03	1.4... V_{DD}-0.36	93/95	-	0.5; 1000	<10	75	CORE
acmpc04	0.42... V_{DD}-1.52	98/100	-	0.5; 1000	<10	80	CORE
acmpc06	0... V_{DD}	22/ 24	-	0.5; 1000	<10	200	CORE

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Comparators feature a standby mode

Bandgaps

Name	Bandgap Voltage (unloaded) [V]; T = 30°C min / typ / max	Temperature Coefficient [ppm/°C]	Supply Current [µA]	Required Process Module
abgpc01	- / 1.281 / -	+200; T= -40 °C to T= 20°C +50; T= 20 °C to T= 85°C	30	CORE
abgpc02	- / 1.211 / -	+100; T= -40 °C to T= 20°C +100; T= 20 °C to T= 85°C	25	CAPRES
abgpc03	- / 1.227 / -	+80; T= -40 °C to T= 20°C +60; T= 20 °C to T= 85°C	57	CAPRES
abgpc04	- / 1.248 / -	+200; T= -40 °C to T= 20°C +100; T= 20 °C to T= 85°C	3.7	CAPRES

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C , all Bandgaps feature a standby mode

Bias Cells

Name	Bias Voltage V_{BP} for PMOS [V]; @V_{DD}=5V, T=30°C	Temperature Coefficient IVBP [ppm /°C]	Bias Voltage V_{BN} for NMOS [V]; @V_{DD}=5V, T=30°C	Temperature Coefficient IVBN [ppm /°C]	Supply Current [µA]	Required Process Module
abiac01	V_{DD}-1.025	-1000	0.964	-1250	6.5	CORE
abiac02	V_{DD}-1.236	-1100	1.29	-1120	12	CORE
abiac03	V_{DD}-1.474	-1150	1.28	-1200	23	CORE
abiac04	V_{DD}-1.027	-3020	0.966	-3000	6.5	CAPRES
abiac05	V_{DD}-1.243	-750	1.133	-750	12.5	CAPRES
abiac06	V_{DD}-1.478	-800	1.295	-850	32	CAPRES

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Bias Cells feature a standby mode

Analog Library Cells *(continued)*

Analog to Digital Converter							
Name	Principle	Resolution [Bits]	Accuracy [LSB] INL/DNL	Conversion Time [Clock Cycles]	Conversion Rate [kS/s]	Input Voltage Range [V] min/max	Required Process Module
ADC10	successive approximation	10	±1.5 / ±0.5	12	90	V_{SSA}/V_{DDA}	CAPRES
Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ....85 °C							

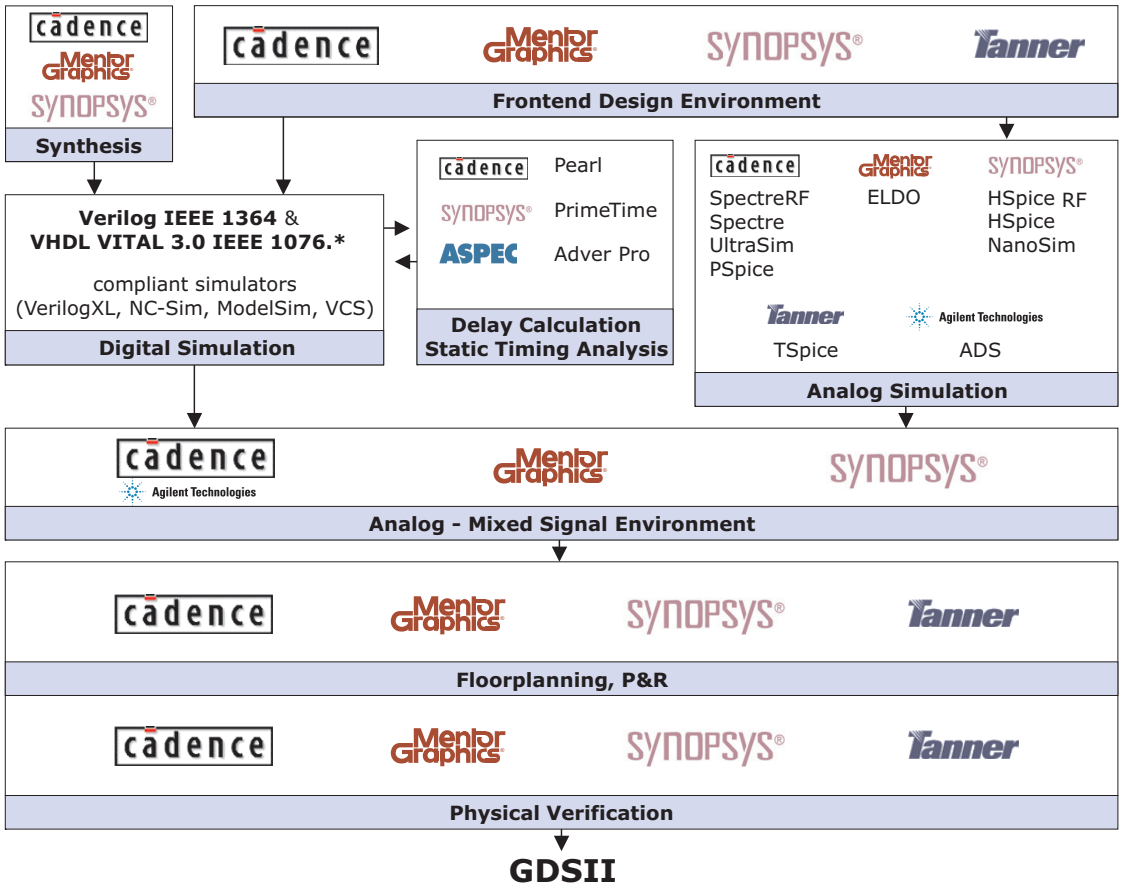
Digital to Analog Converter						
Name	Principle	Resolution [Bits]	Accuracy [LSB] INL/DNL	Conversion Time [µs] @ V_{ref}=5V, C_L=10pF	Input Voltage Range [V] min/max	Required Process Module
DAC10	voltage scaling	10	±0.6 / ±0.2	12	V_{SSA}/V_{DDA}	CAPRES
Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ....85 °C						

RC Oscillators				
Name	Frequency [kHz]	Conditions	Supply Current (specified @ V_{DD}=5V, T=25°C) [µA]	Required Process Module
arcoc01	100	@V_{DD}=5V; T=25°C	77	CAPRES
arcoc02	133 / 200 / 382	@V_{DD}=5V; T=25°C dig. code= 0h / 10h / 1Fh	73	CAPRES
arcoc03	10	@V_{DD}=5V; T=25°C	3.8	CORE
arcoc04	200	@V_{DD}=5V; T=25°C	73	CAPRES
arcoc05	1000	@V_{DD}=5V; T=25°C	100	CAPRES
arcoc06	670 / 1000 / 1860	@V_{DD}=5V; T=25°C dig. code= 0h / 10h / 1Fh	100	CAPRES
Note: All Parameters are valid for V_{DD}: 4.5 V to 5.5V, T: -40 ....85 °C				

Power-On-Reset				
Name	High/Low Treshold Voltage [V]	T_{DEL} [µs] Delay VDD -> H to POR -> L typical	I_{DDL} [µA] DC-Current POR	Required Process Module
aporc01	2.15	3.2	0.01	CORE
aporc02	2.24 / 2.02	5.7	1.8	CORE
aporc03	2.03 / -	5.0	3.2	CORE
Note: All Parameters are valid for V_{DD}: 4.5 V to 5.5V, T: -40 ....85 °C				

Charge Pumps				
Name	Clock Frequency [MHz] min / typical / max	Output Voltage [V]	Supply Current [µA]	Required Process Module
achpc01	0.25 / 1.0 / 2.0	6.24; I_{load} = 0 µA	12; I_{load} = 0 µA	CAPRES
		5.68; I_{load} = 10 µA	40; I_{load} = 10 µA	
		5.33; I_{load} = 20 µA	52; I_{load} = 20 µA	
Note: All Parameters are valid for V_{DD}: 4.5 V to 5.5V, T: -40 ....85 °C				

Supported EDA Tools



Note: Diagram shows overview of all X-FAB supported EDA tools. More details are available for registered customers on X-TIC.

X-FAB's IC Development Kit "TheKit"

The X-FAB IC Development ***Kit*** is a complete solution for easy access to X-FAB technologies. TheKit is the best interface between standard CAE tools and X-FAB's processes and libraries. TheKit is available in two versions, the Master Kit and the Master Kit Plus. Both versions contain documentation, a set of software programs and utilities, digital and I/O libraries which contain full front-end and back-end information for the development of digital, analog and mixed signal circuits. Tutorials and application notes are included as well.

The Master Kit Plus additionally provides a set of general purpose analog functions mentioned in section "Analog Library Cells" and is subject to a particular license.

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