YAMAR Electronics Ltd.
Preliminary Description

DCB1M - Transceiver for Powerline Communication

The information in this data sheet is preliminary and may be changed without notice.

1. General

The DCB1M is an innovative technology for multiplex communication over noisy wires such as vehicle's DC Powerline, at speeds up to 1.3Mbps. The DCB1M is based on DC-BUS™ technology for network communication between modules sharing a common DC or AC powerline. It avoids complex cabling, saves weight, and simplifies installation. The device supports UART and SPI communication protocols, enabling the user to use his preferred application protocol. The technology is implemented in small size logic that can be ported into any FPGA or ASIC.

Main Features

- *Communication over DC or AC power line*
- *Bit rates of up to 1.3Mbps*
- *Built in Modem, Error Correction and Synchronization*
- *Multiplex CSMA/CA mechanism*
- *Selectable communication robustness*
- supports UART, SPI *protocols*
- *Sleep mode for low power consumption*

Main Benefits

- *Eliminates complex harness*
- *Reduces weight and installation time*
- *Robust to power line noises*
- *Allows flexible network designs*
- *Suitable for voice and video streaming*
- *Low cost CMOS Implementation*

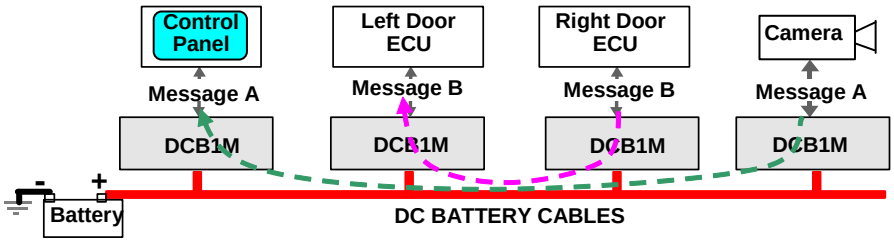

Figure 1 - An example of DCB1M network

DC-BUS technology can be beneficial to many applications ranging from Aerospace, Automotive, Industrial and even Toys.

www.yamar.com Tel: +972-3-5445294 Fax: +972-3-5445279

2. Overview

The DCB1M network

The DCB1M operates as part of a network consisting of multiple DCB1M devices. Each device can transmit messages to other devices over the power lines at four selectable communication rates for enhanced robustness, ranging from 1.3Mbps down to 450Kbps for very noisy channel. The data on the powerline is phase modulated by a sine wave at a predefined carrier frequency.

Each DCB1M device can communicate with its host using one of the supported protocols (UART and SPI). There is no restriction on the network data protocol. As an example, one host using SPI protocol can communicate with another host interfacing with UART protocol where the DCB1M devices operate as gateways between the hosts.

DCB1M Channel parameters

Channel frequency:	5MHz
Data transfer rate:	1.3Mbps, 1Mbps, 490 Kbps, 223 Kbps.
Cable length:	Depends on the power line loads AC impedance.

DCB1M Architecture

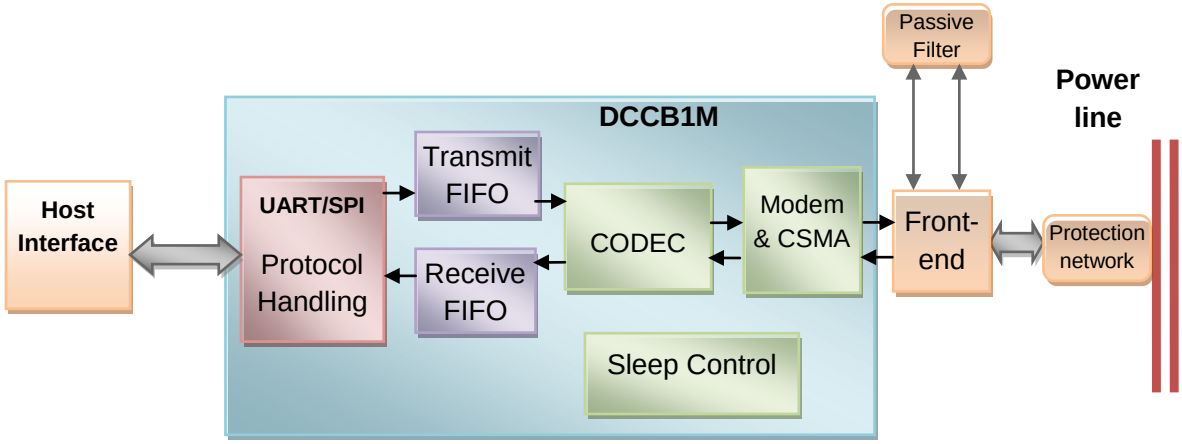

Figure 2.1 - DCB1M Block Diagram

The DCB1M is divided into the following main building blocks;

- Protocol handling block, interprets the host protocol.
- Transmit and Receive internal FIFOs, each has 128 bytes, providing a buffer between the host and the DC-BUS powerline.
- CODEC block, encodes/decodes the data according to the channel protection selected.

- Modem block, phase modulates and demodulates the data to and from the DC-BUS powerline.

- CSMA/CA mechanism allow Carrier sense and arbitration capabilities to the device
- Sleep mechanism, ensures low power operation during sleep mode. During Sleep mode, the device wakes up for short period of time to detect possible wakeup messages from other devices on the powerline.

DCB1M Frame Structure

The DCB1M receives data from its host in variety of protocols. The data is constructed internally into frames. Each frame starts with a Preamble, followed by at least, one data packet and terminated by a “frame end” indication as described in Figure 2.2. When enabled, the DCB1M message will include in the Preamble, the Carrier Sense and Arbitration (See Section 5 - 6).

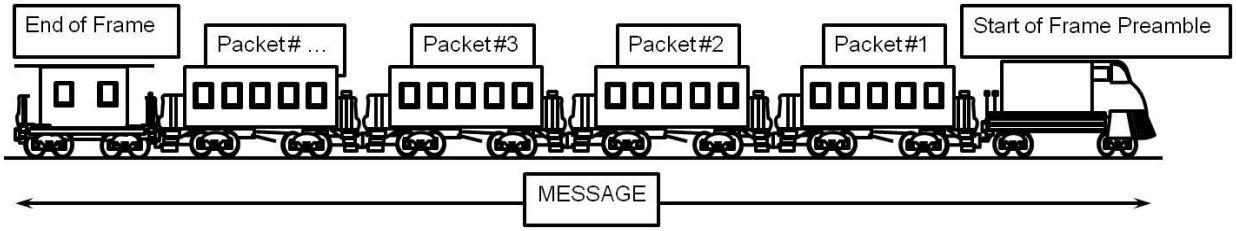

Figure 2.2 - Message construction

Each data packet is protected by an Error Correction Code [ECC] with a strength chosen by the user, using a proper command (see protocols section). Choosing a stronger ECC will result in lower baud rate. Table 1 shows the available codes and their corresponding baud rates over the DC-BUS powerline.

Codec Select	Max Baud RATE (Mbps)
Code 0	1.34
Code 1	1
Code 2	0.49
Code 3	**0.223 (Default)**

Table 1 Codec Selection

3. DCB1M Registers

DCB1M Internal Registers

The DCB1M contains internal registers for configuration and status check. Each of these register is accessible by the host for read and write operations. The way to access these register is different for each protocol and describe at protocols section. This section elaborates on the different registers and their default values after reset.

Control Register 0:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	1	1
Reserved	Reserved	Reserved	**nLoopback**	Reserved	Reserved	Reserved	Reserved

Bits [3:0] - Reserved

Bit [4] - nLoopBack - "1" disables loopback of HDI to HDO

Bits [7:5] - Reserved

Control Register 1:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	0
Reserved							

Bits [7:0] - Reserved

Control Register 2:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	0	0	0	1	1
Reserved	Reserved	E.Interf Det	E.Arbitration	E.Carrier Sense	Reserved	Codec_Sel[1]	Codec_Sel[0]

Bits [1:0] - Codec Select - Selecting the coding strength of the transmitted message (UART Interface only) see Table 2

Bit [2] - Reserved

Bit [3] - Enable Carrier Sense mode

Bit [4] - Enable Arbitration mode

Bits [5] - Enable Interference Detection

Bits [6] - Reserved

Bits [7] - Reserved

Table 2 Codec Select Configuration (UART interface only)

Control_register2 (1:0)	Codec Select
00	Code 0
01	Code 1
10	Code 2
11	Code 3 (Default)

Control Register 3:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	1	1	1	1
SPI Interrupt Mask [7:0]							

Bits [7:0] - SPI Interrupt Mask [7:0]

Control Register 4:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	0
Arbitration ID [7:0]							

Bits [7:0] - Arbitration ID [7:0]

Control Register 5:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	0
Arbitration ID [10:8]							

Bits [2:0] - Arbitration ID [10:8]
Bits [7:3] - Reserved

4. DCB1M Protocols

The DCB1M can interface with UART and SPI protocols. The selection between the protocols is made after reset and is valid until the next reset.

There are two pins (if_mode [1:0]) that configure the protocols selection,

If_mode[1:0]	**Selected Protocol**
00	UART
01	Reserved
10	SPI
11	Reserved

Table 3 Protocols Selection

UART Protocol

The UART communication protocol uses 4 pins:

HDI	Data Input from the host	
HDC	Data/Command select between transmitting data ('1') or writing a command ('0').	Shared function with CS
HDO	Data output to the host	
RTR	Ready to Receive signal indicating that the device is ready to receive new data from the host.	Used to control the data flow between the host and the DCB1M.Shared function with INT (‘Go_NoGo’ signal)

Table 4 UART interface pins

Read and Write operation to Internal Registers

The device can accept read and write commands to its internal registers. The read command, contains the internal register address (**0** to **3**) in the higher nibble and the read command **0xD** at the lower nibble. The write command contains the internal register address (**0** to **3**) in the higher nibble and the write command **0x5** at the lower nibble. For example, in order to write to an internal register at address 3 the host needs to lower pin DC, send **0x35** and then send another byte with the requested value. To read the same register the host need to lower the DC pin and to send **0x3D**, the register content will be sent back to the host by the DO pin.

Bit Rate Configuration

For basic UART communication only two pins are required the DI and DO, this will allow to transmit at 115K2bps (The device default UART bit rate). However in order to change the bit rate (up to 921.2Kbps) and to gain access to the device internal registers, the DC pin is also required. By lowering the DC pin, the device enters the command mode and will not transmit the incoming data to the DC-BUS, and will not forward any received bytes to the Host. When a command is sent to the device it will automatically detect the host's bit rate and will switch to that bit rate. For example, by lowering pin DC and sending 0x55 at 230.4Kbps, the device will switch to the

230.4Kbps bit rate and after rising back the DC pin, the host will be able to communicate with the device at 230.4Kbps.

Codec Select Configuration

When interfacing a UART host, the user can configure the max baud rate of the DCB either by the Codec_Select [1:0] pins or by configuring 'Control Register 2' . Both methods have the same priority and the last configuration change will determine the DCB baud rate.

UART Examples

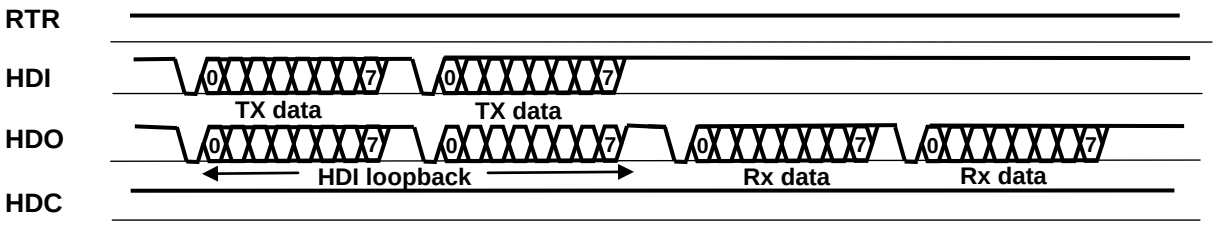

Figure 3 - UART Typical communication Sequence

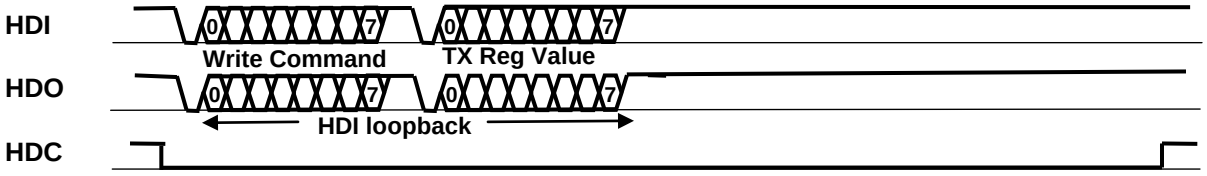

Figure 3.1 - UART Write Command Sequence

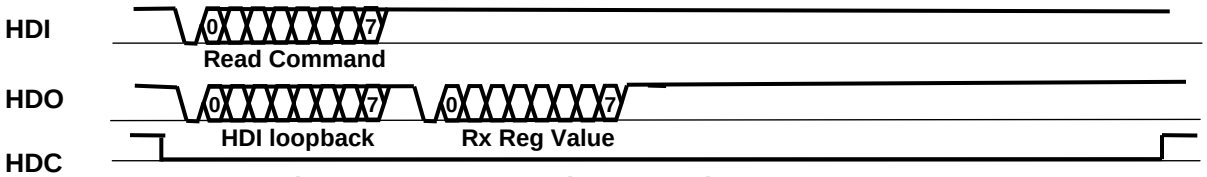

Figure 3.2 - UART Read Command Sequence

SPI Protocol

The SPI communication protocol uses 5 pins.

HDI	Data Input from the host	
HCS	Chip select input.	Shared function with DC
HDO	Data output to the host	
SCK	Serial clock input.	
HINT	Interrupt output (Active High)	Shared function with RTR

Table 5 SPI protocol pins

The device is acting as an SPI slave with CPOL = 1 and CPHA = 1. The data is sampled at the rising edge of the CLK and outputted at the falling edge of the CLK, the default state of the CLK pin is HIGH. The expected data is MSB first. Max CLK rate is 10 MHz.

When the host lowers the DC pin, the DCB1M expect a command to be received. Based on the received command, the host can send data to the DCB1M or to start receiving new data from the DCB1M. For example, to send a frame to the DCB1M the host lowers the CS pin and sends a one byte TX DATA command to the device, following the command the host starts to send the data bytes. To close the transferred frame, the Host needs to raise the DC pin and lower it again and send the frame end command.

Flow control

In addition to the required 3 pins (HDI, HDO and SCK), the HINT (interrupt) pin is used to manage the SPI communication. There is one interrupt register and ones mask register allowing to enable or to mask the interrupts *(See Control Register 3).* When an interrupt is issued by the DCB1M then the host has to read the interrupt status registers to determine the current status of the device.

Status Int. registers

7	6	5	4	3	2	1	0
Rsrv	Rsrv	Rsrv	Rx fifo empty	Rx fifo almost full	Rx frame end	Tx fifo almost empty	Tx fifo almost full

Tx fifo almost full - The TX FIFO is almost full. (116 out of 128 bytes are in the TX FIFO)

Tx fifo almost empty - The TX FIFO is almost empty (12 bytes left in TX FIFO).

Rx frame end - A frame end indication was received from the DC-BUS.

Rx fifo almost full - The Rx FIFO is almost full. (98 out of 128 bytes are in the RX FIFO)

Rx fifo empty - The Rx FIFO is empty. Any further read operation from it will output an invalid byte.

Rsrv - Reserved bit for future use.

Rsrv - Reserved bit for future use.

Rsrv - Reserved bit for future use.

SPI Commands

There are six commands that can be sent after lowering the CS pin:

TX DATA - Start to transmit the following bytes to the DC-BUS. The TX DATA command contains also the transmit baud rate option.

0x04 - Full Speed (Codec Select '11')

0x14 - 3/4 Speed (Codec Select '10')

0x24 - Half Speed (Codec Select '01')

0x34 - 1/3 Speed (Codec Select '00')

FRAME END (0x0F) - Send a frame end message to the DC-BUS.

RX DATA (**0x0B)** - Start to read the received data to the host.

WRITE REG. (0xY5) - Write to control register Y.

READ REG. (0xYD) - Read from control register Y.

READ INT. (0x01) - Read the interrupt register.

SPI Examples

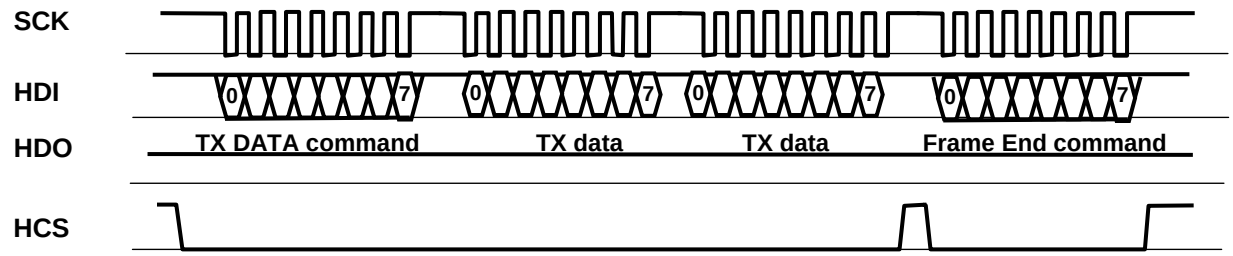

Figure 4 - SPI Transmit data sequence

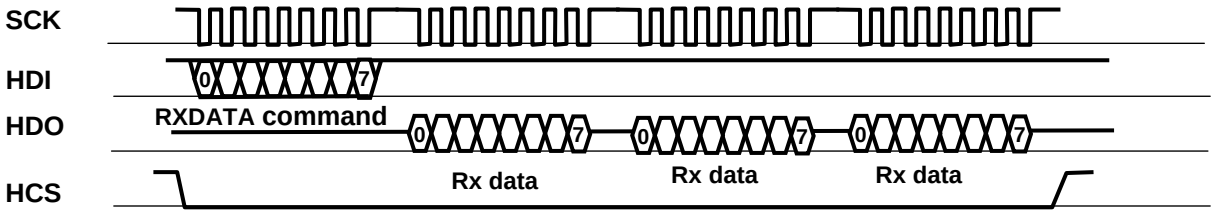

Figure 4.1 - SPI Receive data sequence

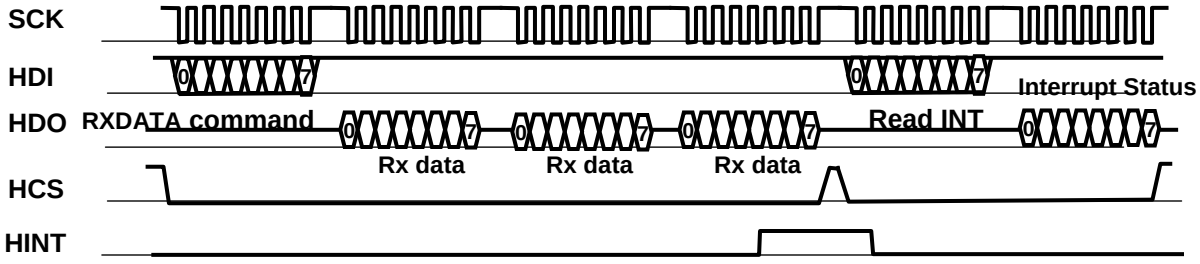

Figure 4.2 - SPI Receive data sequence with RX FIFO Empty interrupt event

5. Carrier Sense

The carrier sense [CS] prevents one DCB1M from interfering another DCB1M's transmit. In this mode the DCB1M will check if the DC-BUS is idle or if there is currently an ongoing transmit. If the CS is enabled, the frame will start with a carrier sense period prior to sending the sync pattern.

To enable the CS mode, set '*Control Register 2'* bit [3] to '1'**.**

6. Arbitration

The arbitration mode is used to prioritizing messages. If two DCB1M devices want to gain access to the DC-BUS at the same time, then the arbitration mechanism can be used to allow access to the message with the higher priority. When the arbitration mode is enabled, the message will begin with a carrier sense period followed by the arbitration sequence. If the arbitration has passed successfully then the DCB1M will continue with the transmission by sending the sync pattern, else, the DCB1M will abort the transmission and will wait for the received message to complete before trying to retransmit.

The arbitration pattern is configured by Arbitration ID [10:0] (See *Control Register 4 and 5).*
The Device with the highest priority (ID = 0) will win in the Arbitration process and will gain access to the DC-BUS.
To enable the Arbitration mode set '*Control Register 2'* bit [4] to '1'**.**

7. Sleep mode

The device has three power consumption modes: Normal Mode (normal transmitting and receiving), Sleep Mode (power saving mode), and Standby Mode (after waking up, while pin nSleep is low). A transition between these modes depends on the sleep control pin, or remotely, when a Wakeup message is detected on the bus.

During the Sleep mode, the device enters into power saving operation where only its internal low frequency clock operates. The device wakeup every 32mS for duration of 1.5mS to detect a dedicated wakeup message on the DC-BUS. If such message is detected, the device switches to Standby mode, raising its INH pin to indicate its host that a wakeup message has been detected. It is the responsibility of the host to raise the nSleep pin in order to switch to Normal operation mode.

Entering Sleep mode

The host can place the device into Sleep mode by a lowering to "0" (falling edge) pin nSleep .When the device enters to Sleep mode it lowers pin INH.

There are two ways to wakeup the device from Sleep mode.

Wakeup from pin nSleep

In this case, the host wake the DCB1M by rising the nSleep pin. The raise the INH pin and start automatically to transmit the wakeup message.

The device transmits the wakeup message to wakeup all other devices on the DC-BUS. While transmitting this wakeup message to the DC-BUS, the device lowers pin HDO. After the transmission is complete the device raises pin HDO (can be used to signal/interrupt the host). After the transmission is completed and pin nSleep is high, the device enters Normal mode. See Figure 5 for signals description.

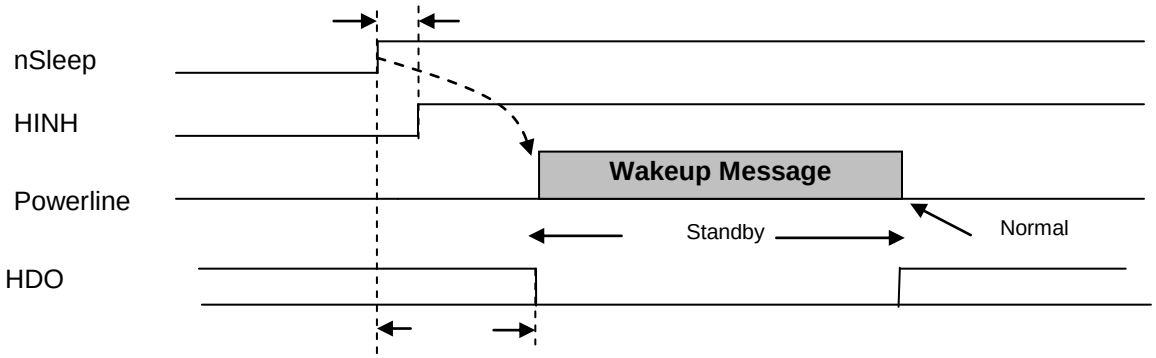

Figure 5 - Wakeup from nSleep pin

Wakeup from bus message

During Sleep mode, the device wakes up every 32mS periodically to check for activity on the bus. If a wakeup message is detected, the device enters Standby mode and raises pin INH. The device then signals the host by lowering pin HDO for a minimal duration of 8 bits, and a maximal duration of about 150mSec. The host has to raise nSleep pin (otherwise the device will remain in Standby mode). After completing the reception, the device enters Normal mode. See Figure 5.1 for signals description.

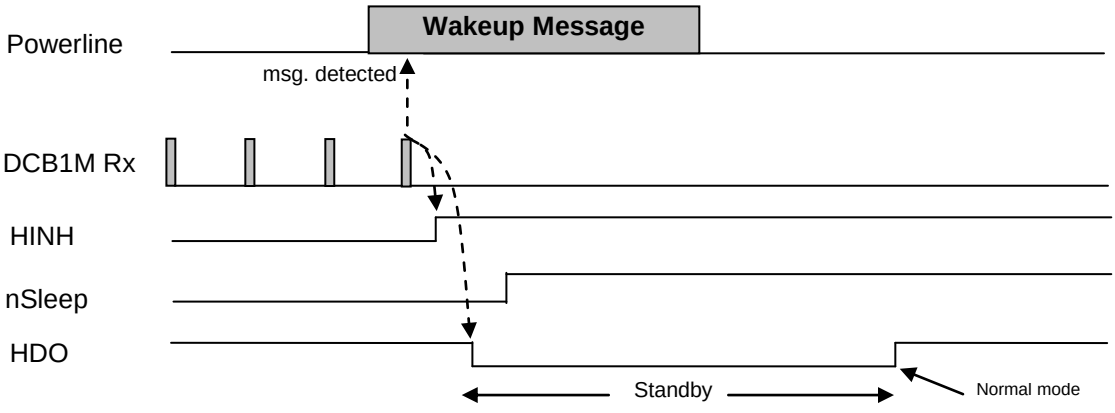

Figure 5.1 - Wakeup from bus message

Revision History

Revision	Issue Date	Comments
0.1	9.5.12	Preliminary beta addition
0.15	20.4.13	Updating Table 1
0.2	5.10.14	Update Table 1
0.3	17.11.2014	Update DCB1M Internal Registers mapping
0.4	9.2.2016	Update sections 5 and 6.