YAMAR Electronics Ltd.
Product Overview

DCB1M - Transceiver for Powerline Communication

This information is preliminary and may be changed without notice. Jan 2013

1. General

The DCB1M is an innovative technology for multiplex communication over noisy wires such as vehicle's DC Powerline, at speeds up to 1.3Mbps. The DCB1M is based on DC-BUS™ technology for network communication between modules sharing a common DC or AC powerline. It avoids complex cabling, saves weight, simplify installation and increase reliability. The device supports UART and SPI communication protocols, enabling the user to use his preferred application protocol. The Multi-rate Forward Error Correction mechanism allows enhanced data robustness according to the actual communication conditions, ranging from 1.3Mbps down to 450Kbps for very noisy channel. The technology is implemented in small size logic that can be ported into any FPGA or ASIC.

Features

- *Communication over DC or AC power line*
- *Bit rates of up to 1.3Mbps*
- *Built in Modem, Error Correction and Synchronization*
- *Multiplex CSMA/CA mechanism*
- *Selectable coding for communication robustness*
- Supports UART, SPI *protocols*
- *Sleep mode for low power consumption*

Benefits

- *Eliminates complex harness*
- *Reduces weight and installation time*
- *Robust to power line noises*
- *Allows flexible network designs*
- *Suitable for voice and video streaming*
- *Low cost CMOS Implementation*

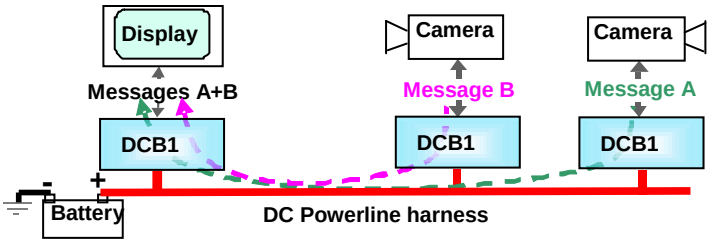

Figure 1 – Cameras network over powerline

DC-BUS technology can be beneficial to many applications ranging from Aerospace, Automotive, Industrial and many more.

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The DCB1M network

The DCB1M operates as part of a network consisting of multiple DCB1M devices. Each device can transmit messages to other devices over the power lines at four selectable communication rates for enhanced robustness, ranging from 1.3Mbps down to 450Kbps for very noisy channel. The data on the powerline is phase modulated by a sine wave at a predefined carrier frequency.

Each DCB1M device can communicate with its host using one of the supported protocols (UART and SPI). There is no restriction on the network data protocol. As an example, one host using SPI protocol can communicate with another host interfacing with UART protocol where the DCB1M devices operate as gateways between the hosts.

DCB1M Channel parameters

Channel frequency: 5MHz

Data transfer rate: 1.3Mbps, 1Mbps, 490 Kbps, 223 Kbps.

Cable length: more than 20m (mainly depends on the AC impedance @5MHz of loads connected to the powerline).

DCB1M Architecture

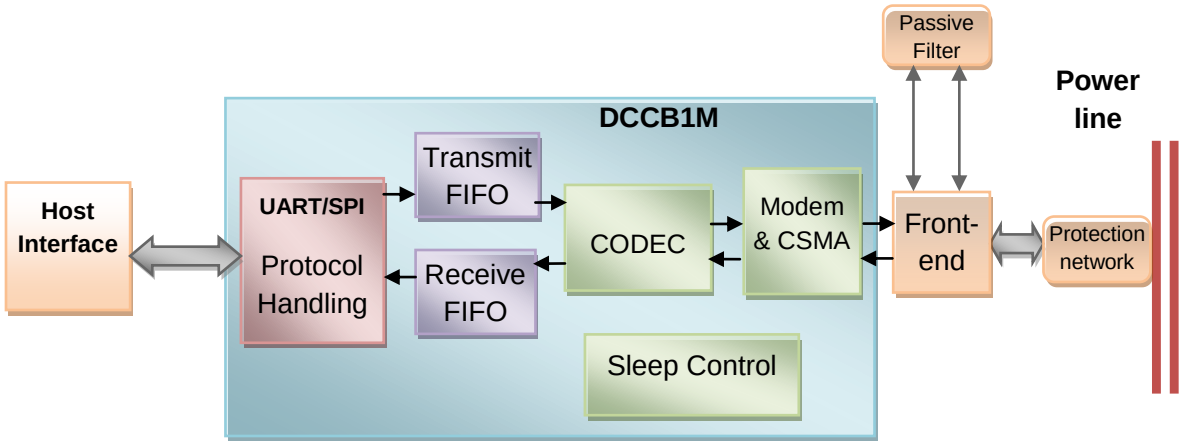

Figure 2 - DCB1M Block Diagram

The DCB1M is divided into the following main building blocks;

- Protocol handling block, interprets the host protocol.
- Transmit and Receive internal FIFOs, each has 128 bytes, providing a buffer between the host and the DC-BUS powerline.
- CODEC block, encodes/decodes the data according to the channel protection selected.
- Modem block, phase modulates and demodulates the data to and from the DC-BUS powerline.

- CSMA/CA mechanism allow Carrier sense and arbitration capabilities to the device
- Sleep mechanism, ensures low power operation during sleep mode. During Sleep mode, the device wakes up for short period of time to detect possible wakeup messages from other devices on the powerline.

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