ZFx86™

System-on-a-Chip

Easy Embedded PC System

Hardware Quick Start Guide

July 9, 2009

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1. Overview

The ZFx86 Easy Embedded PC reference design is intended to provide a complete development environment that can be used to demonstrate how a target system based on the ZFx86 chip will perform. It is extremely integrated. The standard PC type interfaces are built into the chip (serial and parallel ports, etc.). Additional onboard features include video, LAN and an IDE based solid state disk drive.

There is an ISA and PCI connector for hosting additional adapters.

The designer can deploy additional ISA or PCI based "chips" within the confines of the EEPC by acquiring a plug in eval board from the chip vendor, and installing it into the appropriate connector. This way you can quickly (and easily) mimic the behavior of your target design. At this early point in the project, you can supply this 'virtual target' hardware to your software development team for applications integration (various OS's are provided).

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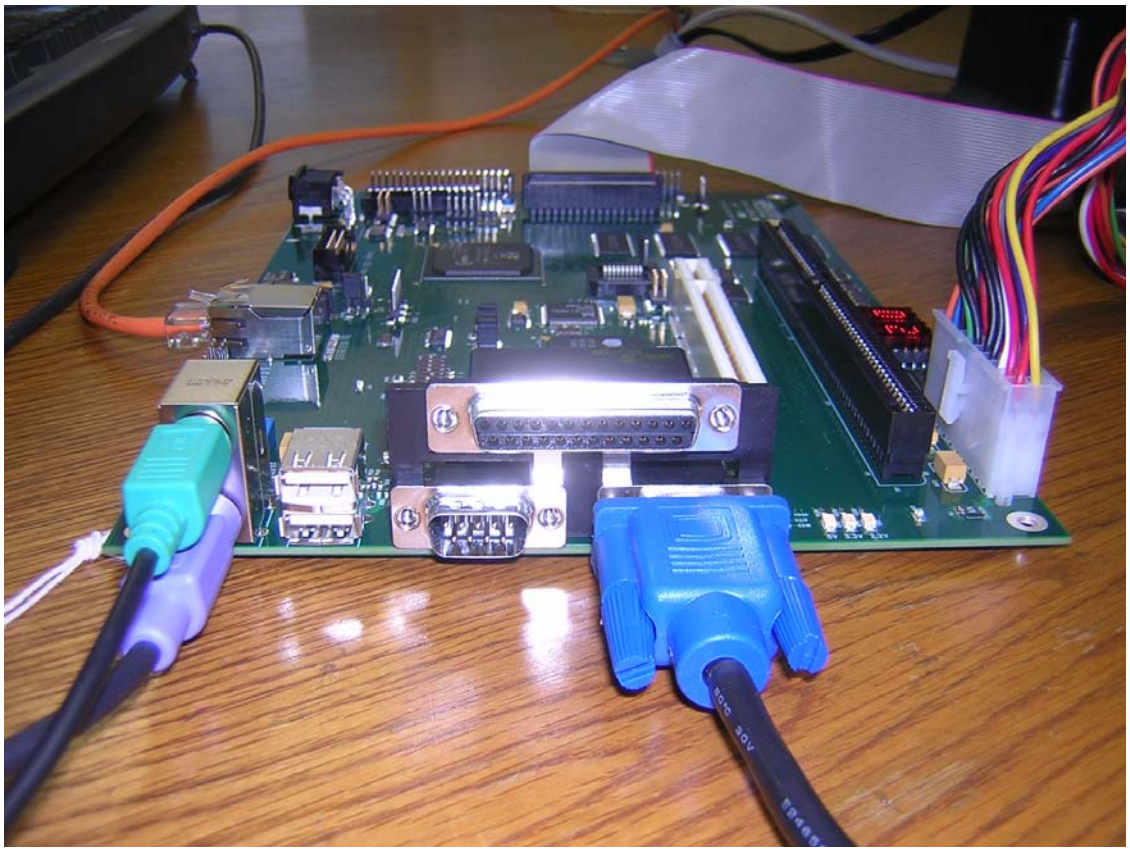


Figure 1-1 ZFx86 Easy Embedded PC System

2. Hardware Setup

2.1. EEPC Board

General Specifications:

- CPU ZFx86 – 486 operating at a max. of 100MHZ with integrated:
  FPU
  SDRAM controller
  PCI & ISA
  Dual IDE controller
  Floppy controller
  Dual RS232
  Dual USB (low speed operation only at this time)
  Parallel port
  PS2 keyboard and mouse controllers
  Realtime clock/calendar
  Additionally, an internal monitor ROM facilitates a number of utility programs used for board bring up and field troubleshooting.

- BIOS Phoenix version 6, release 4 loaded. Video BIOS is also installed.

- DRAM 128Mbytes of 32 bit wide SDRAM is comprised of four 32MByte devices.

- Video Dual VGA and LCD operation is provided by a Silicon Motion SM712 video controller with integrated memory (4MB)

- LAN 10/100 integrated MAC/PHY from Realtek RTL8139DL

- HD 128MB is onboard as a solid state disk (IDE interface) from SST. DR DOS 7.03 is already installed.

- Power - an ATX power supply (not included) provides 5V and 3.3V to the board. The ZFx86's core voltage (2.20V) is derived from an LDO connected to the 5V supply. +/- 12V and -5V are not used.

- Dimensions – 7" x 10"

2. Default Jumper Settings

Several switches and jumpers allow configuration of many of the features the ZFx86 chip provides. We have pre-configured the system to enable as many features as possible, and to configure them in the typical manner.

2.1. Clocking

The clocking scheme utilizes the Cypress CY2292F triple PLL clock generator. It has been programmed with four system clock frequencies (SYSCLK). The ZFx86 EEPC is pre-configured with the following setting selections (CY2292F rev 7):

SYSTEM SPEED SETTINGS:

							FRONT SIDE		BACKSIDE			
SYSCLK	JP1-	JP1-	CPU	CPUCLK	SW2-	PCI	PCI	SW2-	PCI	JP1-	JP1-	
SPEED	5&6	7&8	SPEED	MULT	3,2	SPEED	DIVIDE	4	SLCT	1&2	3&4	
25MHz	OUT	OUT	25MHz	x1	on:on	25MHz	/1	on	25MHz	OUT	IN	
33MHz	IN	OUT	33MHz	x1	on:on	33MHz	/1	on	33MHz	OUT	IN	
33MHz	IN	OUT	100MHz	x3	off:off	33MHz	/1	on	33MHz	OUT	IN	
50MHz	IN	IN	50MHz	x1	on:on	25MHz	/2	off	25MHz	IN	OUT	
50MHz	IN	IN	100MHz	x2	on:off	25MHz	/2	off	25MHz	IN	OUT	default
66MHz	OUT	IN	66MHz	x1	on:on	33MHz	/2	off	33MHz	IN	OUT	

2.2 JUMPERS

2.2.1 **JP1** System clock select described in above table

2.2.2 **JP2** Watch Dog loopback

1&2 disconnected (default)

2&3 connected

2.2.3 **JP4** Realtime clock/CMOS memory battery

1&2 normal (default)

2&3 clear CMOS

2.2.4 **JP11** AMD flash memory select

1&2 enable

2&3 disable (default)

Jumpers (cont'd)

2.2.4 **JP12** Memory socket SKTU22 (PLCC) select

1&2 GPIO0 select

3&4 ZFx86 memCS1 select

5&6 ZFx86 memCS0 (boot) select (default)

2.2.5 **JP22** Secondary solid state HD write protect (SST NAND drive)

1&2 not write protected (default)

2&3 write protected

2.2.6 **JP23** Secondary solid state drive select (SST NAND drive)

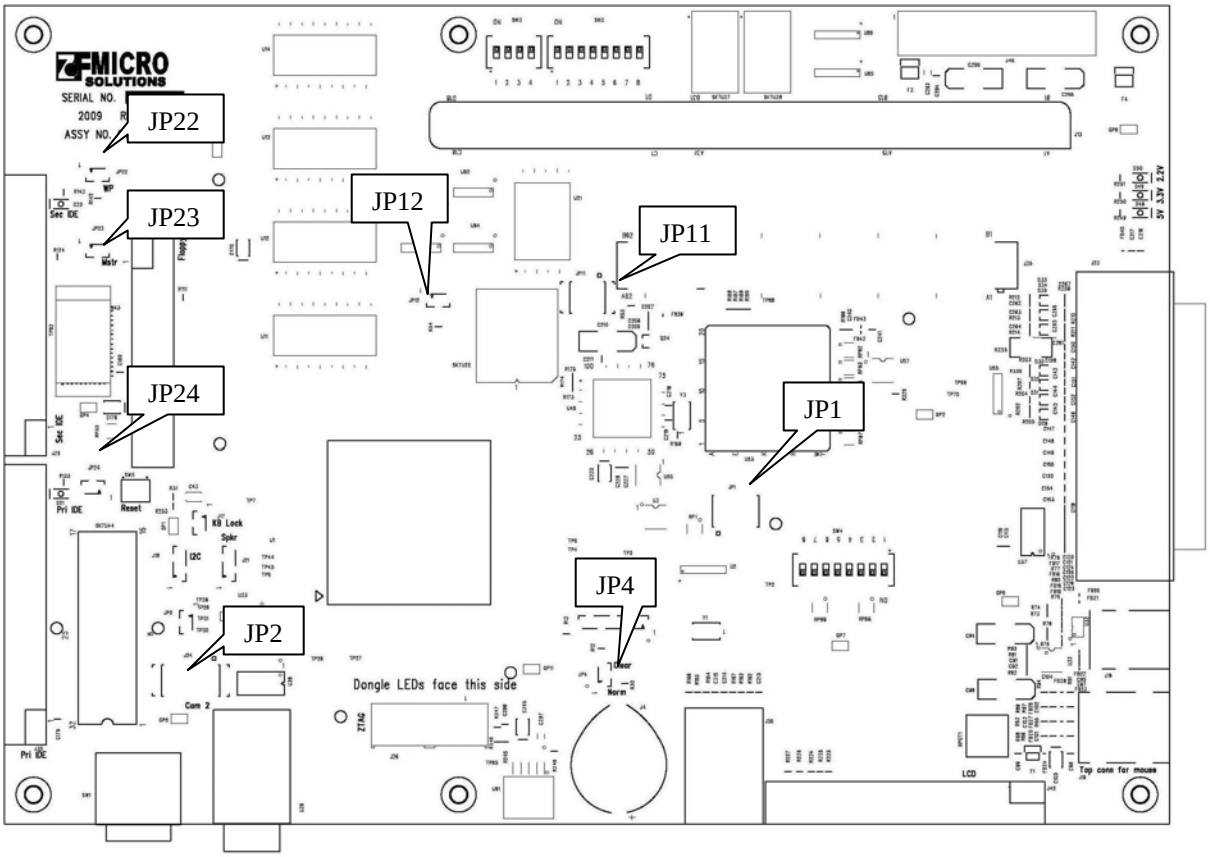
1&2 slave

2&3 master (default)

2.2.7 **JP24** Primary solid state drive mode (Apacer ATA drive)

1&2 non DMA mode (default)

2&3 DMA mode



Easy Embedded PC jumper locations

2.3 Connectors

2.3.1 **J1** JTAG 1x7

2.3.2 **J4** Battery holder coincell (2032)

2.3.3 **J13** ISA card edge connector

2.3.4 **J16** USB dual type A

2.3.5 **J17** Keyboard lock 1x3

2.3.6 **J18** i2c 1x4

2.3.7 **J19** keyboard/mouse combo dual 6 pin mini DIN

2.3.8 **J21** speaker 1x4

2.3.9 **J23** VGA/RS232 (COM1)/parallel port combo 15/9/25 DSUB combo

2.3.10 **J24** RS232 (COM2) 2x5

2.3.11 **J25** Floppy 2x17 **NOTE PIN 1 orientation, a reversed cable will destroy the contents of the floppy media.**

2.3.12 **J26** ZTAG 2x7

2.3.13 **J29** IDE, secondary 2x20

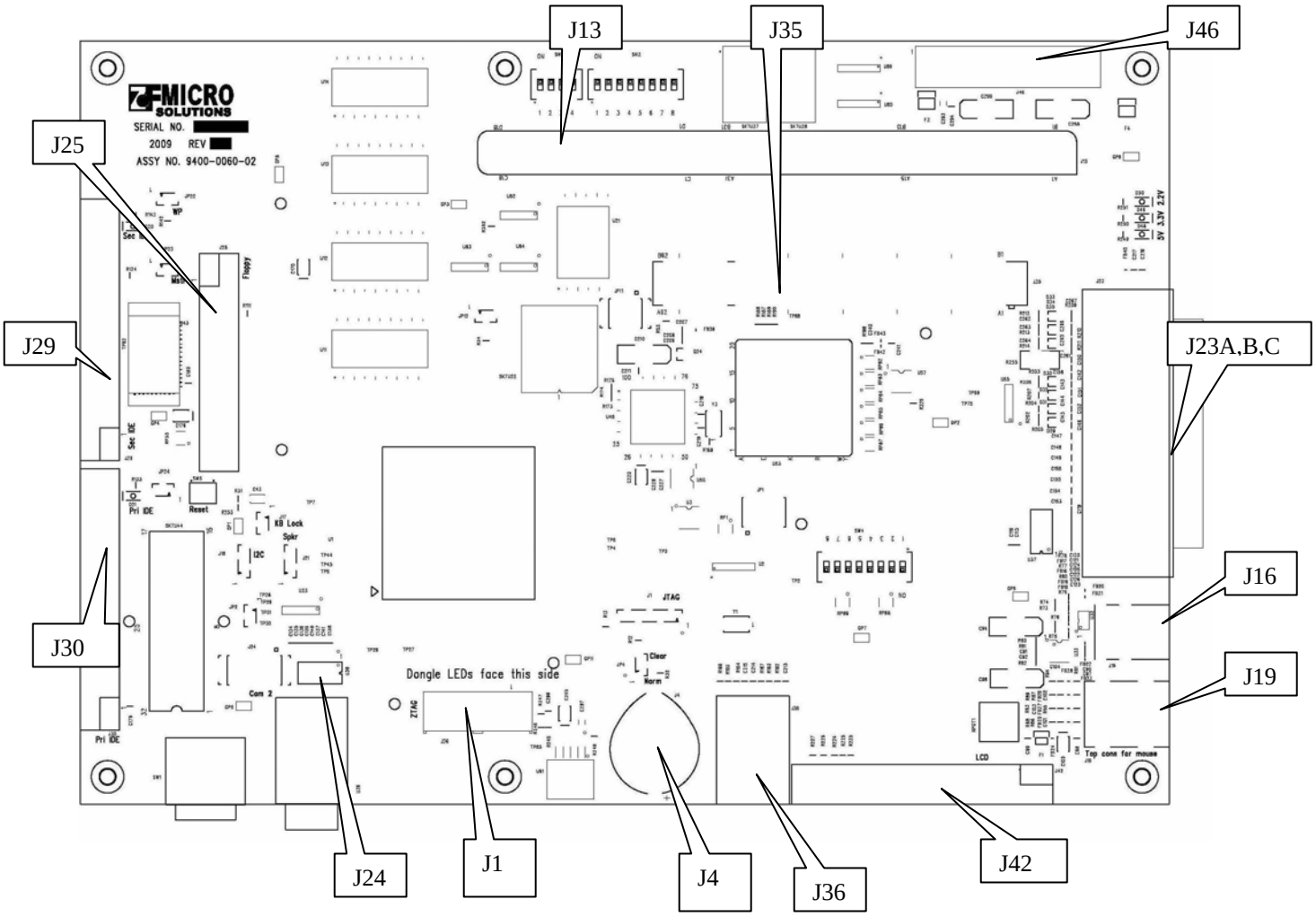
2.3.14 **J30** IDE, primary 2x20

2.3.15 **J35** PCI card edge connector

2.3.16 **J36** LAN RJ45 (with integrated transformer and activity LEDs)

2.3.17 **J42** LCD, TTL 2x20

2.3.18 **J46** Power, ATX 2x10



Easy Embedded PC connector locations

2.4 Switches

2.4.1 **SW1** power, rocker

2.4.2 **SW2** ZFx86 bootstrap, system config, 8 position DIP

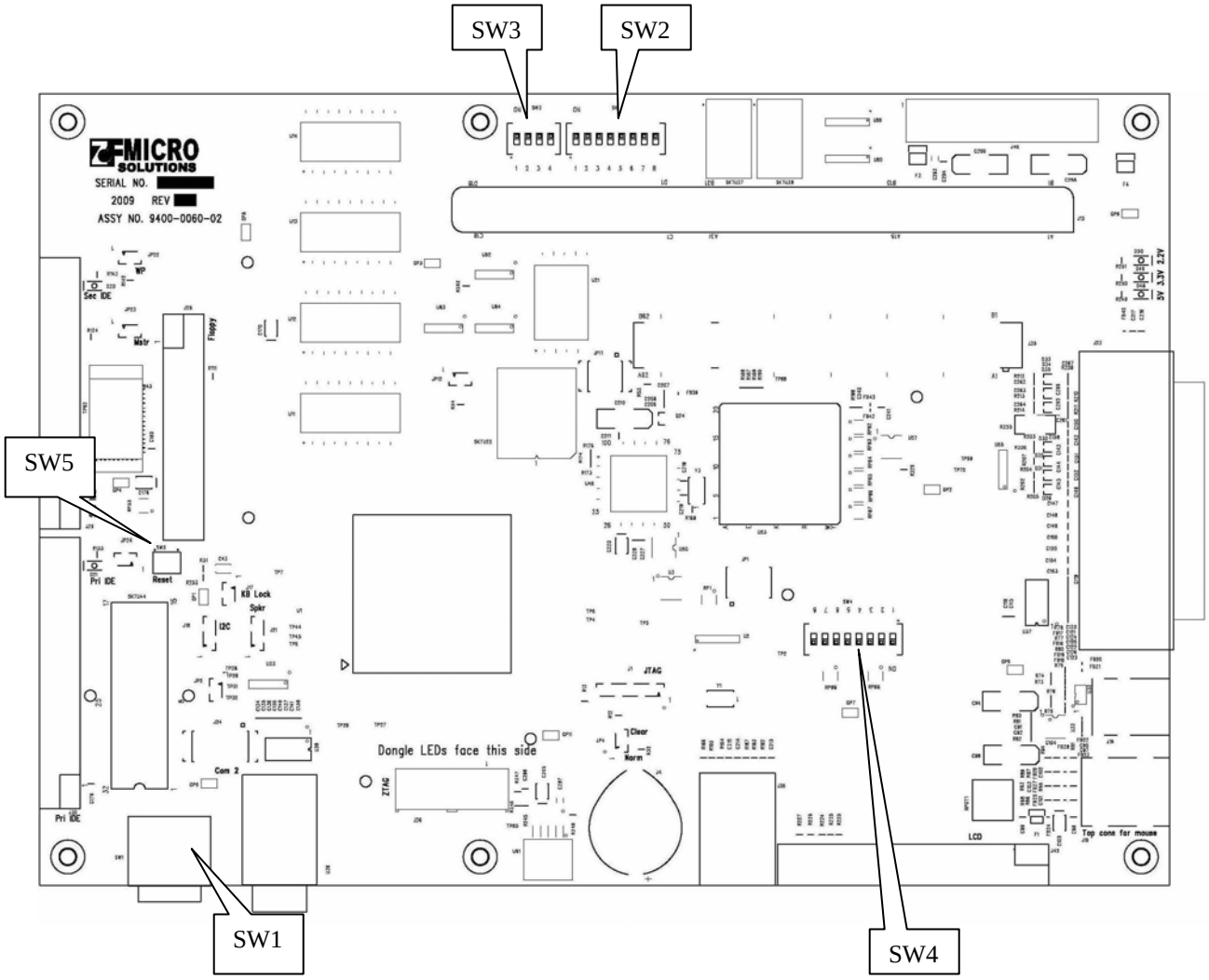
See system speed settings table in section **2.1** (Clocking) for positions 2, 3 & 4. All other positions should be off (default)

2.4.3 **SW3** ZFx86 bootstrap, user defined, 4 position DIP

2.4.4 **SW4** Video controller config.

Position 4 off, all others on.

2.4.5 **SW5** Reset, push button



Easy Embedded PC switch locations