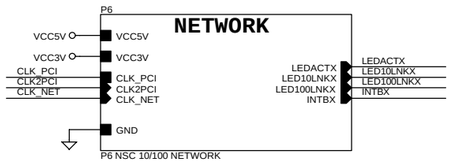

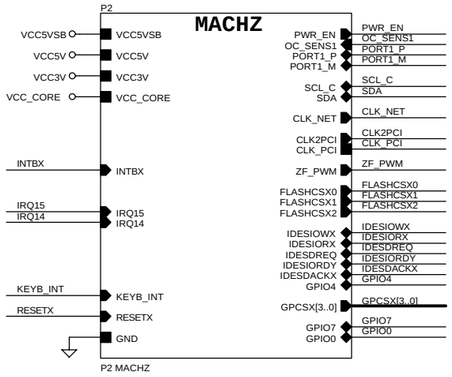

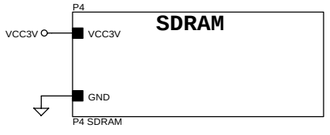

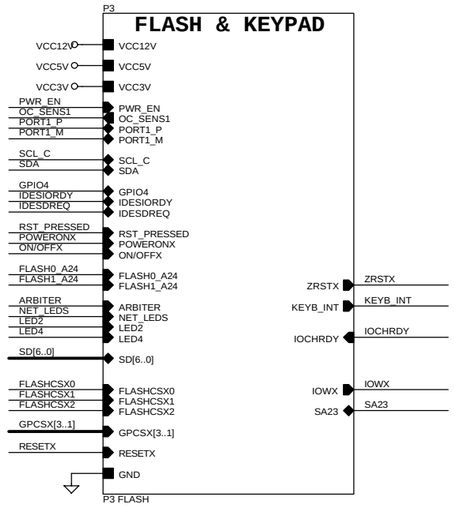

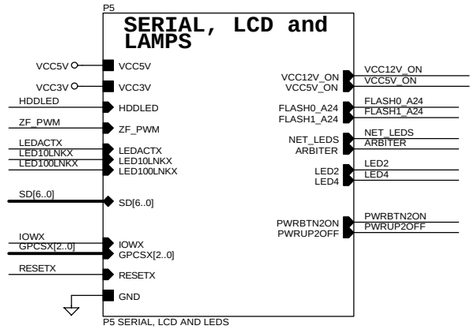

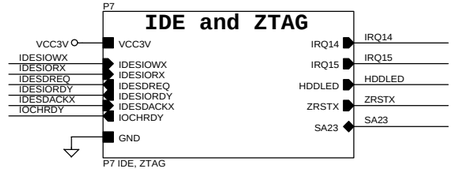

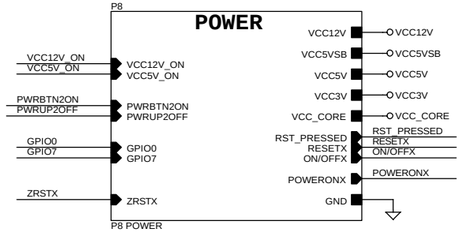

BD1

ZF: 8800-0050-04
ADG: 6721010400

PCBOARD

90210104-01

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(650) 965-3800

APPROVALS	Date
Drawn K. Kevvai	
Checked A.Kuusik	
Designed by	

Title: NETWORK DISK DRIVE: Main

Rel: 01

Size: C | Document nr | ZF nr: 9400-0050-00-X4 | Rev: 4

Date: Monday, November 06, 2000 | Sheet 1 of 8

PSEL1	PSEL0	PCLK1	PCLK2,3	PCLK4
0	0	25.00	50.00	18.75
0	M	TEST	TEST	TEST
0	1	TEST	TEST	TEST
M	0	40.00	80.00	20.00
M	M	33.33	66.66	25.00
M	1	20.00	40.00	25.00
1	0	20.00	33.33	25.00
1	M	20.00	66.66	25.00
1	1	TEST	TEST	TEST

KEYBOARD

CMOS BATTERY

1-2 NORM
2-3 CLR
CMOS

1-2 WD OSC EXT
2-3 WD OSC INT

POWER

PWM OUT

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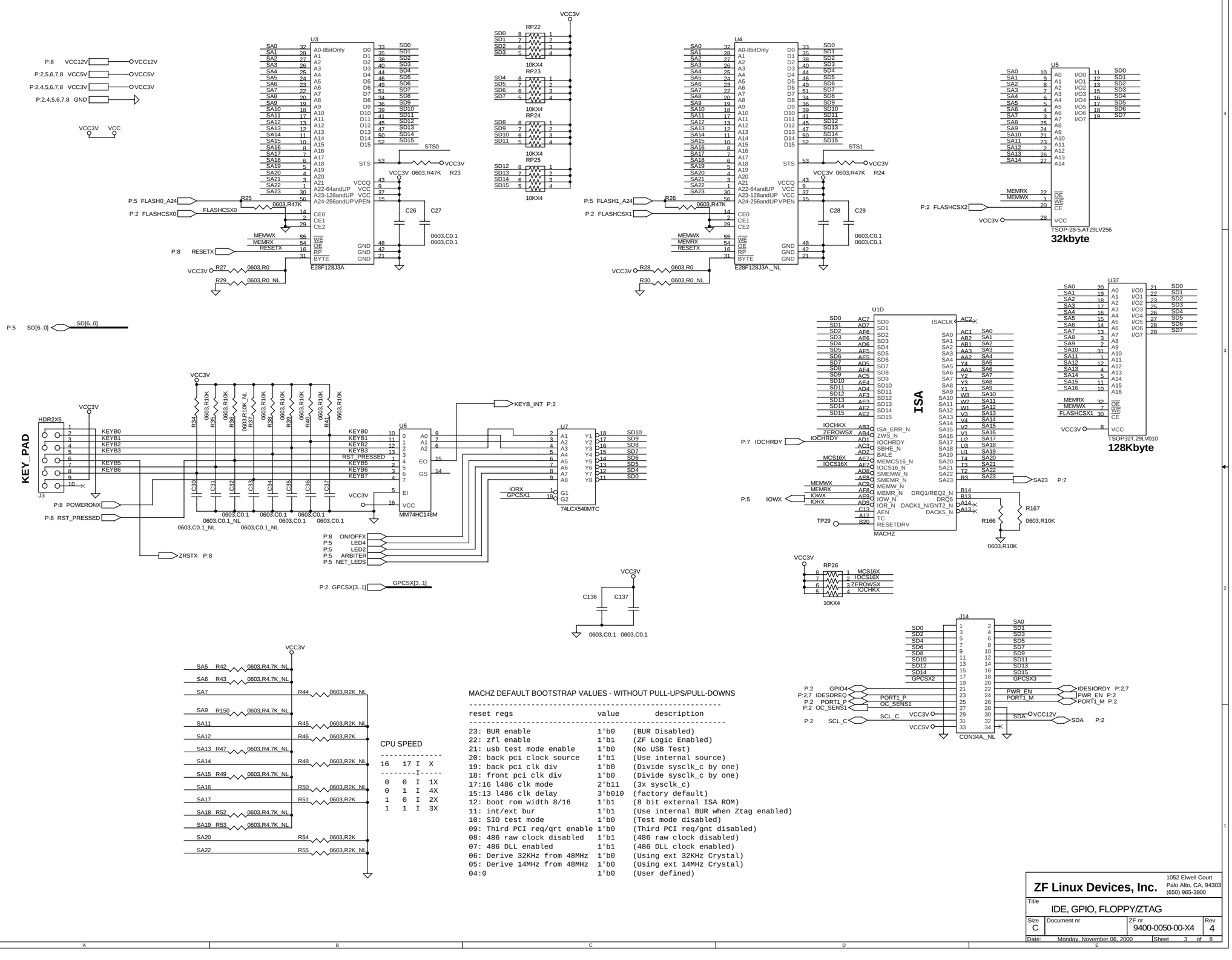
Title: MACHZ

Size	Document nr	ZF nr	Rev
C		9400-0050-00-X4	4

Date: Monday, November 06, 2000 Sheet 2 of 8



CPU SPEED

16	17	I	X
0	0	I	1X
0	1	I	4X
1	0	I	2X
1	1	I	3X

MACHZ DEFAULT BOOTSTRAP VALUES - WITHOUT PULL-UPS/PULL-DOWNS

reset regs	value	description
23: BUR enable	1'b0	(BUR Disabled)
22: zfl enable	1'b1	(ZF Logic Enabled)
21: usb test mode enable	1'b0	(No USB Test)
20: back pci clock source	1'b1	(Use internal source)
19: back pci clk div	1'b0	(Divide sysclk_c by one)
18: front pci clk div	1'b0	(Divide sysclk_c by one)
17:16 l486 clk mode	2'b11	(3x sysclk_c)
15:13 l486 clk delay	3'b010	(factory default)
12: boot rom width 8/16	1'b1	(8 bit external ISA ROM)
11: int/ext bur	1'b1	(Use internal BUR when Ztag enabled)
10: SIO test mode	1'b0	(Test mode disabled)
09: Third PCI req/grt enable	1'b0	(Third PCI req/gnt disabled)
08: 486 raw clock disabled	1'b1	(486 raw clock disabled)
07: 486 DLL enabled	1'b1	(486 DLL clock enabled)
06: Derive 32KHz from 48MHz	1'b0	(Using ext 32KHz Crystal)
05: Derive 14MHz from 48MHz	1'b0	(Using ext 14MHz Crystal)
04:0	1'b0	(User defined)

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(650) 965-3800

Title: IDE, GPIO, FLOPPY/ZTAG

Size	Document nr	ZF nr	Rev
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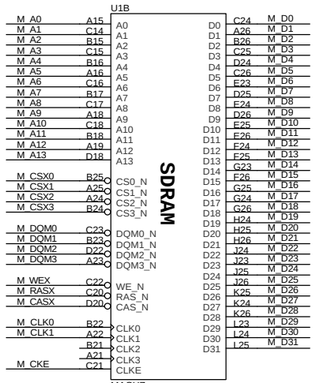

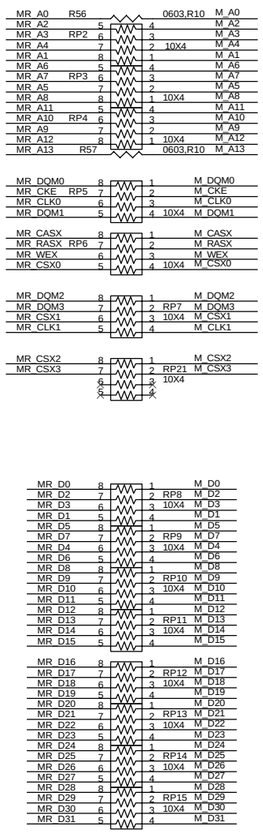

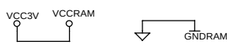

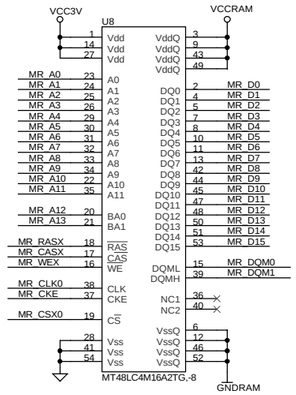

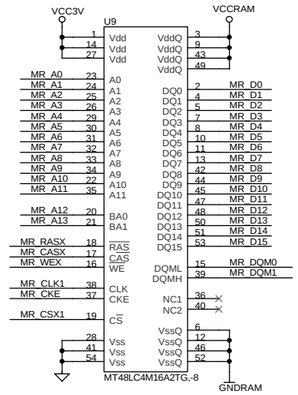

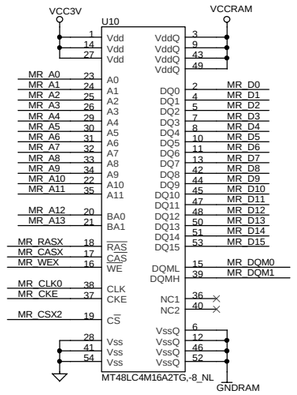

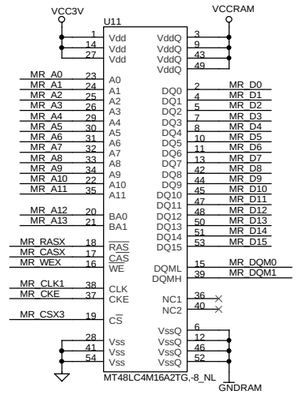

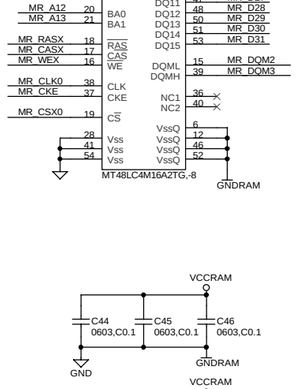

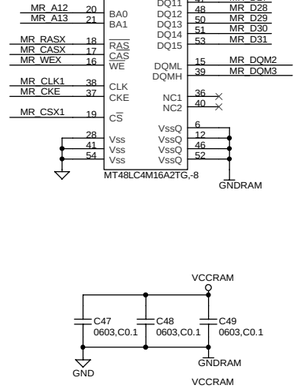

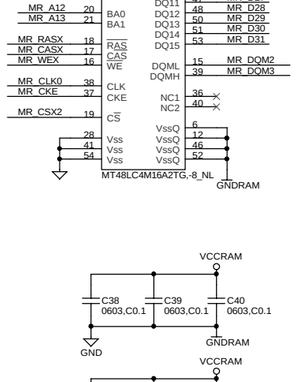

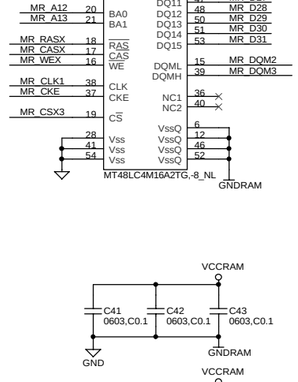

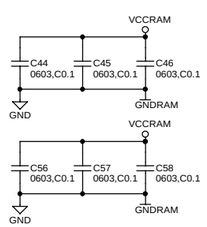

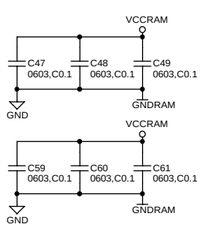

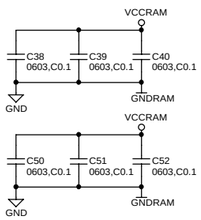

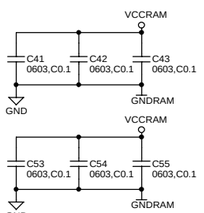

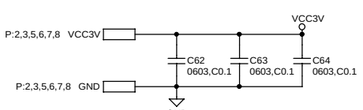

ZF Linux Devices, Inc.	1052 Elwell Court Palo Alto, CA, 94303 (650) 965-3800		
Title: SDRAM - DIMM			
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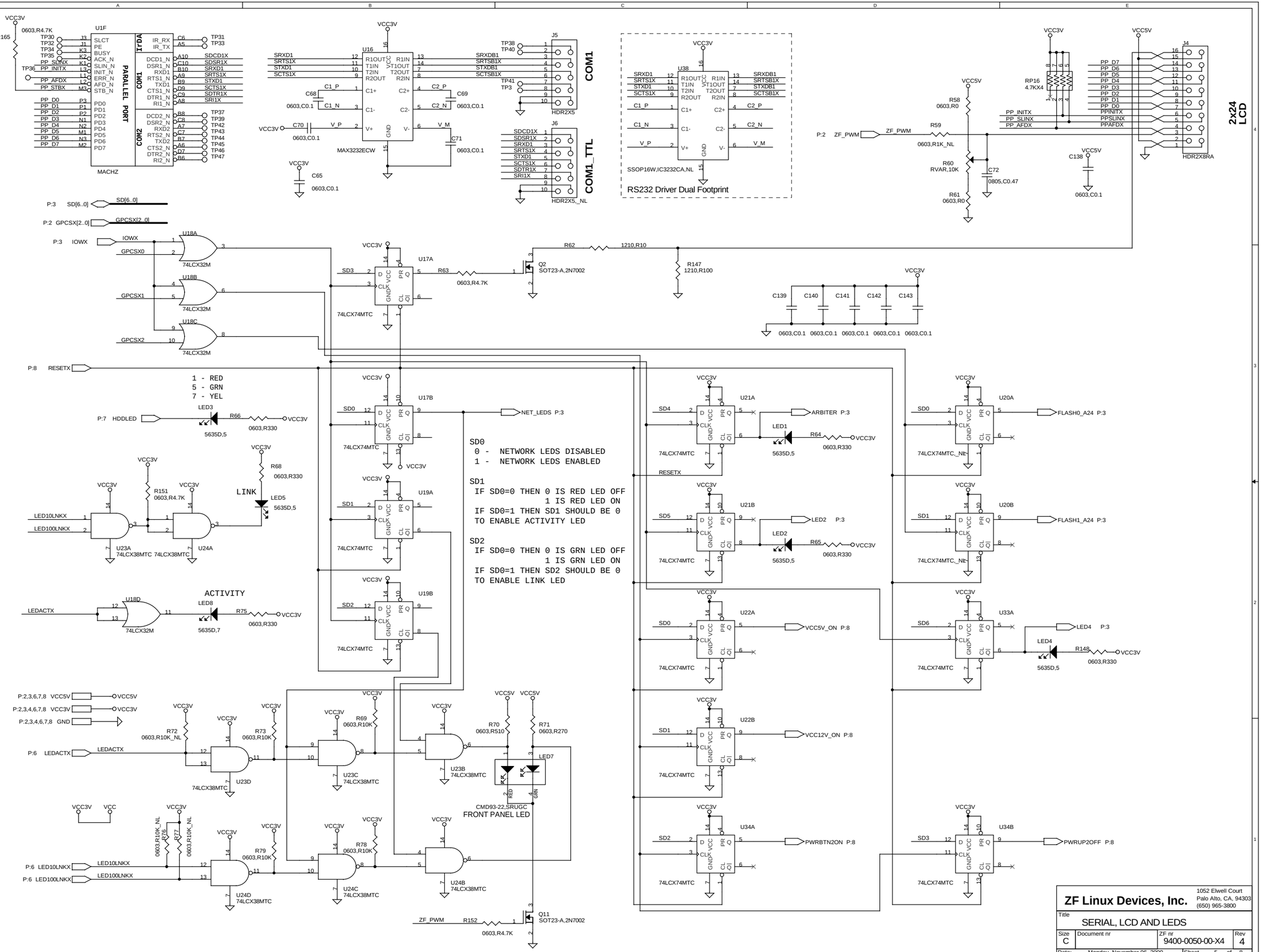
U1F
PARALLEL PORT
MACHZ
U16
MAX3232ECW
J5
COM1
J6
COM1_TTL
HDR2X5
HDR2X5_.NL
U38
SSOP16W,IC3232CA,NL
RS232 Driver Dual Footprint
RP16
4.7KX4
J4
HDR2X8RA
2x24
LCD
U18A
U18B
U18C
74LCX32M
U17A
U17B
U19A
U19B
74LCX74MTC
Q2
SOT23-A,2N7002
U21A
U21B
U20A
U20B
74LCX74MTC_NE
U22A
U22B
U33A
U34A
U34B
U23A
U23B
U23C
U23D
74LCX38MTC
U24A
U24B
U24C
U24D
U18D
LED3
LED1
LED2
LED4
LED5
LED7
LED8
5635D,5
5635D,7
CMD93-22,SRUGC
FRONT PANEL LED
Q11
SOT23-A,2N7002
1 - RED
5 - GRN
7 - YEL
LINK
ACTIVITY
SD0
0 - NETWORK LEDS DISABLED
1 - NETWORK LEDS ENABLED
SD1
IF SD0=0 THEN 0 IS RED LED OFF
1 IS RED LED ON
IF SD0=1 THEN SD1 SHOULD BE 0
TO ENABLE ACTIVITY LED
SD2
IF SD0=0 THEN 0 IS GRN LED OFF
1 IS GRN LED ON
IF SD0=1 THEN SD2 SHOULD BE 0
TO ENABLE LINK LED
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Title
SERIAL, LCD AND LEDS
Size C
Document nr
ZF nr 9400-0050-00-X4
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Date: Monday, November 06, 2000
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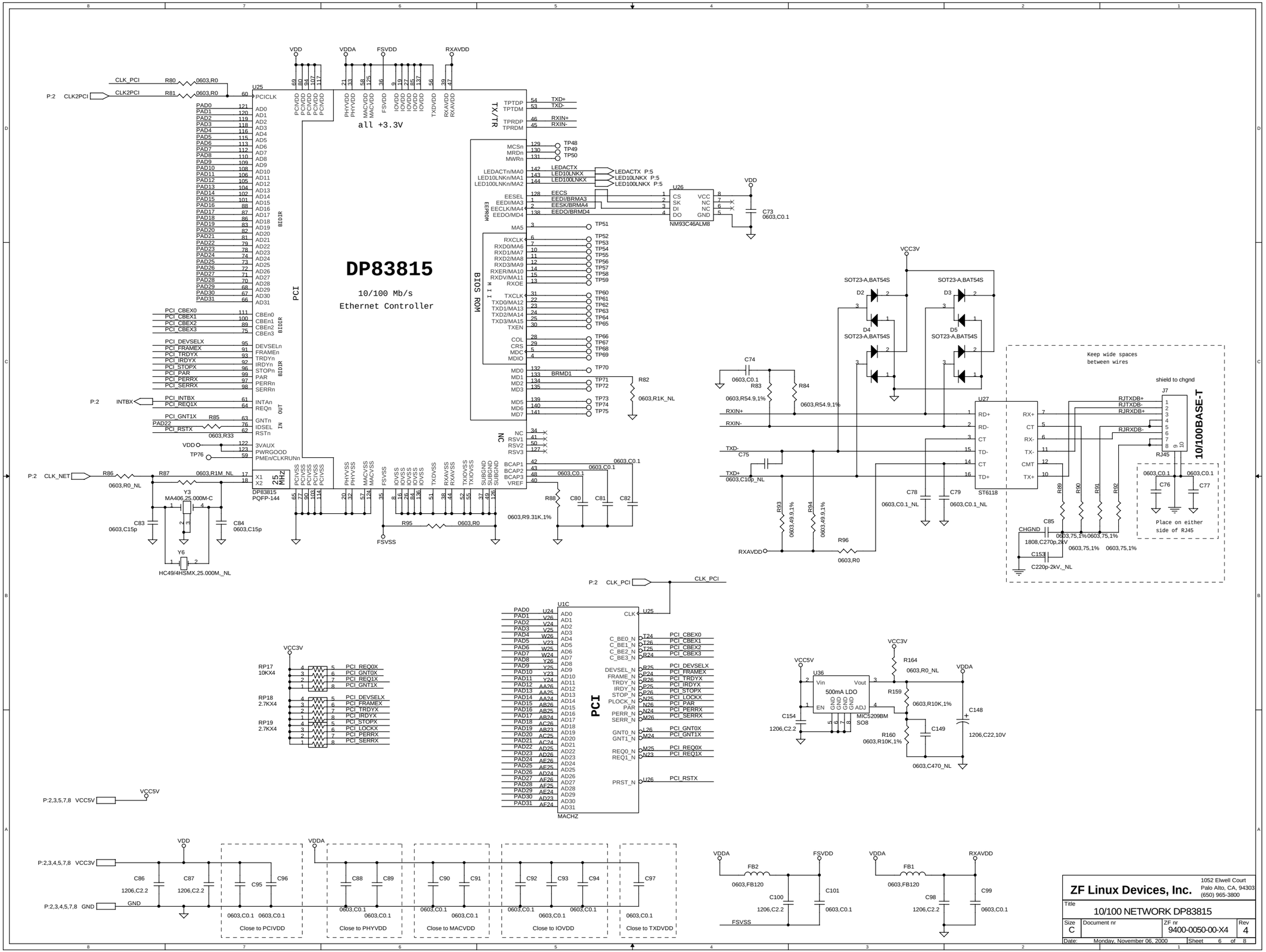
DP83815
10/100 Mb/s
Ethernet Controller
all +3.3V
PCI
BIOS ROM
TX/TR
U25
DP83815
PQFP-144
U26
NM93C46ALM8
U27
ST6118
U1C
MACHZ
U36
500mA LDO
MIC5209BM
SO8
J7
RJ45
10/100BASE-T
Keep wide spaces between wires
shield to chgnd
Place on either side of RJ45
Close to PCIVDD
Close to PHYVDD
Close to MACVDD
Close to IOVDD
Close to TXDVDD
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Title
10/100 NETWORK DP83815
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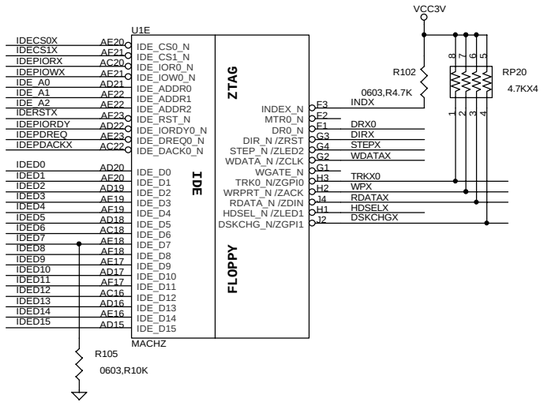
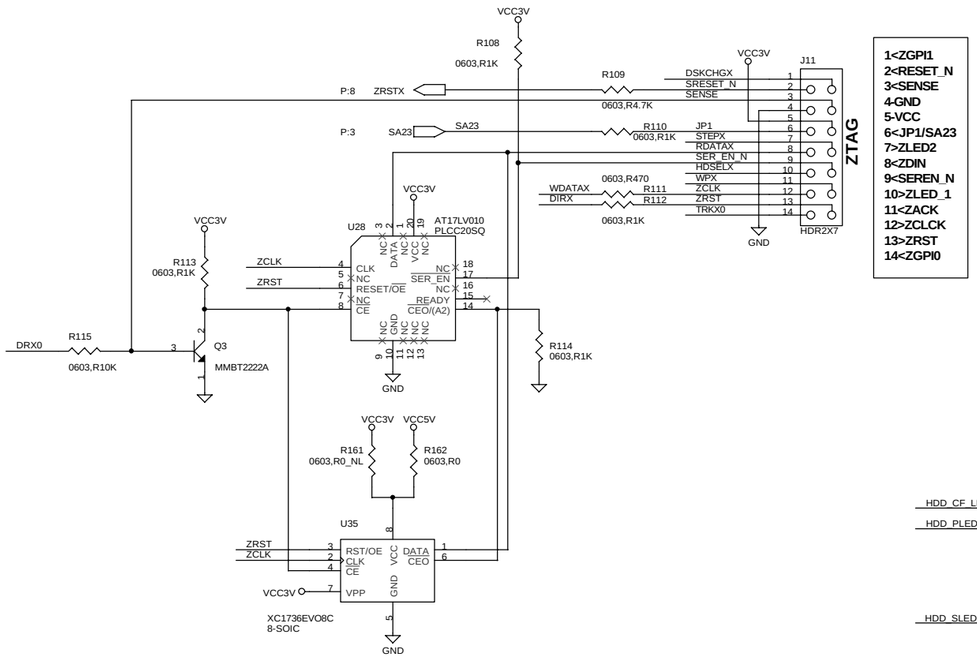
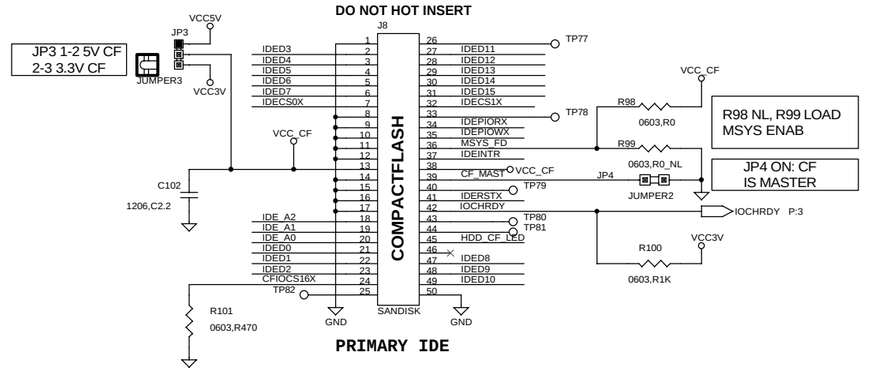
Sheet 6 of 8

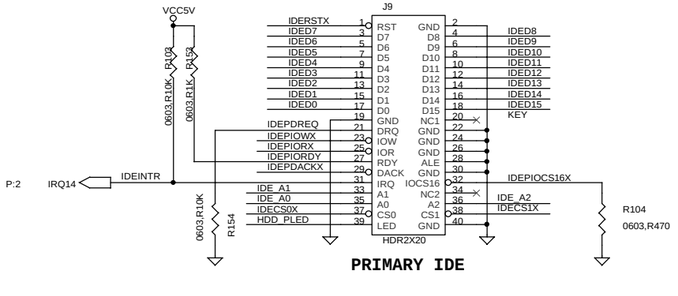
P:2,3,4,5,6,8 VCC3V → VCC3V

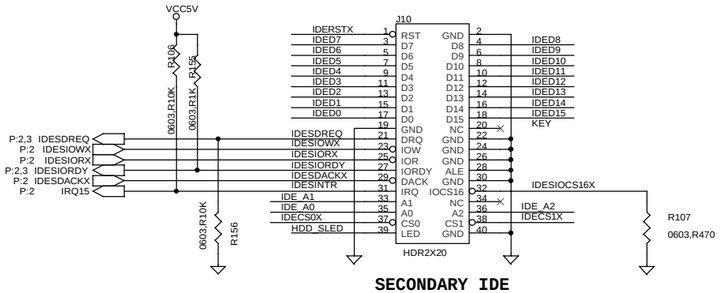
P:2,3,4,5,6,8 GND → GND



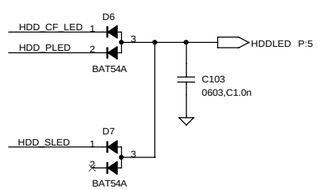








HDD ACT



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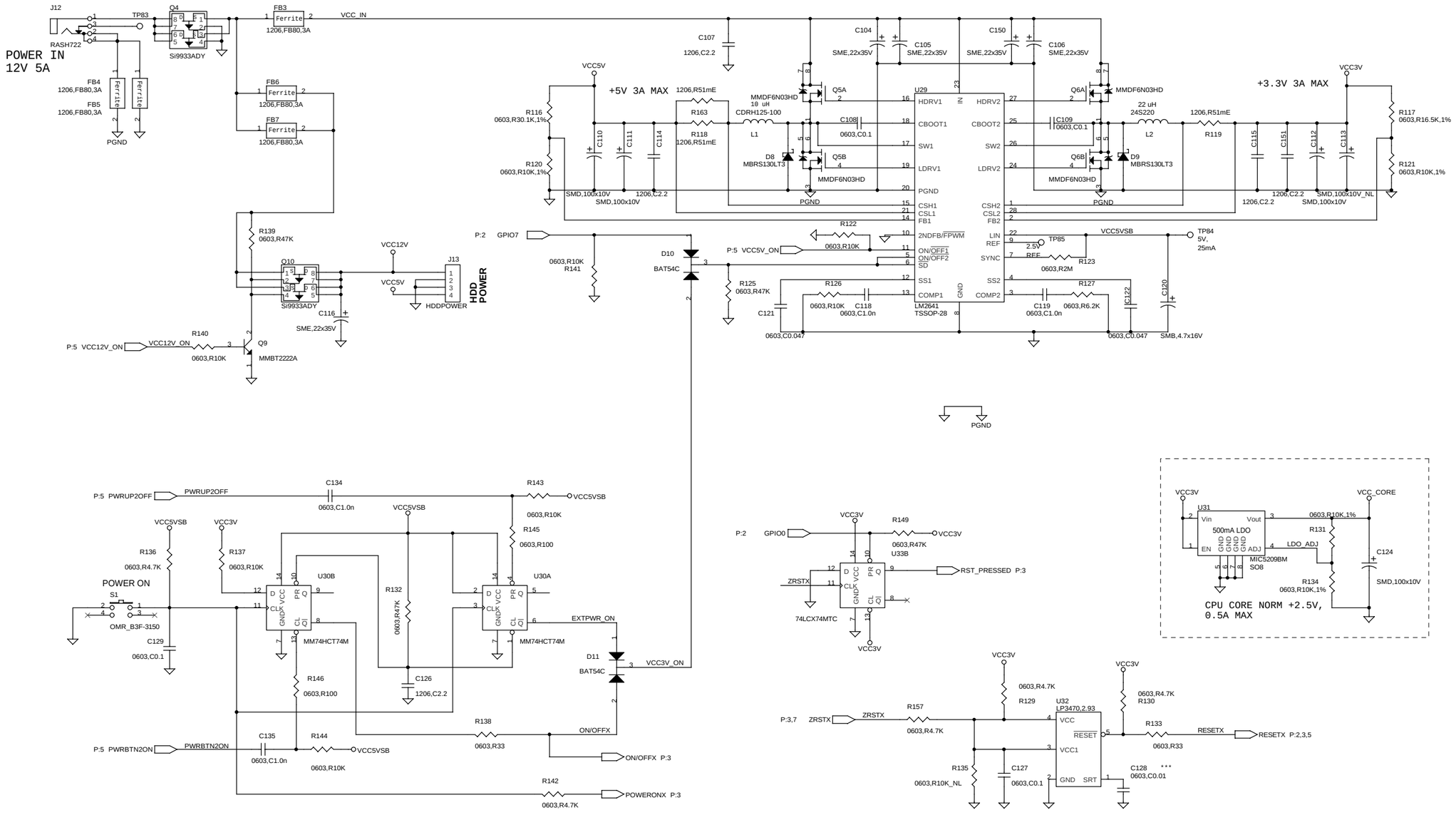
Title: IDE, FLOPPY/ZTAG		
Size: C	Document nr	ZF nr: 9400-0050-00-X4 — Rev: 4
Date: Monday, November 06, 2000		Sheet 7 of 8



ZF Linux Devices, Inc.	1052 Elwell Court Palo Alto, CA, 94303 (650) 965-3800		
Title: POWER, RESET, FRONT PANEL			
Size: C	Document nr:	ZF nr: 9400-0050-00-X4	Rev: 4
Date: Monday, November 06, 2000		Sheet 8 of 8	