

Key Design Features

- Synthesizable, technology independent VHDL Core
- SPI™ serial-bus compliant
- Supports up to 16 slave devices
- Intuitive command interface featuring a simple valid-ready handshake protocol
- Input/output FIFOs permit queuing of sequential SPI requests and corresponding read data
- Architecture allows sustained 8-bit read/write operations
- Configurable serial clock frequency
- Configurable clock polarity setting (CPOL)
- Configurable clock phase setting (CPHA)
- Capable of Full-duplex or Half-duplex operation
- Data rates of up to 40 Mbps¹

Applications

- Driving SPI slave devices
- Inter-chip board-level communications
- Robust communication at higher data rates than other serial protocols such as I2C, UART and USB 1.0

Generic Parameters

Generic name	Description	Type	Valid range
t_period	Serial clock period (in system clock cycles)	integer	≥ 5
cpol	Clock polarity	integer	0, 1 (As per SPI™ specification)
cpha	Clock phase	integer	0, 1 (As per SPI™ specification)
wfifo_depth	Master instruction write FIFO depth	integer	≥ 2
wfifo_depth_log2	Master instruction write FIFO depth log2	integer	log2(wfifo_depth)
rfifo_depth	Slave read data FIFO depth	integer	≥ 2
rfifo_depth_log2	Slave read data FIFO depth log2	integer	log2(rfifo_depth)

¹ Maximum attainable data rate will be determined by the choice of system clock frequency and the physical characteristics of the bus

Block Diagram

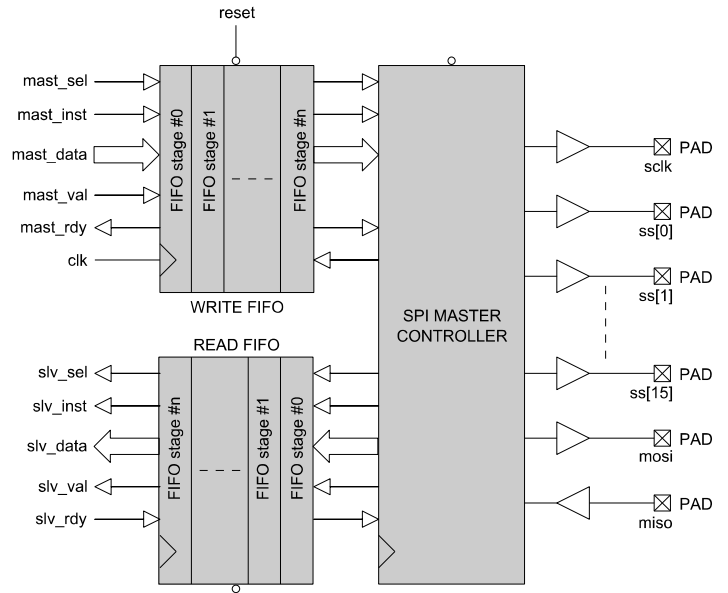


Figure 1: SPI Master Interface Controller architecture

Pin-out Description

Pin name	I/O	Description	Active state
clk	in	Synchronous clock	rising edge
reset	in	Asynchronous reset	low
mast_sel[3:0]	in	Slave device selection (0 to 15)	data
mast_inst[1:0]	in	Master instruction	data
mast_data[7:0]	in	Master data to be serialized	data
mast_val	in	Master instruction valid	high
mast_rdy	out	Master ready handshake	high
sclk	out	SPI™ serial clock	rising or falling edge ²
ss[15:0]	out	SPI™ slave select (One hot decode)	low
mosi	out	SPI™ Master out / Slave in	data
miso	in	SPI™ Master in / Slave out	data
slv_sel[3:0]	out	Slave device id	data
slv_inst[1:0]	out	Slave instruction	data
slv_data[7:0]	out	Slave data received from slave device	data
slv_val	out	Slave data valid	high
slv_rdy	in	Slave ready handshake	high

² Note that the serial clock characteristics are dependent on the CPOL and CPHA settings. See the SPI™ specification for more details

General Description

SPI_MASTER is an SPI™ compliant serial interface controller capable of driving up to 16 different slave devices in Full-Duplex operation. The controller receives data and instructions via the master instruction interface. These instructions are then processed by the controller core in order to generate the appropriate signals on the SPI bus. The serial slave data on the SPI bus is also captured by the controller and de-serialized for presentation at the slave read data port.

The SPI master controller is comprised of three main blocks as described by Figure 1. These blocks are the master instruction write FIFO, the SPI controller core and the slave read-data output FIFO.

The serial clock-period is determined by the the generic parameter *t_{period}*. This parameter specifies the *sclk* period in system clock cycles. As an example, if the system clock '*clk*' is running at 130MHz and a serial clock frequency of 10MHz is required, a value of *t_{period}* = 13 should be specified. In addition, the generic parameters *cpol* and *cpha* permit the clock polarity and phase characteristics to be specified as per the SPI™ specification. The table below shows a brief summary of these settings.

CPOL	CPHA	Description
0	0	Serial clock default state logic '0' Data sampled on rising-edge of serial clock Data sampled on falling-edge of serial clock
0	1	Serial clock default state logic '0' Data sampled on falling-edge of serial clock Data sampled on rising-edge of serial clock
1	0	Serial clock default state logic '1' Data sampled on falling-edge of serial clock Data sampled on rising-edge of serial clock
1	1	Serial clock default state logic '1' Data sampled on rising-edge of serial clock Data sampled on falling-edge of serial clock

Master Write FIFO

Instructions to the SPI master controller are sent via an input FIFO whose depth is determined by the generic parameter *wfifo_depth*. The write FIFO interface operates in accordance with the valid/ready pipeline protocol meaning that instructions and data are written to the FIFO on the rising edge of *clk* when *mast_val* is high and *mast_rdy* is high³

The write FIFO may be used to 'queue up' a sequence of commands and data while current commands are being processed on the bus. As soon as the write FIFO becomes full then the FIFO will disable the *mast_rdy* signal signifying that further requests are not possible.

Likewise, the *mast_rdy* signal will also be disabled if the slave read-data FIFO becomes full. In both situations, no further commands will be accepted by the SPI controller until the FIFOs have emptied.

The instructions to the SPI controller are very intuitive and follow the exact sequence of commands that the user wishes to appear on the SPI bus. The following table outlines the set of commands accepted by the controller via the Master write FIFO.

MASTER INSTRUCTION INPUT FORMAT

<i>mast_inst</i> [3:0]	<i>mast_data</i> [7:0]	Description
"00"	[7:0] : Write data	SPI WRITE Write 8-bits serially on the SPI bus. Ignore the read data bits (Half-duplex operation)
"01"	[7:0] : 'X' Don't care	SPI READ Read 8-bits serially on the SPI bus. Write data is don't care. (Half-duplex operation)
"10"	[7:0] : Write data	SPI READ/WRITE Read and write 8-bits serially on the SPI bus. (Full-duplex operation)
"11"	[7:0] :Don't care	NULL Dummy instruction. (May be used to force the slave select signal inactive between sequential SPI transfers)

As an example, to write two consecutive bytes followed by two consecutive reads from the same slave device with the slave select signal forced inactive-high in between, the instructions "00", "00", "11", "01", "01" would be sent.

Of course, the exact sequence of instructions required will depend on the functionality of the slave device that is to be accessed. For this reason, there is no restriction in the ordering of instructions that may be sent to the SPI master controller.

SPI Master Controller Core

The master controller is a state-machine that accepts instructions from the write FIFO and generates the appropriate signals on the SPI bus. Immediately after an asynchronous reset of the core, the state machine starts in the reset state with the slave select lines '*ss*' inactive high. On receipt of the first valid instruction, the state machine will take control of the bus and drive the *sclk*, *ss* and *mosi* lines in response to the received instructions and data. If the instruction is a read operation, the controller will also sample the input serial data on the *miso* pin.

The default state of the serial clock and the edges in which the serial data are sampled and changed is dependent on the *cpol* and *cpha* settings as described earlier.

Slave Read FIFO

For every master instruction received by the controller, the controller also sends a copy of the original instruction plus the slave read data (if applicable) to the Slave read FIFO. In the case that the originating instruction was a slave write then the slave read data contains a copy of the original master data. The following table gives a brief summary of the instruction format.

³ See Zipcores application note: [app_note_zc001.pdf](#) for more examples of the valid/ready protocol and it's implementation

SLAVE INSTRUCTION OUTPUT FORMAT

<i>slv_inst</i> [3:0]	<i>slv_data</i> [7:0]	Description
"00"	[7:0] : (same as original <i>mast_data</i>)	SPI WRITE
"01"	[7:0] : (same as original <i>mast_data</i>)	SPI READ
"10"	[7:0] : (same as original <i>mast_data</i>)	SPI READ/WRITE
"11"	[7:1] : Slave Address [0] : R/W flag	ADDR

Note that the *slv_inst* outputs are identical to the *mast_inst* inputs. The exception is the NULL instruction where nothing is logged in the slave read FIFO.

Functional Timing

Figure 2 shows a simple series of instructions sent to the controller. The sequence is: WRITE, READ, WRITE and READ/WRITE. Note that the FIFO is full after the third instruction and *mast_rdy* is de-asserted for one clock cycle. In the following cycle, *mast_rdy* goes high and the final instruction is transferred.

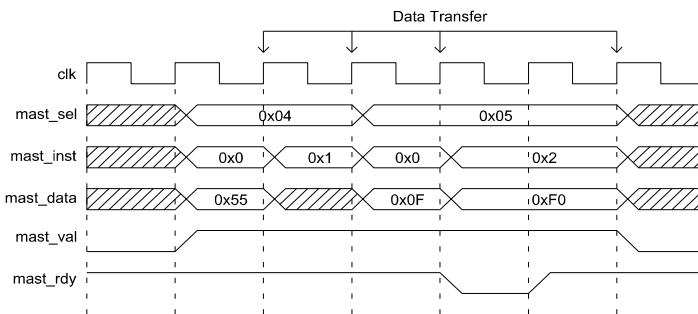


Figure 2: Master Instruction interface timing

Figure 3 demonstrates the series of responses on the Slave port for the same set of instructions.

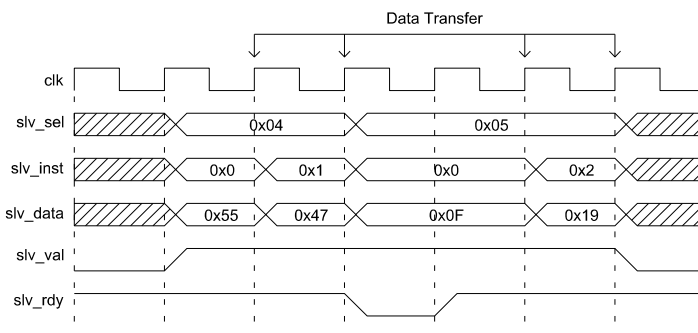


Figure 3: Slave Instruction interface timing

Finally, Figure 4 demonstrates the corresponding SPI bus signals that are generated in response to the sequence of instructions described above.

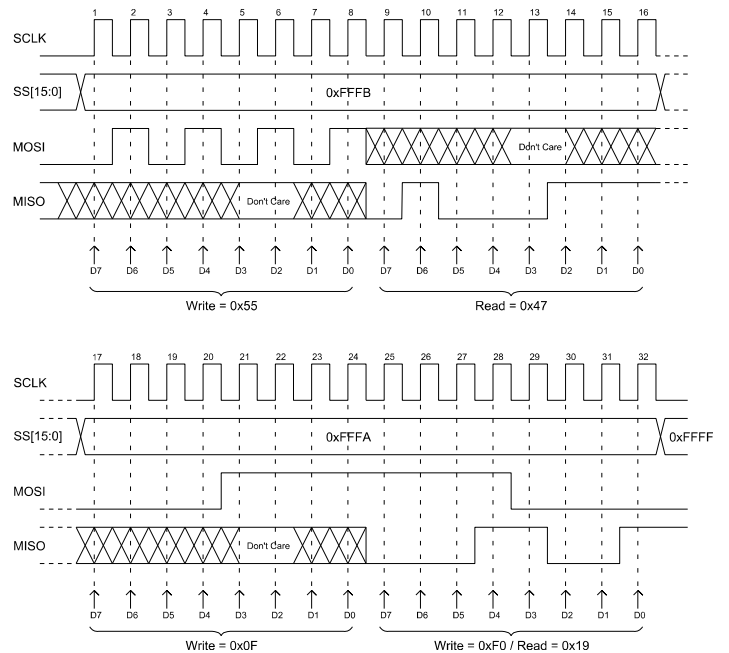


Figure 4: SPI bus signalling

Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

Source file	Description
<i>spi_fifo.vhd</i>	Input/output FIFOs
<i>spi_master_cont.vhd</i>	SPI master controller
<i>spi_master.vhd</i>	Top-level block
<i>spi_master_bench.vhd</i>	Top-level test bench

Functional Testing

An example VHDL test bench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. *spi_fifo.vhd*
2. *spi_master_cont.vhd*
3. *spi_mast.vhd*
4. *spi_master_bench.vhd*

The VHDL test bench instantiates the *spi_master* component in a loopback configuration – meaning that SPI writes are mirrored on the read SPI port. In addition, the user may modify the generic parameters on the SPI master component in order to select the desired clock relationships (CPOL/CPHA) and the desired serial clock frequency.

In the default set up, the simulation must be run for around 100 ms during which time a random sequence of instructions will be sent to the master controller.

The simulation generates two text files: *spi_master_in.txt* and *spi_master_out.txt*. These files respectively contain the input and output data captured at the master instruction and slave data ports during the course of the test. The contents of these two files may be compared to verify the operation of the SPI master controller.

Development Board Testing

The SPI Master Interface Controller was implemented on a Xilinx® 2V3000 FPGA running at a system clock frequency of 130MHz. The SPI Slave device was also implemented on the FPGA with the whole system initially set up to run at a serial clock frequency of 500KHz. After testing was performed at 500KHz, further testing was performed to verify correct operation at the higher frequency of 10MHz.

In all examples, the SPI mode was specified as mode 0,0 (CPOL = 0, CPHA = 0) meaning that data is sampled on the rising edge of the clock and changed on the falling edge. The default state of the clock is logic '0'.

Figure 6 below shows the relationship between the slave select signal and the serial clock. The top trace is *ss[0]* and the bottom trace is *sclk*. Notice that the slave select signal has a setup/hold time of at least 1/2 serial clock before and after the serial clock is enabled and disabled. This ensures compatibility with slower SPI slave devices.

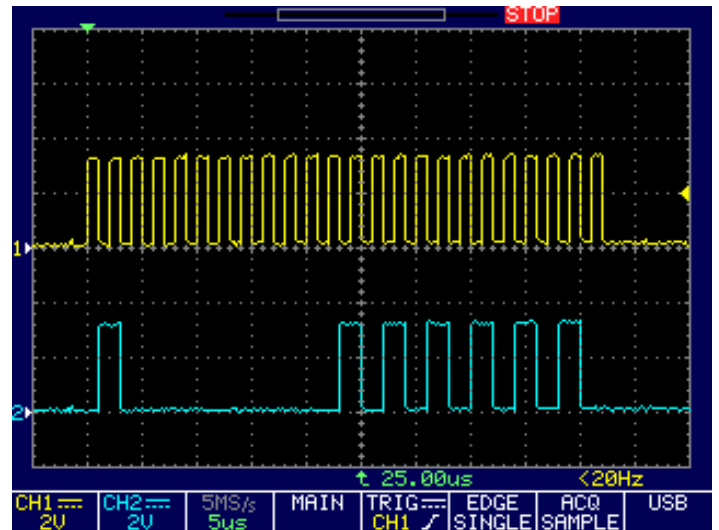


Figure 6: 24-bit SPI write detail at 500KHz

Finally, Figure 7 shows detail of a read operation at 10Mbps. This was achieved running at a system clock frequency of 130MHz with the generic parameter *t_{period}* set to 13.

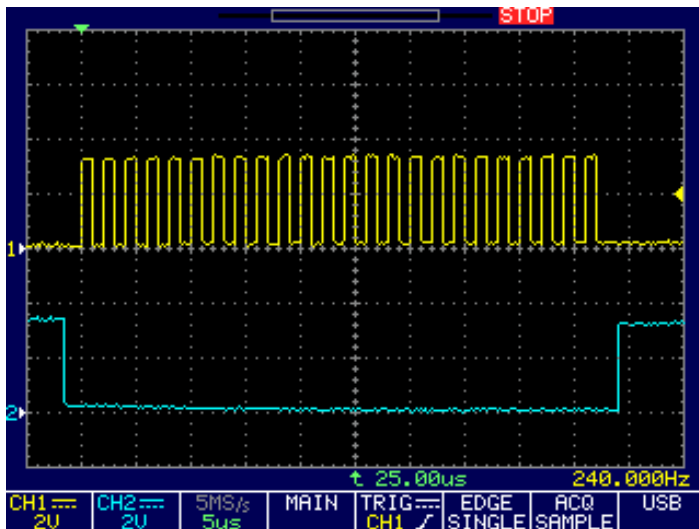


Figure 5: SPI serial clock/slave select relationship

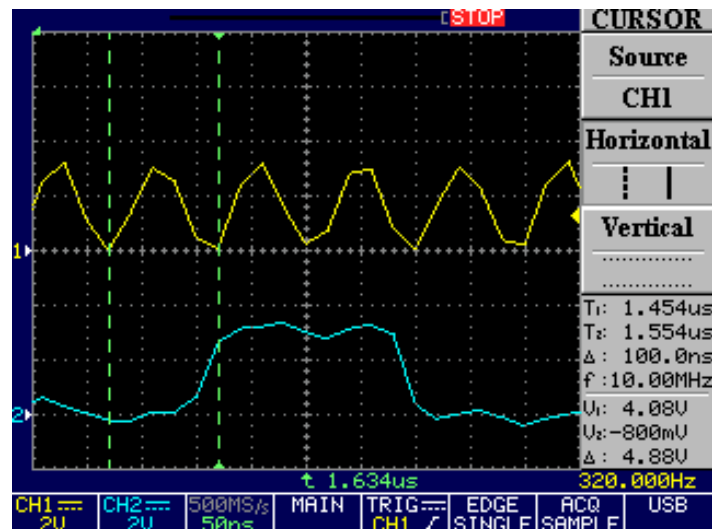


Figure 7: SPI read operation at 10Mbps

The next figure demonstrates the corresponding 3-byte write at 500KHz of the value 0x40, 0x0A, 0xAA. The top trace is the serial clock *sclk* and the bottom trace is the serial data out *mosi*.

Synthesis

The files required for synthesis and the design hierarchy is shown below:

- spi_master.vhd
 - spi_master_cont.vhd
 - spi_fifo.vhd

The VHDL core is designed to be technology independent. However, as a benchmark, synthesis results have been provided for the Xilinx® Virtex 6 and Spartan 6 FPGA devices. Synthesis results for other FPGAs and technologies can be provided on request.

Note that in order to achieve the fastest and most area efficient designs the size of the FIFOs should be kept to a minimum. Any unused slave select pins should be left open and the resulting logic will be optimized out during synthesis.

Trial synthesis results are shown with the generic parameters set to: $t_period = 5$, $cpol = 0$, $cpha = 0$, $wfifo_depth = 8$, $wfifo_depth_log2 = 3$, $rfifo_depth = 8$, $rfifo_depth_log2 = 3$.

Resource usage is specified after Place and Route.

VIRTEX 6

Resource type	Quantity used
Slice register	68
Slice LUT	157
Block RAM	0
DSP48	0
Occupied slices	54
Clock frequency (approx)	350 MHz

SPARTAN 6

Resource type	Quantity used
Slice register	70
Slice LUT	162
Block RAM	0
DSP48	0
Occupied slices	61
Clock frequency (approx)	250 MHz

Revision History

Revision	Change description	Date
1.0	Initial revision	30/03/2009
1.1	Fixed typos in pin-out description Updated synthesis results	23/02/2010
1.2	Updated synthesis results for Xilinx® 6 series FPGAs	31/05/2012