Key Design Features

- Synthesizable IP Core for all FPGA and ASIC technologies
- Supplied as human readable VHDL (or Verilog) source code
- Video (re)interlacer converts any progressive video format to it's interlaced equivalent – e.g. 1080p to 1080i
- Supports 24-bit RGB or 4:4:4 YCbCr pixels
- Supports all video resolutions up to 2^{16} x 2^{16}
- Fully pipelined architecture with simple valid-ready flow control
- Self-flushing design operates like a simple FIFO
- One frame in generates one interlaced field out
- Output rate is one pixel per clock
- Supports 500 MHz+ operation on basic FPGA devices

Applications

- Conversion of all standard and custom video formats such as 1920x1080p to 1920x1080i, 720x480p to 720x480i etc.
- Video solutions for flat panel displays, portable devices, video consoles, video format converters, set-top boxes, digital TV etc.

Pin-out Description

Pin name	I/O	Description	Active state
clk	in	Synchronous clock	rising edge
reset	in	Asynchronous reset	low
pixels_per_line [15:0]	in	Number of pixels per input line of video	data
lines_per_frame [15:0]	in	Number of lines per input frame of video	data
pixin [23:0]	in	24-bit input pixel	data
pixin_vsync	in	Vertical sync in	high
pixin_hsync	in	Horizontal sync in	high
pixin_val	in	Input pixel valid	high
pixin_rdy	out	Ready to accept input pixel (handshake signal)	high
pixout [23:0]	out	24-bit output pixel	data
pixout_field	out	Output field number	0: odd, 1: even
pixout_vsync	out	Vertical sync out	high
pixout_hsync	out	Horizontal sync out	high
pixout_val	out	Output pixel valid	high
pixout_rdy	in	Ready to accept output pixel (handshake signal)	high

Block Diagram

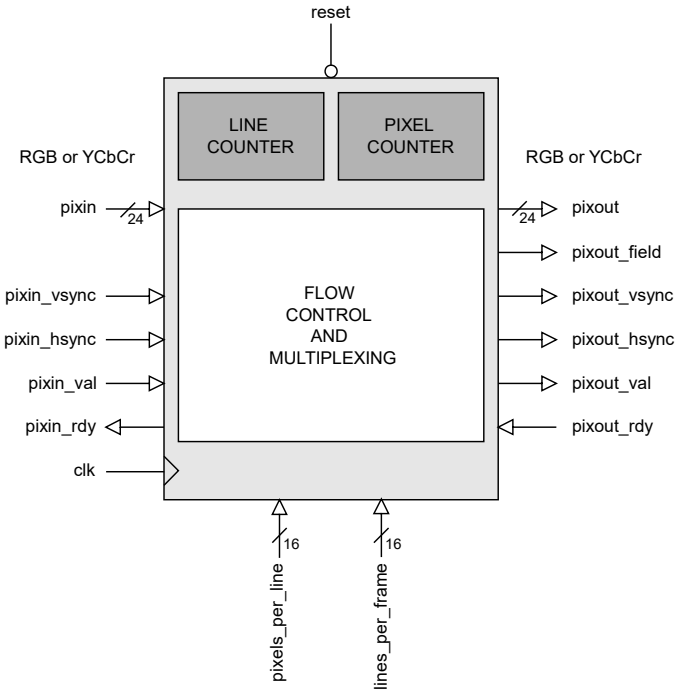

Figure 1: Video Interlacer architecture

General Description

The INTERLACER IP Core (Figure 1) is a fully pipelined video interlacer solution that converts any progressive video format into it's interlaced equivalent. The format of the input video is defined by the parameters *pixels_per_line* and *lines_per_frame*. These values specify the size of one input frame of video in pixels and lines. Each interlaced output field will have half the number of lines as an input frame.

The input and output interfaces are streaming interfaces that follow a simple valid-ready pipeline protocol[1]. Input pixels and syncs are sampled on the rising edge of *clk* when *pixin_val* and *pixin_rdy* are both high. Likewise, output pixels and syncs are sampled on the rising edge of *clk* when *pixout_val* and *pixout_rdy* are high. The interfaces are compatible with all Zipcores video IP Cores and allow for easy connectivity between modules.

The input sync signals *vsync* and *hsync* are sideband flags that are coincident with the first pixel of a frame and the first pixel of a line respectively. The output sync signals are coincident with the first pixel of an output *field.* Note that the output interface has an additional *field* flag that identifies whether the field is odd or even. This field flag is held high or low for the duration of the output field.

Note that if no flow control is required in the design and the output is guaranteed to accept pixels without stalling, then the signal *pixout_rdy* may be tied high and the signal *pixin_rdy* may be ignored.

1 Please see Zipcores application note: app_note_zc001.pdf for more examples of how to use the valid-ready pipeline protocol