Key Design Features

- Synthesizable, technology independent VHDL IP Core
- Conversion of pixels between RGB and YCbCr colour spaces
- Supports 24-bit RGB888 and 30-bit YCbCr 4:4:4 formats
- Fully pipelined architecture with simple flow control
- Features VSYNC and HSYNC sideband flags to keep track of video frame and line boundaries
- Output 1 x pixel per clock
- Small implementation size
- Support for 400 MHz+ operation on basic FPGA devices

Applications

- Digital video and image processing
- Interfacing between different video processing and video transceiver ICs that use different colour spaces

Pin-out Description

Pin name	*I/O*	*Description*	*Active state*
clk	in	Synchronous clock	rising edge
reset	in	Asynchronous reset	low
pixin_r [7:0]	in	Red component in	data
pixin_g [7:0]	in	Green component in	data
pixin_b [7:0]	in	Blue component in	data
pixin_y [9:0]	in	Luma Component in	data
pixin_cb [9:0]	in	Chroma (Blue) component	data
pixin_cr [9:0]	in	Chroma (Red) component	data
pixin_vsync	in	Vertical sync flag in	high
pixin_hsync	in	Horizontal sync flag in	high
pixin_val	in	Input pixel valid	high
pixin_rdy	out	Input pixel ready	high
pixout_r [7:0]	out	Red component out	data
pixout_g [7:0]	out	Green component out	data
pixout_b [7:0]	out	Blue component out	data
pixout_y [9:0]	out	Luma Component out	data
pixout_cb [9:0]	out	Chroma (Blue) component	data
pixout_cr [9:0]	out	Chroma (Red) component	data
pixout_vsync	out	Vertical sync flag out	high
pixout_hsync	out	Horizontal sync flag out	high
pixout_val	out	Output pixel valid	high
pixout_rdy	in	Output pixel ready	high

Block Diagram

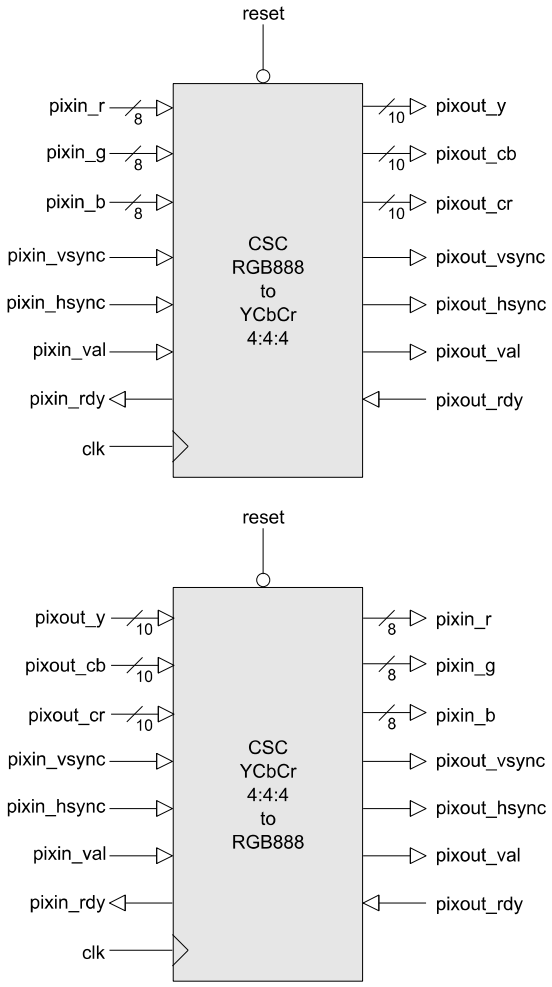

Figure 1: Colour-Space Converter architecture

General Description

The CSC IP Core (Figure 1) is a fully pipelined colour-space converter that converts pixels between the RGB and YCbCr colour spaces. In total, the IP Core package contains two distinct modules – one module that converts from 24-bit RGB to 30-bit 4:4:4 YCbCr and the other that performs the reciprocal operation from 4:4:4 YCbCr to RGB.

Pixels flow into the design in accordance with the valid ready pipeline protocol[1]. Input pixels and syncs are sampled on the rising edge of *clk* when *pixin_val* and *pixin_rdy* are both high. At the output interface, pixels and syncs are sampled on a the rising edge of *clk* when *pixout_val and pixout_rdy* are high. The input and output sync signals are sideband flags that are coincident with the first pixel of a frame and the first pixel of a line. These are useful to identify the video frame and line boundaries and are included for compatibility with the rest of Zipcores video IP.

Note that if no flow control is required in the design and the output interface can always accept pixels, then the *pixout_rdy* signal may be tied high. Likewise, the *pixin_rdy* flag may be ignored in this case.

1 See Zipcores application note: app_note_zc001.pdf for more examples of how to use the valid-ready pipeline protocol