



PESDxS5UD series

Fivefold ESD protection diode arrays

Rev. 02 — 7 December 2006

Product data sheet

1. Product profile

1.1 General description

Fivefold ElectroStatic Discharge (ESD) protection diode arrays in a SOT457 (SC-74) small Surface-Mounted Device (SMD) plastic package designed to protect up to five signal lines from the damage caused by ESD and other transients.

1.2 Features

- ESD protection of up to five lines
- Max. peak pulse power: $P_{PP} = 200$ W
- Ultra low leakage current: $I_{RM} = 50$ pA
- Low clamping voltage: $V_{CL} = 12$ V at $I_{PP} = 20$ A
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); I_{PP} up to 20 A

1.3 Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Communication systems
- Portable electronics
- Subscriber Identity Module (SIM) card protection

1.4 Quick reference data

Table 1. Quick reference data

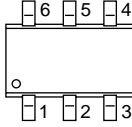
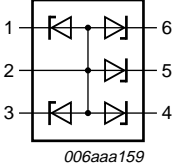
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per diode						
V_{RWM}	reverse standoff voltage					
	PESD3V3S5UD		-	-	3.3	V
	PESD5V0S5UD		-	-	5	V
	PESD12VS5UD		-	-	12	V
	PESD15VS5UD		-	-	15	V
	PESD24VS5UD		-	-	24	V

Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _d	diode capacitance	f = 1 MHz; V _R = 0 V				
	PESD3V3S5UD		-	215	300	pF
	PESD5V0S5UD		-	165	220	pF
	PESD12VS5UD		-	73	100	pF
	PESD15VS5UD		-	60	90	pF
	PESD24VS5UD		-	45	70	pF

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
1	cathode 1		
2	common anode		
3	cathode 2		
4	cathode 3		
5	cathode 4		
6	cathode 5		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD3V3S5UD	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457
PESD5V0S5UD			
PESD12VS5UD			
PESD15VS5UD			
PESD24VS5UD			

4. Marking

Table 4. Marking codes

Type number	Marking code
PESD3V3S5UD	E1
PESD5V0S5UD	E2
PESD12VS5UD	E3
PESD15VS5UD	E4
PESD24VS5UD	E5

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per diode					
P _{PP}	peak pulse power	t _p = 8/20 μs	[1][2] -	200	W
I _{PP}	peak pulse current	t _p = 8/20 μs	[1][2]		
	PESD3V3S5UD		-	20	A
	PESD5V0S5UD		-	20	A
	PESD12VS5UD		-	10	A
	PESD15VS5UD		-	6	A
	PESD24VS5UD		-	4	A
Per device					
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	+150	°C
T _{stg}	storage temperature		-65	+150	°C

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Measured from pin 1, 3, 4, 5 or 6 to 2.

Table 6. ESD maximum ratings

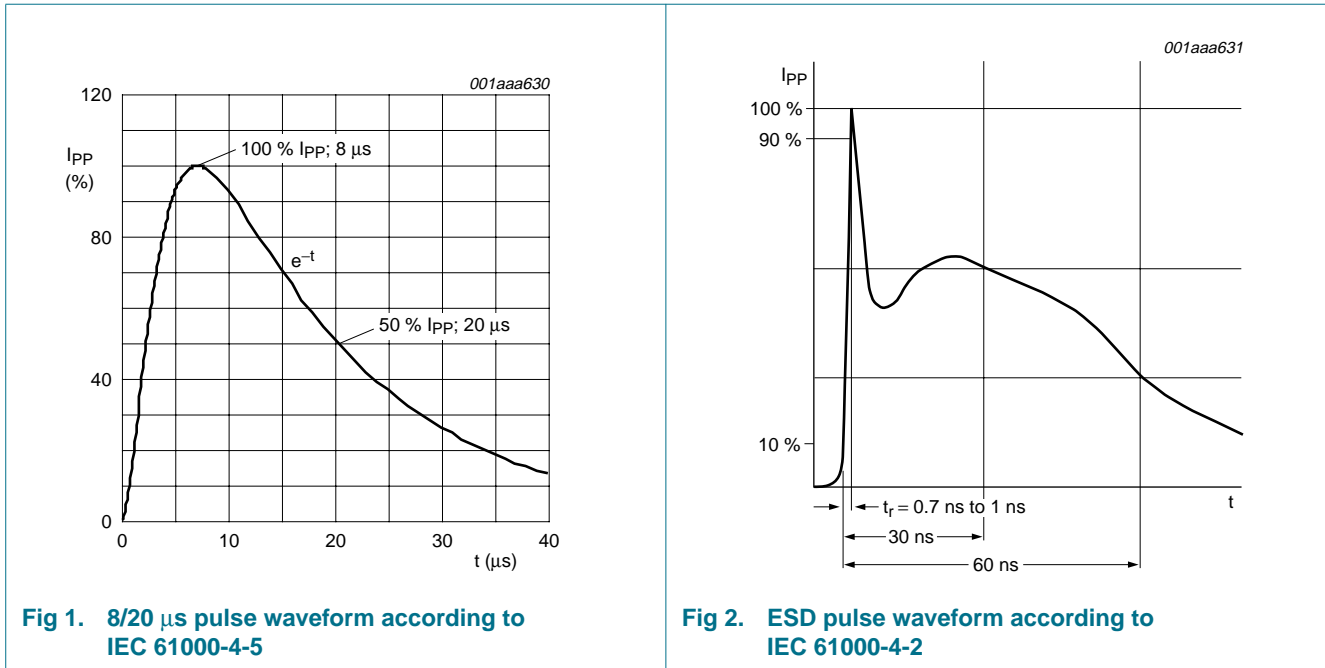
Symbol	Parameter	Conditions	Min	Max	Unit
Per diode					
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1][2]		
	PESD3V3S5UD		-	30	kV
	PESD5V0S5UD		-	30	kV
	PESD12VS5UD		-	30	kV
	PESD15VS5UD		-	30	kV
	PESD24VS5UD		-	23	kV
	PESDxS5UD series	MIL-STD-883 (human body model)	-	10	kV

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1, 3, 4, 5 or 6 to 2.

Table 7. ESD standards compliance

Standard	Conditions
Per diode	
IEC 61000-4-2; level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
MIL-STD-883; class 3 (human body model)	> 10 kV



6. Characteristics

Table 8. Characteristics
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per diode						
V _{RWM}	reverse standoff voltage					
	PESD3V3S5UD		-	-	3.3	V
	PESD5V0S5UD		-	-	5	V
	PESD12VS5UD		-	-	12	V
	PESD15VS5UD		-	-	15	V
PESD24VS5UD		-	-	24	V	
I _{RM}	reverse leakage current					
	PESD3V3S5UD	V _{RWM} = 3.3 V	-	300	800	nA
	PESD5V0S5UD	V _{RWM} = 5 V	-	80	200	nA
	PESD12VS5UD	V _{RWM} = 12 V	-	0.05	15	nA
	PESD15VS5UD	V _{RWM} = 15 V	-	0.05	15	nA
PESD24VS5UD	V _{RWM} = 24 V	-	0.05	15	nA	
V _{BR}	breakdown voltage	I _R = 1 mA				
	PESD3V3S5UD		5.3	5.6	5.9	V
	PESD5V0S5UD		6.4	6.8	7.2	V
	PESD12VS5UD		12.5	14.5	16	V
	PESD15VS5UD		17	18	19	V
PESD24VS5UD		25.5	27	29	V	

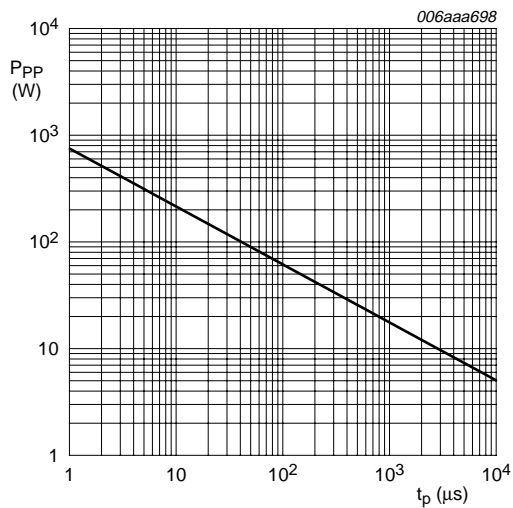
Table 8. Characteristics ...continued

$T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}$				
	PESD3V3S5UD		-	215	300	pF
	PESD5V0S5UD		-	165	220	pF
	PESD12VS5UD		-	73	100	pF
	PESD15VS5UD		-	60	90	pF
	PESD24VS5UD		-	45	70	pF
V_{CL}	clamping voltage		[1][2]			
	PESD3V3S5UD	$I_{PP} = 1\text{ A}$	-	-	8	V
		$I_{PP} = 20\text{ A}$	-	-	12	V
	PESD5V0S5UD	$I_{PP} = 1\text{ A}$	-	-	8	V
		$I_{PP} = 20\text{ A}$	-	-	13	V
	PESD12VS5UD	$I_{PP} = 1\text{ A}$	-	-	17	V
		$I_{PP} = 10\text{ A}$	-	-	24	V
	PESD15VS5UD	$I_{PP} = 1\text{ A}$	-	-	22	V
		$I_{PP} = 6\text{ A}$	-	-	33	V
	PESD24VS5UD	$I_{PP} = 1\text{ A}$	-	-	33	V
$I_{PP} = 4\text{ A}$		-	-	52	V	
r_{dif}	differential resistance	$I_R = 5\text{ mA}$	-	-	25	Ω

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Measured from pin 1, 3, 4, 5 or 6 to 2.



$T_{amb} = 25^{\circ}\text{C}$

Fig 3. Peak pulse power as a function of exponential pulse duration; typical values

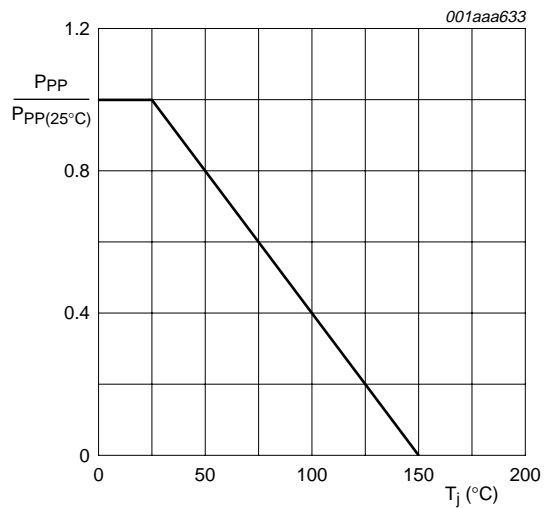
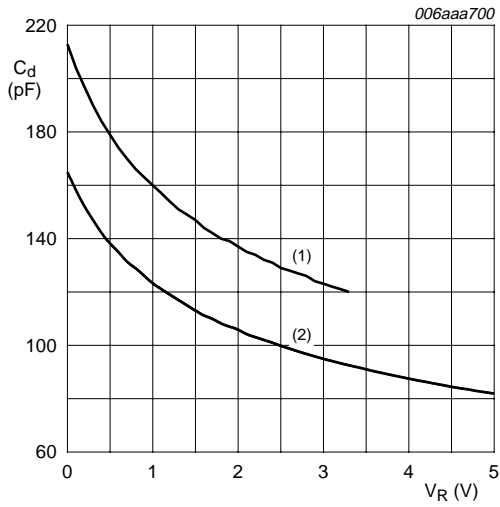
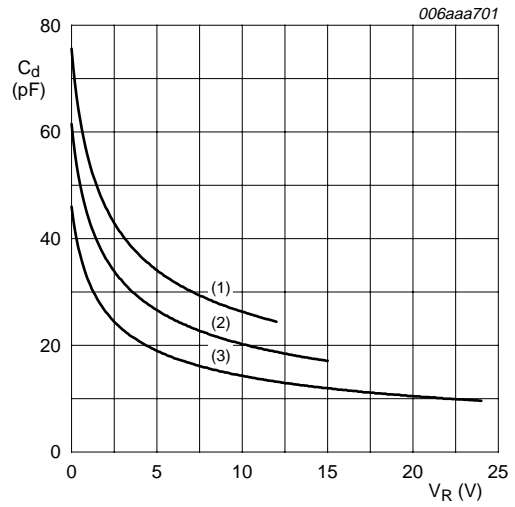


Fig 4. Relative variation of peak pulse power as a function of junction temperature; typical values



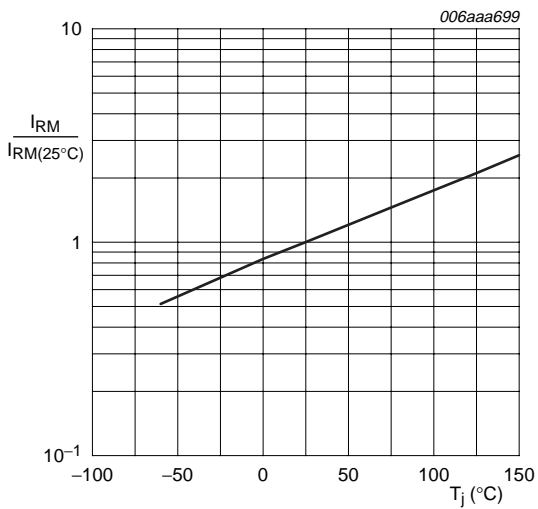
$f = 1 \text{ MHz}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$
 (1) PESD3V3S5UD
 (2) PESD5V0S5UD

Fig 5. Diode capacitance as a function of reverse voltage; typical values



$f = 1 \text{ MHz}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$
 (1) PESD12VS5UD
 (2) PESD15VS5UD
 (3) PESD24VS5UD

Fig 6. Diode capacitance as a function of reverse voltage; typical values



PESD3V3S5UD; PESD5V0S5UD
 I_R is less than 5 nA at 150 °C for:
 PESD12VS5UD; PESD15VS5UD; PESD24VS5UD

Fig 7. Relative variation of reverse leakage current as a function of junction temperature; typical values

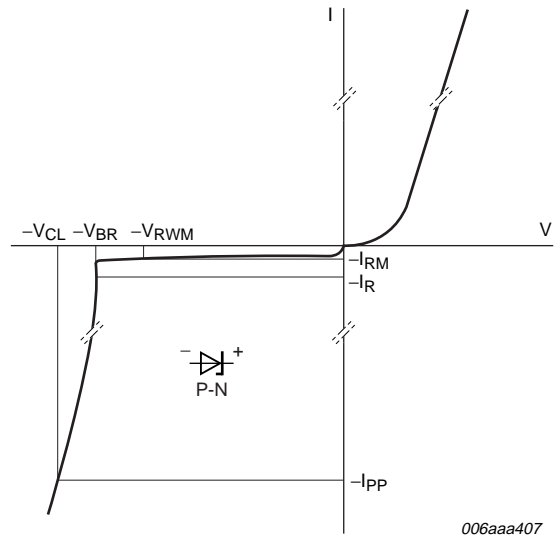


Fig 8. V-I characteristics for a unidirectional ESD protection diode

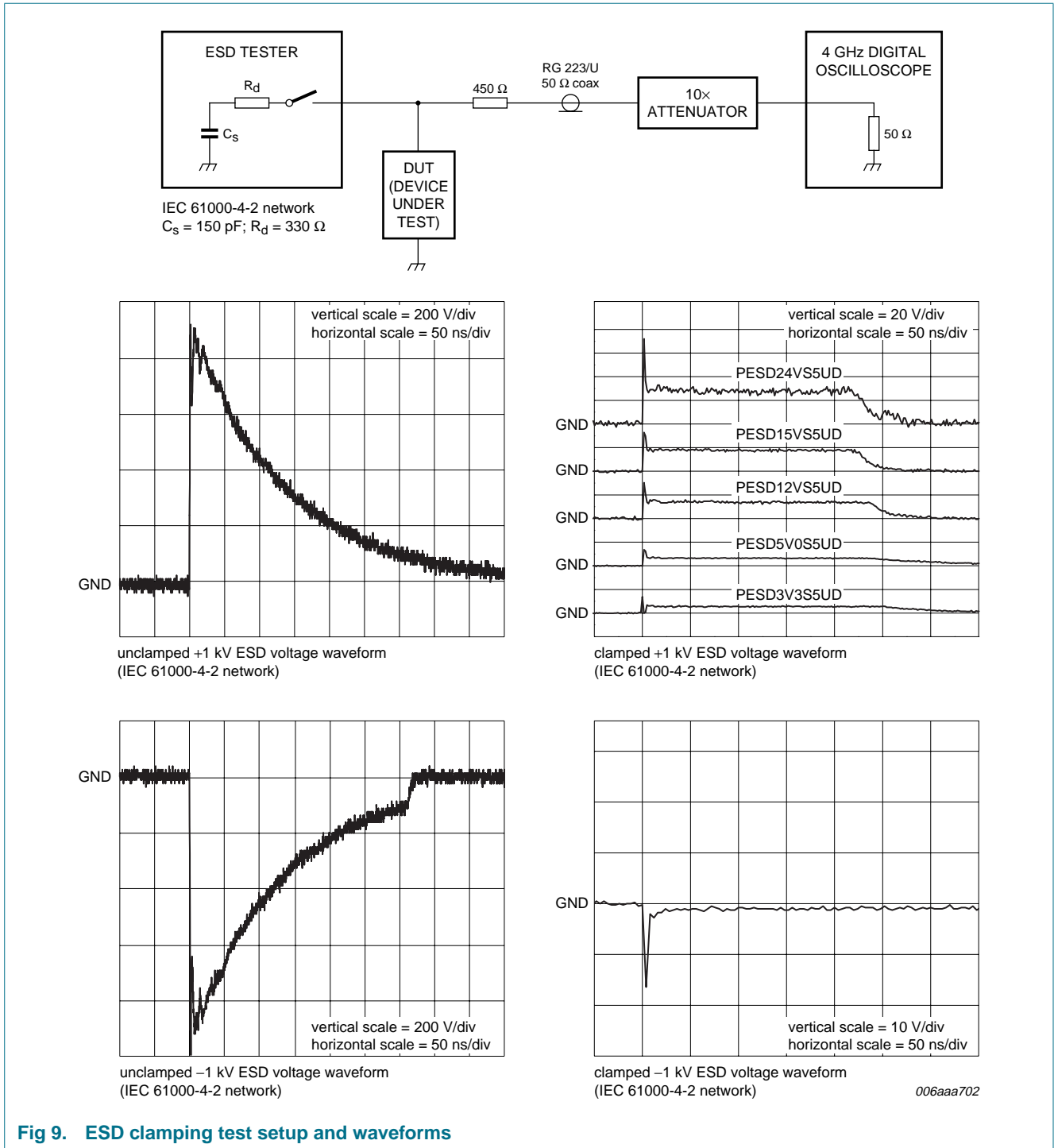


Fig 9. ESD clamping test setup and waveforms

7. Application information

The PESDxS5UD series is designed for the protection of up to five unidirectional data lines from the damage caused by ESD and surge pulses. The PESDxS5UD series may be used on lines where the signal polarities are both, positive and negative with respect to ground. The PESDxS5UD series provides a surge capability of 200 W per line for an 8/20 μ s waveform.

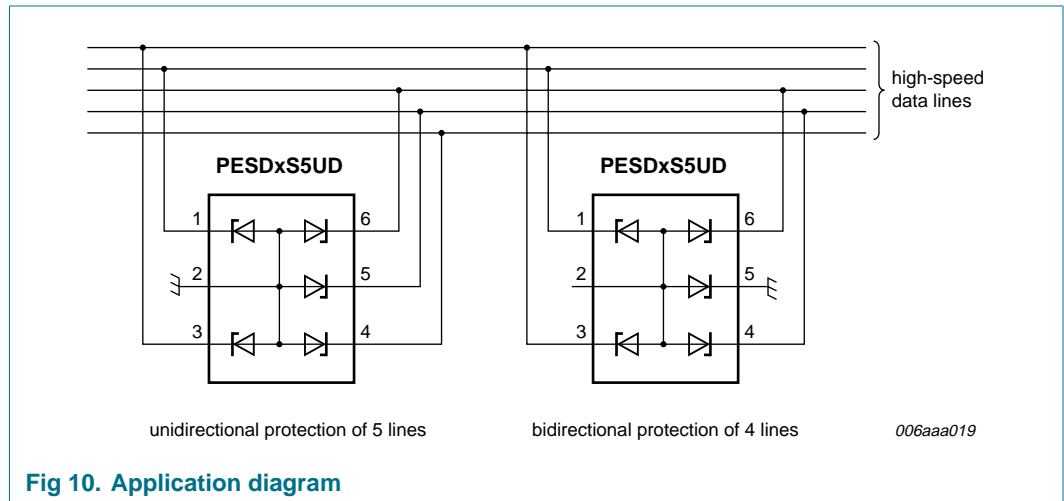


Fig 10. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the PESDxS5UD as close to the input terminal or connector as possible.
2. The path length between the PESDxS5UD and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

8. Package outline

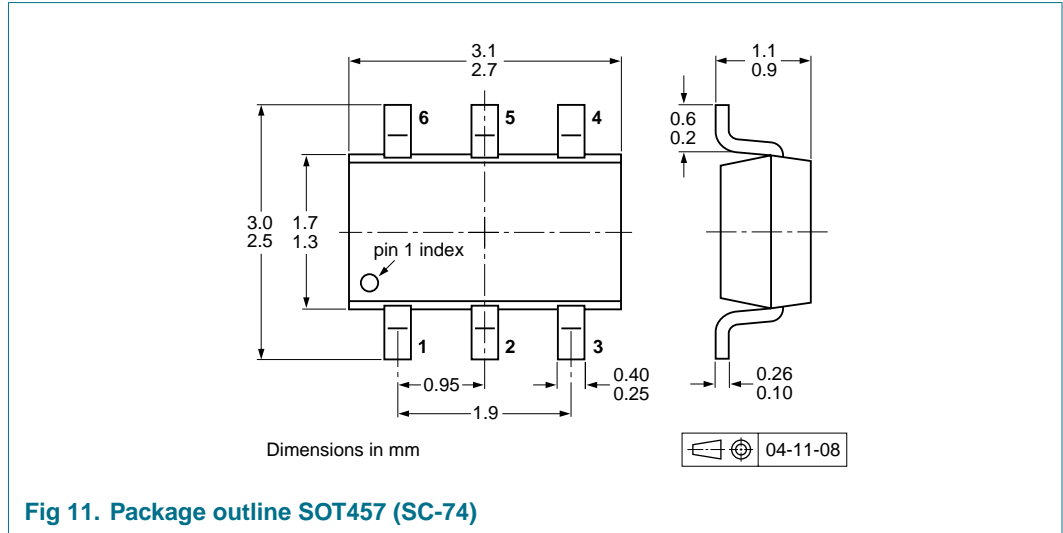


Fig 11. Package outline SOT457 (SC-74)

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

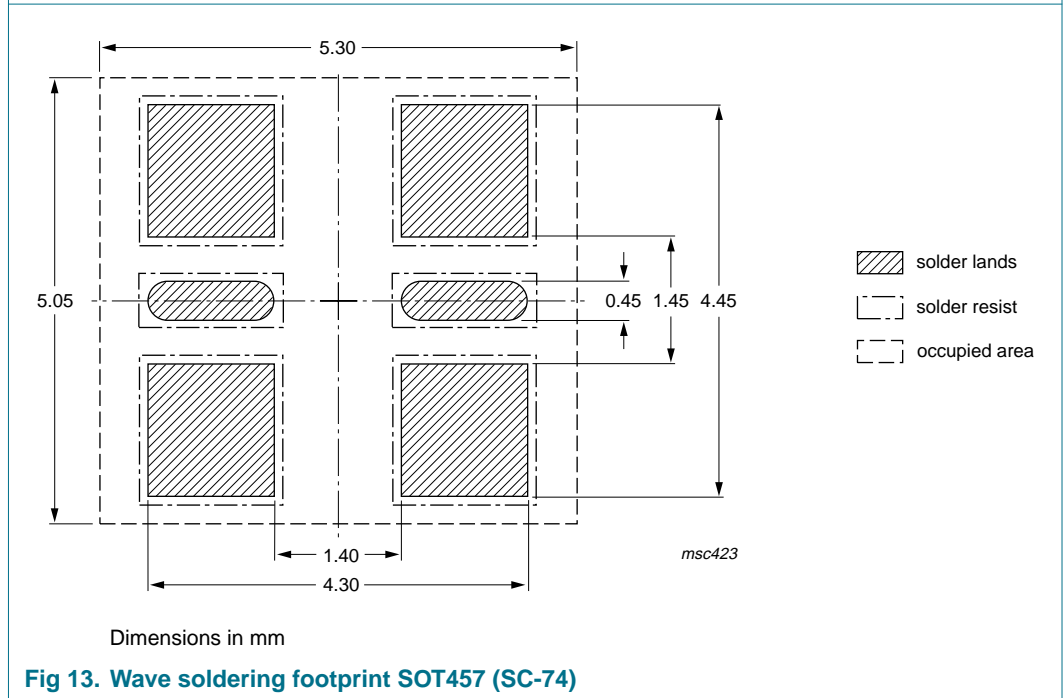
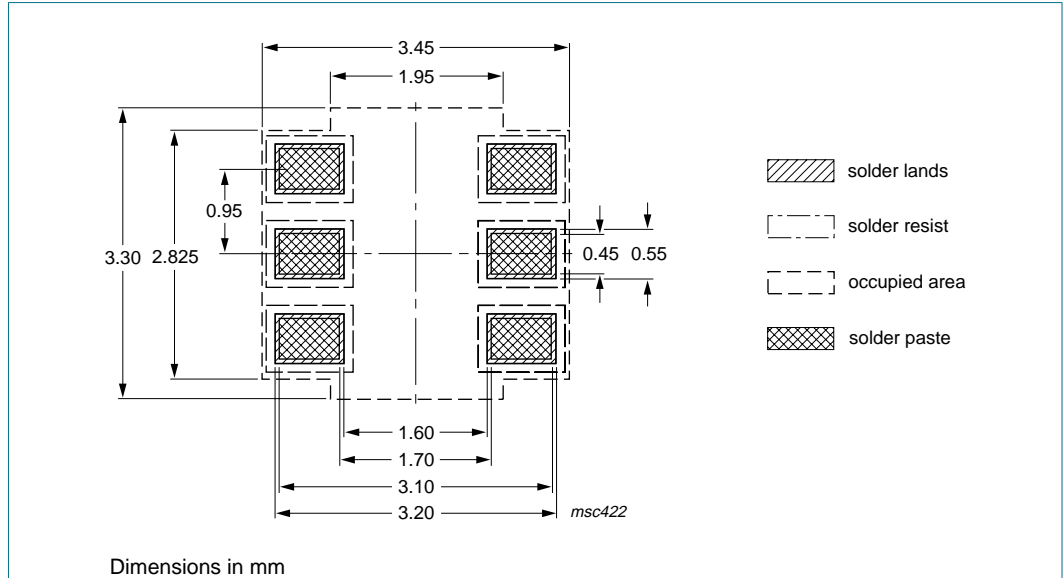
Type number	Package	Description	Packing quantity	
			3000	10000
PESD3V3S5UD	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2] -115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3] -125	-165
PESD5V0S5UD	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2] -115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3] -125	-165
PESD12VS5UD	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2] -115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3] -125	-165
PESD15VS5UD	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2] -115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3] -125	-165
PESD24VS5UD	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2] -115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3] -125	-165

[1] For further information and the availability of packing methods, see [Section 13](#).

[2] T1: normal taping

[3] T2: reverse taping

10. Soldering



11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESDXS5UD_SER_2	20061207	Product data sheet	-	PESDXS5UD_SER_1
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 2 "Pinning": symbol drawing amended • Table 5 "Limiting values": amended • Table 6 "ESD maximum ratings": amended • Table 7 "ESD standards compliance": amended • Table 8 "Characteristics": V_{BR} minimum and maximum values for PESD15VS5UD adapted • Figure 7: figure notes adapted • Section 10 "Soldering": added 			
PESDXS5UD_SER_1	20060404	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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