

NCP562, NCP563

80 mA CMOS Low Iq Low-Dropout Voltage Regulator

This series of fixed output low-dropout linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. This series features an ultra-low quiescent current of 2.5 μ A. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits. The NCP562 series provides an enable pin for ON/OFF control.

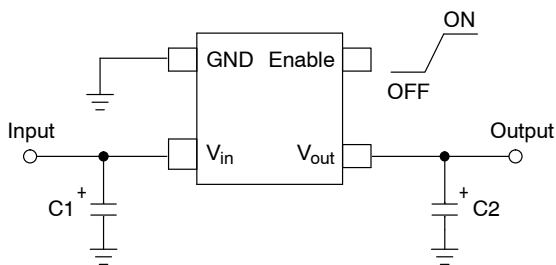
The NCP562/NCP563 has been designed to be used with low cost ceramic capacitors and requires a minimum output capacitor of 0.1 μ F. The device is housed in the micro-miniature SC82-AB surface mount package. Standard voltage versions are 1.5, 1.8, 2.5, 2.7, 2.8, 3.0, 3.3, 3.5 and 5.0 V. Other voltages are available in 100 mV steps.

Features

- Low Quiescent Current of 2.5 μ A Typical
- Low Output Voltage Option
- Output Voltage Accuracy of 2.0%
- Temperature Range of -40° C to 85° C
- NCP562 Provides an Enable Pin
- Pb-Free Packages are Available

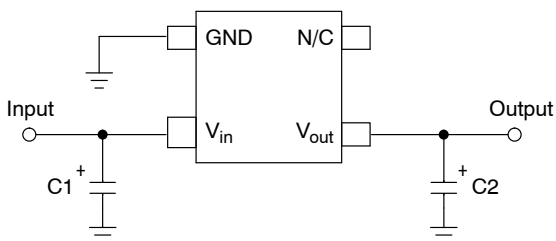
Typical Applications

- Battery Powered Instruments
- Hand-Held Instruments
- Camcorders and Cameras



This device contains 28 active transistors

Figure 1. NCP562 Typical Application Diagram



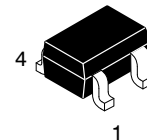
This device contains 28 active transistors

Figure 2. NCP563 Typical Application Diagram



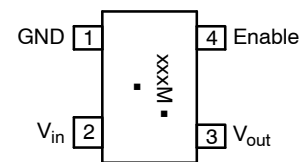
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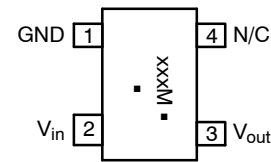


**SC82-AB (SC70-4)
SQ SUFFIX
CASE 419C**

PIN CONNECTIONS & MARKING DIAGRAMS



(NCP562 Top View)



(NCP563 Top View)

- xxx = Specific Device Code
- M = Month Code*
- = Pb-Free Package

(Note: Microdot may be in either location)
*Date Code orientation and/or position and underbar may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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PIN FUNCTION DESCRIPTION

| NCP562 | NCP563 | Pin Name | Description |
|--------|--------|------------------|---|
| 1 | 1 | GND | Power supply ground. |
| 2 | 2 | V _{in} | Positive power supply input voltage. |
| 3 | 3 | V _{out} | Regulated output voltage. |
| 4 | – | Enable | This input is used to place the device into low-power standby. When this input is pulled low, the device is disabled. If this function is not used, Enable should be connected to V _{in} . |
| – | 4 | N/C | No internal connection. |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|------------------------------------|------------------------------|-----------|
| Input Voltage | V _{in} | 6.0 | V |
| Enable Voltage (NCP562 ONLY) | Enable | –0.3 to V _{in} +0.3 | V |
| Output Voltage | V _{out} | –0.3 to V _{in} +0.3 | V |
| Power Dissipation and Thermal Characteristics Power Dissipation Thermal Resistance, Junction-to-Ambient | P _D R _{θJA} | Internally Limited 400 | W °C/W |
| Operating Junction Temperature | T _J | +150 | °C |
| Operating Ambient Temperature | T _A | –40 to +85 | °C |
| Storage Temperature | T _{stg} | –55 to +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V
2. Latch up capability (85°C) ±100 mA DC with trigger voltage.

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ELECTRICAL CHARACTERISTICS

($V_{in} = V_{out(nom.)} + 1.0\text{ V}$, $V_{enable} = V_{in}$, $C_{in} = 1.0\ \mu\text{F}$, $C_{out} = 1.0\ \mu\text{F}$, $T_J = 25^\circ\text{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|--------------------|--|---|--|-----------------------|
| Output Voltage ($T_A = 25^\circ\text{C}$, $I_{out} = 1.0\text{ mA}$) 1.5 V 1.8 V 2.5 V 2.7 V 2.8 V 3.0 V 3.3 V 3.5 V 5.0 V | V_{out} | 1.455 1.746 2.425 2.646 2.744 2.940 3.234 3.43 4.9 | 1.5 1.8 2.5 2.7 2.8 3.0 3.3 3.5 5.0 | 1.545 1.854 2.575 2.754 2.856 3.060 3.366 3.57 5.1 | V |
| Line Regulation 1.5 V–4.4 V ($V_{in} = V_{O(nom.)} + 1.0\text{ V}$ to 6.0 V) 4.5 V–5.0 V ($V_{in} = 5.5\text{ V}$ to 6.0 V) | Reg_{line} | – – | 10 10 | 20 20 | mV |
| Load Regulation ($I_{out} = 10\text{ mA}$ to 80 mA) | Reg_{load} | – | 20 | 40 | mV |
| Output Current ($V_{out} = (V_{out}$ at $I_{out} = 80\text{ mA}) - 3.0\%$) 1.5 V to 3.9 V ($V_{in} = V_{out(nom.)} + 2.0\text{ V}$) 4.0 V–5.0 V ($V_{in} = 6.0\text{ V}$) | $I_{O(nom.)}$ | 80 80 | 280 280 | – – | mA |
| Dropout Voltage ($T_A = -40^\circ\text{C}$ to 85°C , $I_{out} = 80\text{ mA}$, Measured at $V_{out} - 3.0\%$) 1.5 V–1.7 V 1.8 V–2.4 V 2.5 V–2.6 V 2.7 V–2.9 V 3.0 V–3.2 V 3.3 V–4.9 V 5.0 V | $V_{in} - V_{out}$ | – – – – – – – | 550 400 250 230 200 190 140 | 800 550 400 400 350 350 250 | mV |
| Quiescent Current (Enable Input = 0 V) (Enable Input = V_{in} , $I_{out} = 1.0\text{ mA}$ to $I_{O(nom.)}$) | I_Q | – – | 0.1 2.5 | 1.0 6.0 | μA |
| Output Short Circuit Current 1.5 V to 3.9 V ($V_{in} = V_{nom} + 2.0\text{ V}$) 4.0 V–5.0 V ($V_{in} = 6.0\text{ V}$) | $I_{out(max)}$ | 150 150 | 300 300 | 600 600 | mA |
| Output Voltage Noise ($f = 100\text{ Hz}$ to 100 kHz , $V_{out} = 3.0\text{ V}$) | V_n | – | 100 | – | μV_{rms} |
| Enable Input Threshold Voltage (NCP562 ONLY) (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $V_{th(en)}$ | 1.3 – | – – | – 0.3 | V |
| Output Voltage Temperature Coefficient | T_C | – | ± 100 | – | ppm/ $^\circ\text{C}$ |

3. Maximum package power dissipation limits must be observed.

$$PD = \frac{T_J(max) - T_A}{R_{\theta JA}}$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

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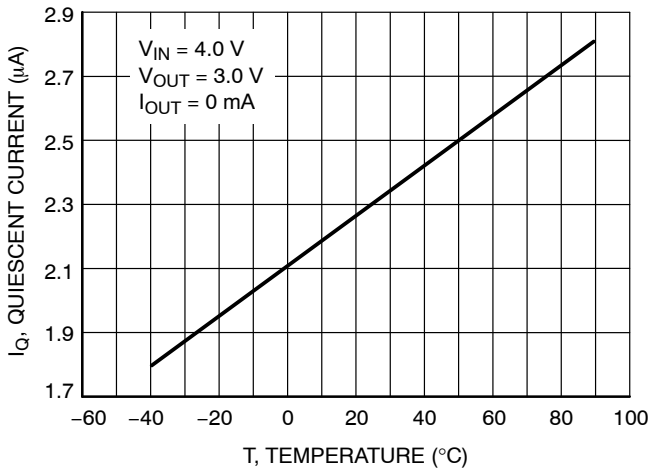


Figure 3. Quiescent Current versus Temperature

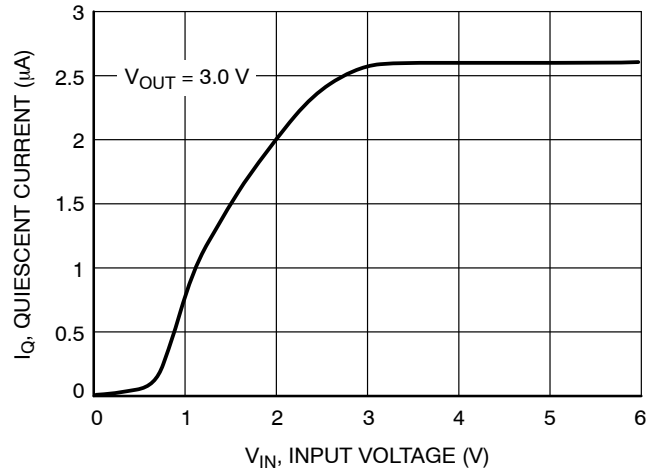


Figure 4. Quiescent Current versus Input Voltage

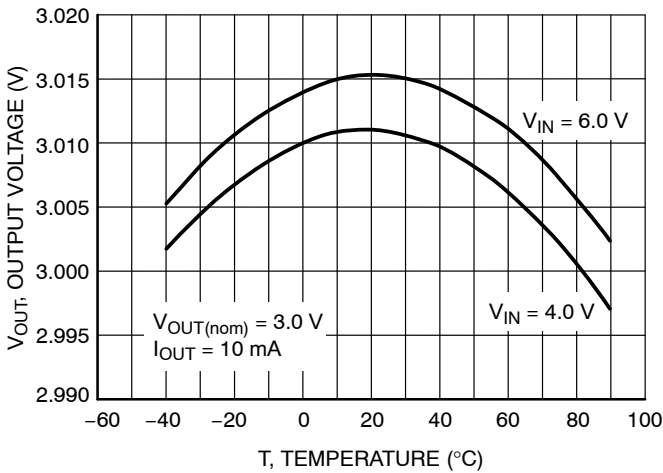


Figure 5. Output Voltage versus Temperature

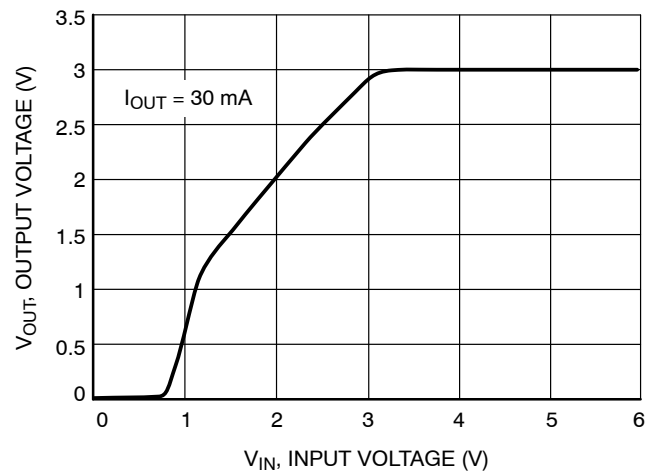


Figure 6. Output Voltage versus Input Voltage

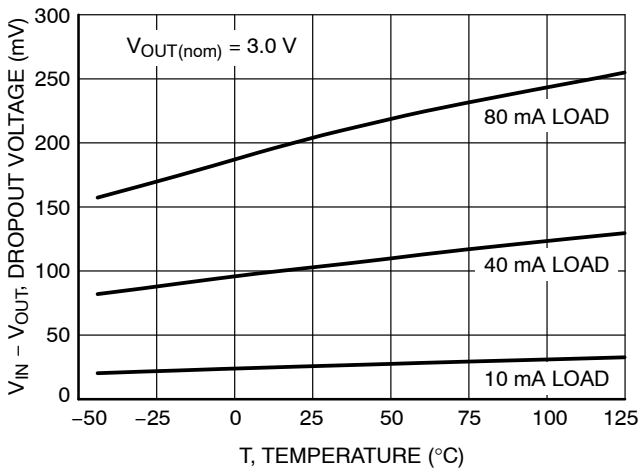


Figure 7. Dropout Voltage versus Temperature

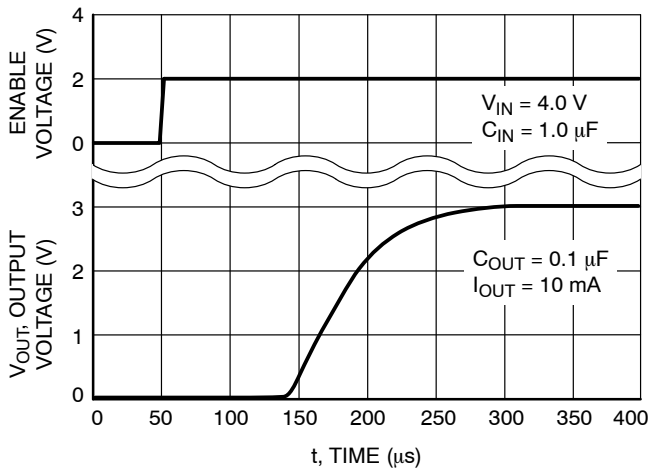


Figure 8. Turn-On Response (NCP562 ONLY)

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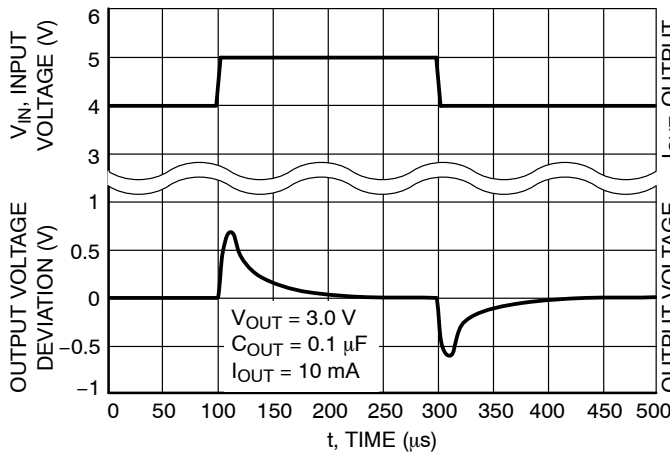


Figure 9. Line Transient Response

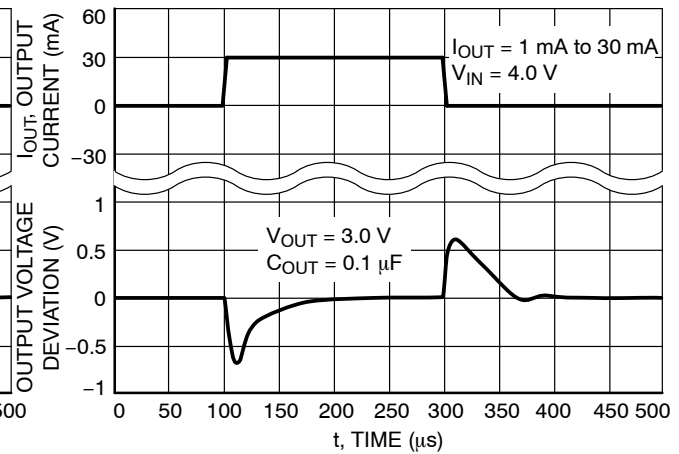


Figure 10. Load Transient Response

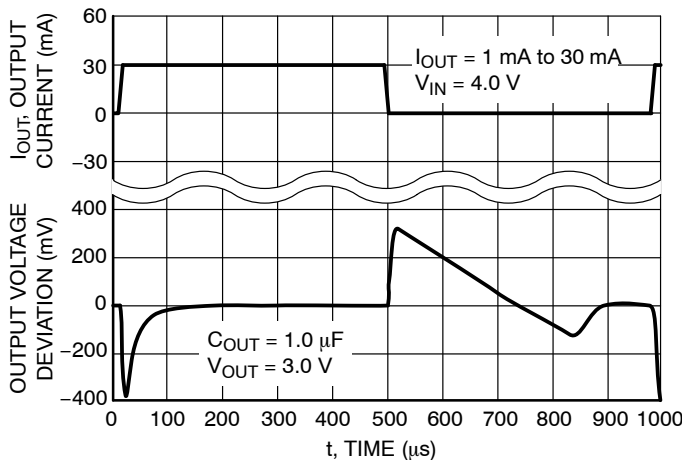


Figure 11. Load Transient Response

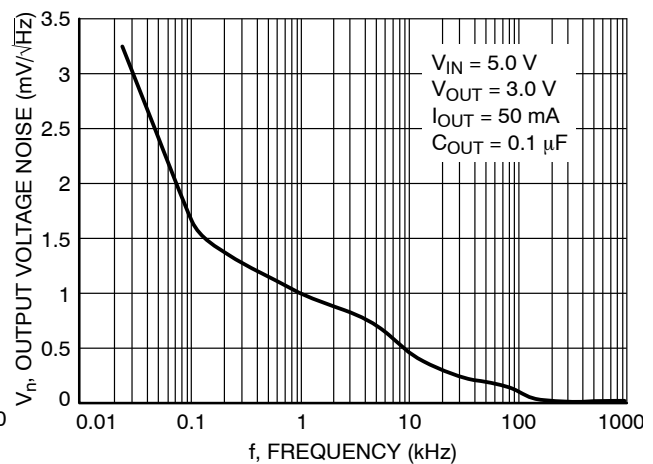


Figure 12. Output Voltage Noise

DEFINITIONS

Load Regulation

The change in output voltage for a change in output current at a constant temperature.

Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 3.0% below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 160°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125°C. Depending on the ambient power dissipation and thus the maximum available output current.

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APPLICATIONS INFORMATION

A typical application circuit for the NCP562 and NCP563 series are shown in Figure 1 and Figure 2.

Input Decoupling (C1)

A 1.0 μF capacitor either ceramic or tantalum is recommended and should be connected close to the NCP562 package. Higher values and lower ESR will improve the overall line transient response.

TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

Output Decoupling (C2)

The NCP562 and NCP563 are very stable regulators and do not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few $\text{m}\Omega$ up to $10\ \Omega$ can thus safely be used. The minimum decoupling value is $0.1\ \mu\text{F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

TDK capacitor: C2012X5R1C105K, C1608X5R1A105K, or C3216X7R1C105K

Enable Operation (NCP562 ONLY)

The enable pin will turn on the regulator when pulled high and turn off the regulator when pulled low. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used, then the pin should be connected to V_{in} .

Hints

Please be sure the V_{in} and GND lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Place external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

Thermal

As power across the NCP562 and NCP563 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the devices have good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$PD = \frac{T_{\text{J(max)}} - T_{\text{A}}}{R_{\theta\text{JA}}}$$

If junction temperature is not allowed above the maximum 125°C , then the NCP562 and NCP563 can dissipate up to $250\ \text{mW}$ @ 25°C .

The power dissipated by the NCP562 and NCP563 can be calculated from the following equation:

$$P_{\text{tot}} = [V_{\text{in}} * I_{\text{gnd}} (\text{lout})] + [V_{\text{in}} - V_{\text{out}}] * I_{\text{out}}$$

or

$$V_{\text{inMAX}} = \frac{P_{\text{tot}} + V_{\text{out}} * I_{\text{out}}}{I_{\text{gnd}} + I_{\text{out}}}$$

If an $80\ \text{mA}$ output current is needed then the ground current from the data sheet is $2.5\ \mu\text{A}$. For an NCP562 or NCP563 ($3.0\ \text{V}$), the maximum input voltage will then be $6.0\ \text{V}$.

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ORDERING INFORMATION

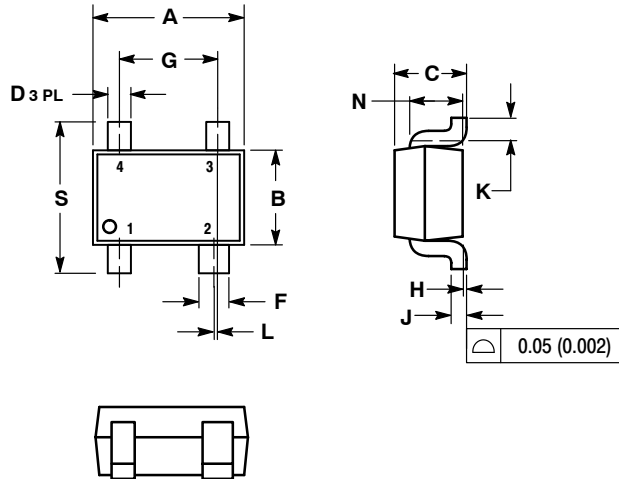
| Device | Nominal Output Voltage | Marking | Package | Shipping† |
|---------------|------------------------|---------|---------|--------------------|
| NCP562SQ15T1 | 1.5 | LDI | SC82-AB | 3000 / Tape & Reel |
| NCP562SQ15T1G | | | | |
| NCP562SQ18T1 | 1.8 | LEY | | |
| NCP562SQ18T1G | | | | |
| NCP562SQ25T1 | 2.5 | LDK | | |
| NCP562SQ25T1G | | | | |
| NCP562SQ27T1 | 2.7 | LEZ | | |
| NCP562SQ27T1G | | | | |
| NCP562SQ28T1 | 2.8 | LDL | | |
| NCP562SQ28T1G | | | | |
| NCP562SQ30T1 | 3.0 | LDM | | |
| NCP562SQ30T1G | | | | |
| NCP562SQ33T1 | 3.3 | LDN | | |
| NCP562SQ33T1G | | | | |
| NCP562SQ35T1G | 3.5 | LJU | | |
| NCP562SQ50T1 | 5.0 | LDP | | |
| NCP562SQ50T1G | | | | |
| NCP563SQ15T1 | 1.5 | LDQ | | |
| NCP563SQ15T1G | | | | |
| NCP563SQ18T1 | 1.8 | LFA | | |
| NCP563SQ18T1G | | | | |
| NCP563SQ25T1 | 2.5 | LDS | | |
| NCP563SQ25T1G | | | | |
| NCP563SQ27T1 | 2.7 | LFB | | |
| NCP563SQ27T1G | | | | |
| NCP563SQ28T1 | 2.8 | LDT | | |
| NCP563SQ28T1G | | | | |
| NCP563SQ30T1 | 3.0 | LDU | | |
| NCP563SQ30T1G | | | | |
| NCP563SQ33T1 | 3.3 | LDV | | |
| NCP563SQ33T1G | | | | |
| NCP563SQ50T1 | 5.0 | LDX | | |
| NCP563SQ50T1G | | | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

SC-82AB CASE 419C-02 ISSUE E

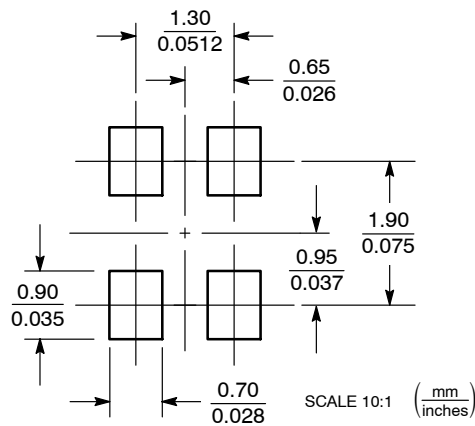


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. 419C-01 OBSOLETE. NEW STANDARD IS 419C-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.8 | 2.2 | 0.071 | 0.087 |
| B | 1.15 | 1.35 | 0.045 | 0.053 |
| C | 0.8 | 1.1 | 0.031 | 0.043 |
| D | 0.2 | 0.4 | 0.008 | 0.016 |
| F | 0.3 | 0.5 | 0.012 | 0.020 |
| G | 1.1 | 1.5 | 0.043 | 0.059 |
| H | 0.0 | 0.1 | 0.000 | 0.004 |
| J | 0.10 | 0.26 | 0.004 | 0.010 |
| K | 0.1 | --- | 0.004 | --- |
| L | 0.05 BSC | | 0.002 BSC | |
| N | 0.2 REF | | 0.008 REF | |
| S | 1.8 | 2.4 | 0.07 | 0.09 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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