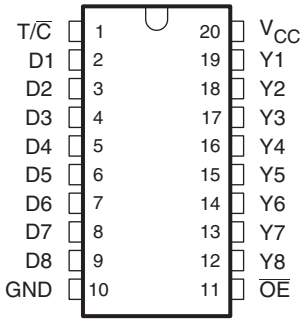
8-BIT INVERTING/NON-INVERTING SCHMITT-TRIGGER BUFFER WITH 3-STATE OUTPUTS

FEATURES

- **Operating Range of 2 V to 5.5 V V_{CC}**
- **8-Bit Inverting/Non-Inverting Outputs**
- **20-Pin Thin Shrink Small-Outline Package [TSSOP (PW)] and 20-Pin Plastic Dual-In-Line Package [PDIP (N)]**

N OR PW PACKAGE
(TOP VIEW)



DESCRIPTION

The SN74AHC8541 8-bit inverting/non-inverting buffers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

All outputs are in the high-impedance state (disabled) when the output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, the respective gate passes the data from the D input to its Y output.

The T/$\overline{C}$ input selects inverting or non-inverting data transfer. When the T/$\overline{C}$ input is high, it provides non-inverting buffers. When the T/$\overline{C}$ input is low, it provides inverting buffers when they are not in the high-impedance state.

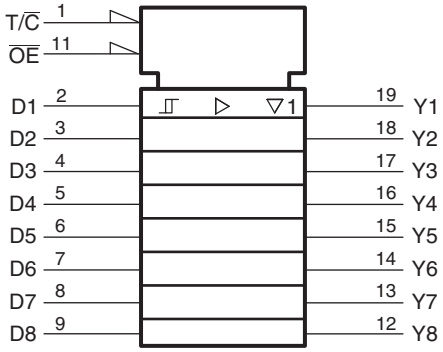
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(EACH BUFFER)(1)

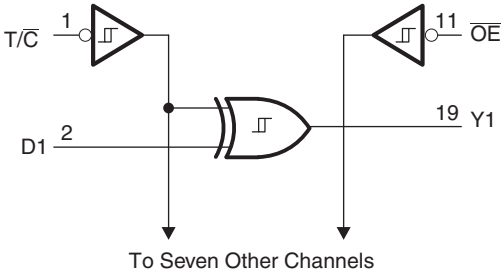
INPUTS			OUTPUT
$\overline{OE}$	T/$\overline{C}$	D	Y
L	H	H	H
L	H	L	L
L	L	H	L
L	L	L	H
H	X	X	Z

(1) L: Low-level
H: High-level
X: Irrelevant
Z: High-impedance (off)

LOGIC SYMBOL



LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impendance or power-off state(2)		–0.5	7	V
	Output voltage range applied in the high- or low-state(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0 V		–20	V
I_{OK}	Output clamp current	V_O < 0 V or VO > V_{CC}		±50	mA
I_O	Continuous output current	V_O = 0 V to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Thermal impedance(4)	N package		69	°C/W
		PW package		83	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.
(4) The package thermal impendance is calculatead in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			2	5.5	V
V_{IH}	High-level input voltage		V_{CC} = 2 V	1.5		V
			V_{CC} = 3.3 V ±0.3 V	V_{CC} × 0.7		
			V_{CC} = 5 V ±0.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage		V_{CC} = 2 V		0.5	V
			V_{CC} = 3.3 V ±0.3 V		V_{CC} × 0.3	
			V_{CC} = 5 V ±0.5 V		V_{CC} × 0.3	
V_I	Input voltage			0	5.5	V
V_O	Output voltage	High or low state		0	V_{CC}	V
		3-state		0	5.5	
I_{OH}	High-level output current		V_{CC} = 2 V		–50	μA
			V_{CC} = 3.3 V ±0.3 V		–6	mA
			V_{CC} = 5 V ±0.5 V		–12	
I_{OL}	Low-level output current		V_{CC} = 2 V		50	μA
			V_{CC} = 3.3 V ±0.3 V		6	mA
			V_{CC} = 5 V ±0.5 V		12	
Δt/ΔV	Input transition rise or fall rate	T/$\overline{C}$, $\overline{OE}$	V_{CC} = 3.3 V ±0.3 V	0	100	ns/V
			V_{CC} = 5 V ±0.5 V	0	20	
		D	V_{CC} = 3.3 V ±0.3 V	0	3	ms/V
			V_{CC} = 5 V ±0.5 V	0	2	
t_{pa}	Pulse reception time(2)		V_{CC} = 3.3 V ±0.3 V	100		ns
			V_{CC} = 5 V ±0.5 V	60		
T_A	Operating free-air temperature			–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Buffer inputs D1 to D8 might accept no pulse after t_{pa} period after receiving the first pulse edge. If the input state changes from H to L or L to H in this period, the corresponding output changes from L to H or H to L respectively, in t_{pa} + t_{pd} as delay time in worst-case scenario.
Maximum input frequency, f_{max}, is calculated by the following formula:
f_{max} = input pulse duty cycle/($t_{pa(min)}$ + $t_{pd(max)}$) when input pulse duty cycle <50%
f_{max} = (1 – input pulse duty cycle)/($t_{pa(min)}$ + $t_{pd(max)}$) when input pulse duty cycle >50%

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	D	3.3 V			2.31	V
			5 V			3.5	
V_{T-}	Negative-going input threshold voltage	D	3.3 V	0.99			V
			5 V	1.5			
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	D	3.3 V	0.33		1.32	V
			5 V	0.5		2	
V_{OH}	High-level output voltage	I_{OH} = –50 µA	2 V	1.9			V
		I_{OH} = –6 µA	3 V	2.48			
		I_{OH} = –12 µA	4.5 V	3.8			
V_{OL}	Low-level output voltage	I_{OL} = 50 µA	2 V			0.1	V
		I_{OL} = 6 µA	3 V			0.44	
		I_{OL} = 12 µA	4.5 V			0.55	
I_I	Input current	V_I = 5.5 V or GND	0 V to 5.5 V			±1	µA
I_{OZ}	OFF-state output current	$V_O = V_{CC}$ or GND	5.5 V			±5	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND, IO = 0 A	5.5 V			20	µA
C_I	Input capacitance	$V_I = V_{CC}$ or GND	5 V		3		pF
C_O	Output capacitance	$V_O = V_{CC}$ or GND	5 V		5		pF
C_{pd}	Power disspation capacitance	f = 1 MHz, no load	5 V		15		pF

(1) All typical values are at T_A = 25°C.

SWITCHING CHARACTERISTICS

V_{CC} = 3.3 V ±0.3 V, T_A = –40°C to 85°C, see Figure 1

PARAMETER		FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time	D	Y	C_L = 15 pF	1	15	29	ns
				C_L = 50 pF	1	18	34	
		T/$\overline{C}$		C_L = 15 pF	1	16	30	
				C_L = 50 pF	1	20	36	
t_{en}	Enable time	$\overline{OE}$	Y	C_L = 15 pF	1	9	16	ns
				C_L = 50 pF	1	11	20	
t_{dis}	Disable time	$\overline{OE}$	Y	C_L = 15 pF	1	8	14	ns
				C_L = 50 pF	1	11	18	

SWITCHING CHARACTERISTICS

V_{CC} = 5 V ±0.5 V, T_A = –40°C to 85°C, see Figure 1

PARAMETER		FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time	D	Y	C_L = 15 pF	1	10	16	ns
				C_L = 50 pF	1	12	20	
		T/$\overline{C}$		C_L = 15 pF	1	11	17	
				C_L = 50 pF	1	13	21	
t_{en}	Enable time	$\overline{OE}$	Y	C_L = 15 pF	1	6	10.5	ns
				C_L = 50 pF	1	8	12.5	
t_{dis}	Disable time	$\overline{OE}$	Y	C_L = 15 pF	1	6	10	ns
				C_L = 50 pF	1	8	11.5	

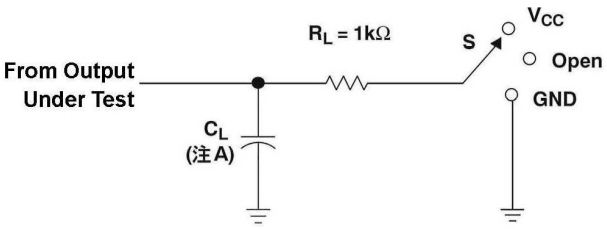
NOISE CHARACTERISTICS(1)

V_{CC} = 5 V, C_L = 50 pF, T_A = –40°C to 85°C

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.5		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low--level dynamic input voltage			1.5	V

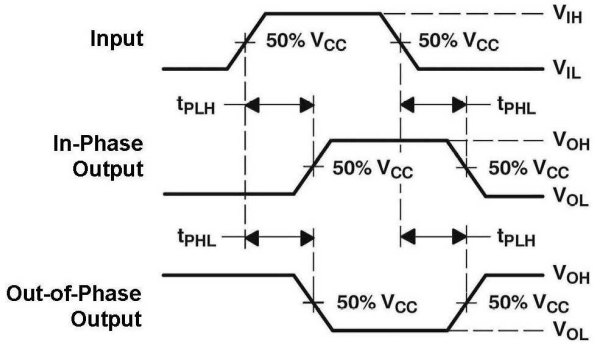
(1) Characteristics are for surface-mount packages only.

PARAMETER MEASUREMENT INFORMATION

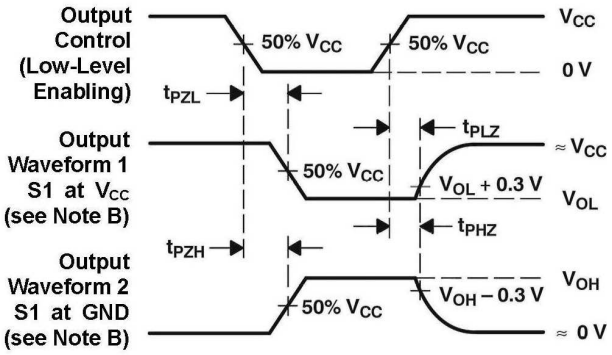


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, tr ≤ 3 ns, t_f ≤3 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PZL} and t_{PZH} are the same as t_{en}.

F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC8541N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC8541N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

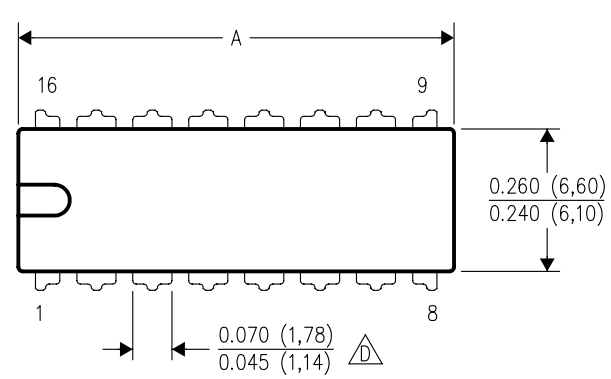
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

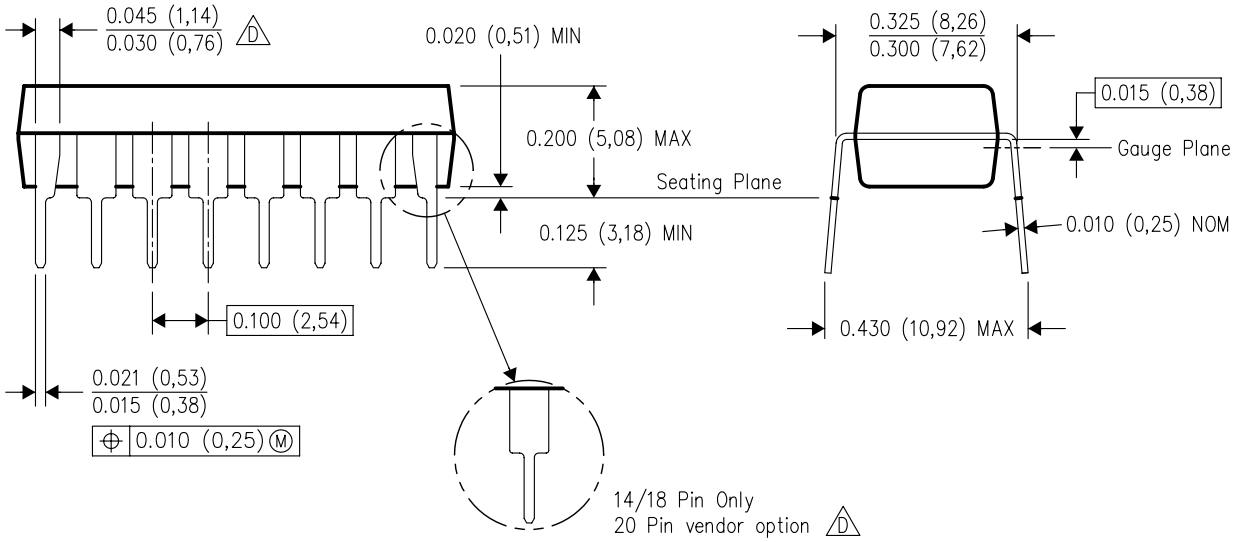
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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