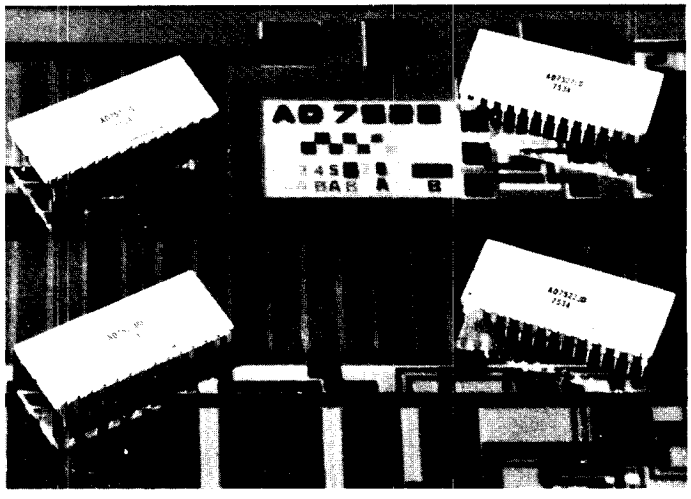
ANALOG DEVICES

CMOS 10-Bit, Buffered Multiplying D/A Converter

AD7522

FEATURES

- 10-Bit Resolution
- 8, 9, & 10-Bit Linearity
- Microprocessor Compatible
- Double Buffered Inputs
- Serial or Parallel Loading
- DTL/TTL/CMOS Direct Interface
- Nonlinearity Tempco: 2ppm of FSR/°C
- Gain Tempco: 10ppm of FSR/°C
- Very Low Power Dissipation
- Very Low Feedthrough



GENERAL DESCRIPTION

The AD7522 is a monolithic CMOS 10-bit multiplying D/A converter, with an input buffer and a holding register, allowing direct interface with microprocessors. Most applications require the addition of only an operational amplifier and a reference voltage.

The key to easy interface to a data bus is the AD7522's ability to load the input buffer in two bytes (an 8-bit and a 2-bit byte), and subsequently move this data to a holding register, where the digital word is converted into an analog current or voltage (with external operational amplifier). The input loading of either 8 or 10 bits can be done in a parallel or serial mode.

The AD7522 is packaged in a 28-pin DIP, and operates with a +15V main supply at 2mA max, and a logic supply of +5V for TTL interface, or +10 to +15V for CMOS interface.

A thin film on high density CMOS process, using silicon nitride passivation, ensures high reliability and excellent stability.

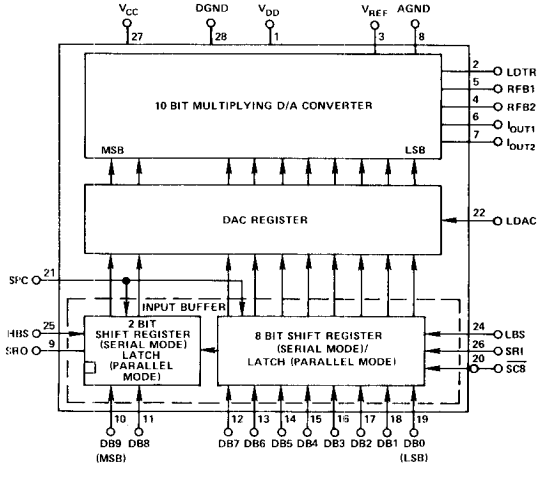
ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0 to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7522JN	AD7522JD	AD7522SD
0.1% (9-Bit)	AD7522KN	AD7522KD	AD7522TD
0.05% (10-Bit)	AD7522LN	AD7522LD	AD7522UD

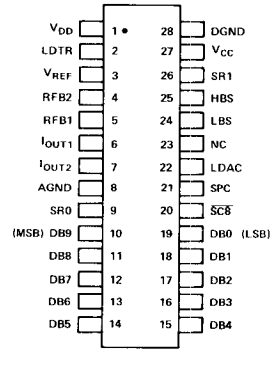
PACKAGE IDENTIFICATION

Suffix "D": Ceramic DIP Package
Suffix "N": Plastic DIP Package

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15V, V_{CC} = +5V, V_{REF} = ±10V, TA = +25°C unless otherwise noted)

PARAMETER		TA = +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
STATIC ACCURACY				
Resolution	All	10 Bits min	10 Bits min	$\overline{SC8}$ = "1"
Nonlinearity	AD7522J	±0.2% FSR max		
	AD7522S	±0.2% FSR max	±0.2% FSR max	
	AD7522K	±0.1% FSR max		
	AD7522T	±0.1% FSR max	±0.1% FSR max	
	AD7522L	±0.05% FSR max		
	AD7522U	±0.05% FSR max	±0.05% FSR max	$-10V \leqslant V_{REF} \leqslant +10V$
Nonlinearity Tempco[1]	AD7522J,K,L	±1ppm FSR/°C typ	±2ppm FSR/°C max	
	AD7522S,T,U		±2ppm FSR/°C max	
Gain Error	AD7522J,K,L	±0.3% Reading typ		
Gain Error Tempco[1]	AD7522J,K,L	±5ppm of Reading/°C typ	±10ppm of Reading/°C max	
	AD7522S,T,U		±10ppm of Reading/°C max	
Output Leakage Current at I_{OUT1} or I_{OUT2}	All		200nA max	I_{OUT1}: DB0 through DB9 = 0 I_{OUT2}: DB0 through DB9 = 1
Power Supply Rejection	AD7522J,K,L	50ppm of Reading/% typ		
AC ACCURACY				
Feedthrough Error[1]	All	1mV p-p typ, 10mV p-p max		V_{REF} = 20V p-p; 10kHz
Output Current Settling Time	AD7522J,K,L	500ns typ		To 0.05% of FSR for a FSR Step. HBS and LBS Low to High LDAC = 1
REFERENCE INPUT				
Input Resistance	All	5kΩ min	20kΩ max	
ANALOG OUTPUT				
Output Capacitance				
C_{OUT1}	AD7522J,K,L	120pF typ		All Data Input High
C_{OUT2}	AD7522J,K,L	40pF typ		All Data Input High
C_{OUT1}	AD7522J,K,L	40pF typ		All Data Inputs Low
C_{OUT2}	AD7522J,K,L	120pF typ		All Data Inputs Low
DIGITAL INPUTS				
Low State Threshold	All	0.8V max	0.8V max	V_{CC} = +5V
	All	1.5V max	1.5V max	V_{CC} = +15V
High State Threshold	All	2.4V min	2.4V min	V_{CC} = +5V
	All	13.5V min	13.5V min	V_{CC} = +15V
Input Current	AD7522J,K,L	1μA typ		
LDAC Pulse Width[1]	All	500ns min	500ns min	LDAC: 0 to +3V
HBS, LBS Pulse Width[1]	All	500ns min	500ns min	HBS, LBS: 0 to +3V
Serial Clock Frequency[1]	All	1MHz max	1MHz max	
HBS, LBS Data Set Up[2]	All	250ns min	250ns min	
Data Hold Time[3]	All	500ns min, 200ns typ	500ns min	
POWER REQUIREMENTS				
I_{DD}	All	2mA max		In Quiescent State
I_{CC}	All	2mA max		In Quiescent State

Notes

[1] Guaranteed by design. Not tested.
[2] Data setup time is the minimum amount of time required for DB0 - DB9 to be stable prior to strobing HBS, LBS.
[3] Data hold time is the minimum amount of time required for DB0 - DB9 to be stable after strobing HBS, LBS.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{REF} to GND . . . . . ±25V
V_{DD} to GND . . . . . +17V
V_{CC} to GND . . . . . +17V
V_{CC} to V_{DD} . . . . . +0.4V
I_{OUT1}, I_{OUT2} . . . . . ±5mA
Operating Temperature
JN, KN, LN versions . . . . . 0 to +70°C
JD, KD, LD versions . . . . . -25°C to +85°C
SD, TD, UD versions . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Power Dissipation (Package)
Up to +50°C:
Plastic (Suffix N) 1200mW
Ceramic (Suffix D) 1000mW
Derate Above +50°C by
Plastic (Suffix N) . . . . . 12mW/°C
Ceramic (Suffix D) . . . . . 10mW/°C
Digital Input Voltage Range . . . . . V_{DD} to GND

CAUTION:

1. Do not apply voltages higher than V_{CC} to SRO.
2. Do not apply voltages higher than V_{DD} or less than GND to any other input/output terminal except V_{REF}, R_{FB1} or R_{FB2}.
3. The digital control inputs are zener protected, however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
4. V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing.

TERMINOLOGY

RESOLUTION

Value of the LSB. For example, a unipolar n-bit converter has a resolution of (2^{-n}) (V_{REF}). A bipolar n-bit converter has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

NONLINEARITY

Error contributed by deviation of the DAC transfer function from a best straight line function. For a multiplying DAC, the nonlinearity should be independent of the sign or magnitude of V_{REF}. Nonlinearity is normally expressed as a percentage of full scale range (% FSR).

GAIN

The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10V full scale. It is a linear error which can be externally adjusted (see gain adjustment on next page).

OUTPUT LEAKAGE CURRENT

Current which appears on the OUT1 terminal when the DAC register is loaded with all "0's" or on the OUT2 terminal when the DAC register is loaded with all "1's."

DAC CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7522's DAC functional block consists of a highly stable Silicon Chromium thin film R-2R ladder, and ten SPDT N-channel current steering switches. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used — that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

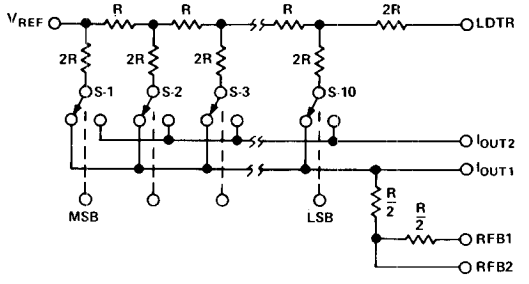


Figure 1. DAC Functional Diagram

EQUIVALENT CIRCUIT

The DAC equivalent circuit is shown in Figure 2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the $I_{REF}/1024$ current source represents the 1LSB of current lost through the ladder termination resistor to ground. The C_{OUT1} and C_{OUT2} output capacitances are as shown when the DAC latches feed the DAC with all "1's." If the DAC latches are loaded with all "0's," C_{OUT1} is 37pF, while C_{OUT2} is 120pF. In addition, C_{SD} is shunted by 10 ohms, and the 10 ohm R_{ON} in I_{OUT1} is replaced by a C_{SD} of 10pF. When fast amplifiers are used, it will be necessary to provide phase compensation (in the form of feedback capacitance) to cancel the pole formed by $R_{FEEDBACK}$ and C_{OUT} if stability is to be maintained.

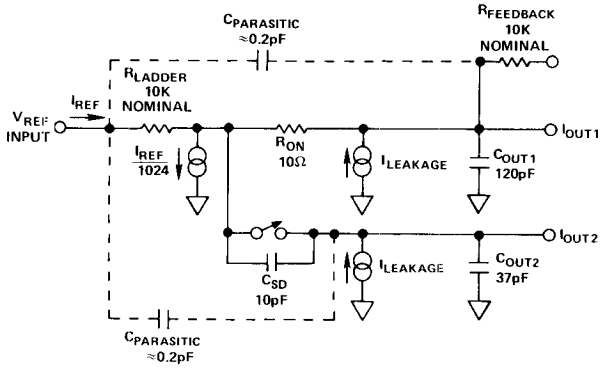


Figure 2. Equivalent Circuit (Shown for all Digital Inputs High)

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	V_{DD}	+15V (nominal) Main Supply.
2	LDTR	R-2R Ladder Termination Resistor. Normally grounded for unipolar operation or terminated at I_{OUT2} for bipolar operation.
3	V_{REF}	Reference Voltage Input. Since the AD7522 is a multiplying DAC, V_{REF} may vary over the range of ±10V.
4	RFB2	$R_{FEEDBACK} \div 2$; gives full scale equal to $V_{REF}/2$.
5	RFB1	$R_{FEEDBACK}$, used for normal unity gain (at full scale) D/A conversion.
6	I_{OUT1}	DAC Current OUT1 Bus. Normally terminated at virtual ground of output amplifier.
7	I_{OUT2}	DAC Current OUT2 Bus, terminated at ground for unipolar operation, or virtual ground of op amp for bipolar operation.
8	AGND	Analog Ground. Back gate of DAC N-channel SPDT current steering switches.
9	SRO	Serial Output. An auxiliary output for recovering data in the input buffer.
10	DB9	Data Bit 9. Most significant parallel data input.
11	DB8	Data Bit 8.
12	DB7	Data Bit 7.
13	DB6	Data Bit 6.
14	DB5	Data Bit 5.
15	DB4	Data Bit 4.
16	DB3	Data Bit 3.
17	DB2	Data Bit 2.
18	DB1	Data Bit 1.
19	DB0	Data Bit 0. Least significant parallel data input.
20	$\overline{SC8}$	8-Bit Short Cycle Control. When in serial mode, if $\overline{SC8}$ is held to Logic "0", the two least significant input latches in the input buffer are bypassed to provide proper serial loading of 8-bit serial words. If $\overline{SC8}$ is held to Logic "1", the AD7522 will accept a 10-bit serial word. Data bits 0 (LSB) and DB1 are in a parallel load mode when $\overline{SC8}$ = 0 and should be tied to a logic low state to prevent false data from being loaded.
21	SPC	Serial/Parallel Control. If SPC is a Logic "0", the AD7522 will load parallel data appearing on DB0 through DB9 into the input buffer when the appropriate strobe inputs are exercised (see HBS and LBS). If SPC is a Logic "1", the AD7522 will load serial data appearing on Pin 26 into the input buffers. Each serial data bit must be "strobed" into the buffer with the HBS and LBS.
22	LDAC	Load DAC: When LDAC is a Logic "0", the AD7522 is in the "hold" mode, and digital activity in the input buffer is locked out. When LDAC is a Logic "1", the AD7522 is in the "load" mode, and data in the input buffer loads the DAC register.
23	NC	No Connection.
24	LBS	Low Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB0 (LSB) through DB7 inputs will be "clocked" into the input buffer on the positive going edge of the LBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edge of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
25	HBS	High Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB9 (MSB) and DB8 data inputs will be "clocked" into the input buffer on the positive going edge of HBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edges of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
26	SRI	Serial Input.
27	V_{CC}	Logic Supply. If +5V is applied, all digital inputs/outputs are TTL compatible. If +10V to +15V is applied, digital inputs/outputs are CMOS compatible.
28	DGND	Digital Ground

Note 1: Logic "1" applied to a data bit steers that bit's current to the $I_{OUT}1$ terminal.

APPLICATIONS

UNIPOLAR OPERATION

Figure 3 shows the analog circuit connections required for unipolar operation. The input code/output voltage relationship is shown in Table 1.

Zero Offset Adjustment

1. Adjust the op amp's offset potentiometer for <1mV on the amplifier junction. (Each millivolt of amplifier V_{OS} causes ±0.66mV of differential nonlinearity which adds to the ladder nonlinearity.)

Gain Adjustment

1. Set R1 and R2 to 0Ω. Load the DAC register with all "1's."
2. If analog out is greater than $-V_{REF}$, increase R1 for required full scale output. If analog out is less than $-V_{REF}$, increase R2 for required full scale output.

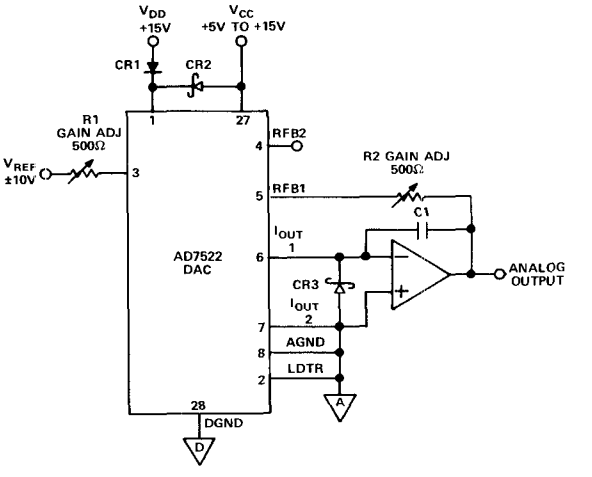


Figure 3. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1 - 2^{-10})$
1000000001	$-V_{REF}(1/2 + 2^{-10})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF}(1/2 - 2^{-10})$
0000000001	$-V_{REF}(2^{-10})$
0000000000	0

Table 1. Unipolar Code Table

BIPOLAR OPERATION

Figure 4 shows the analog circuit connections required for bipolar operation. The input code/output voltage relationship is shown in Table 2.

Zero Offset Adjustment

1. Adjust the offset potentiometer of amplifier A1 and A2 for <1mV on the respective summing junctions. If the analog out for code 1000000000 is not zero, sum current into or out of the summing junction of A1 for 0V at analog out.

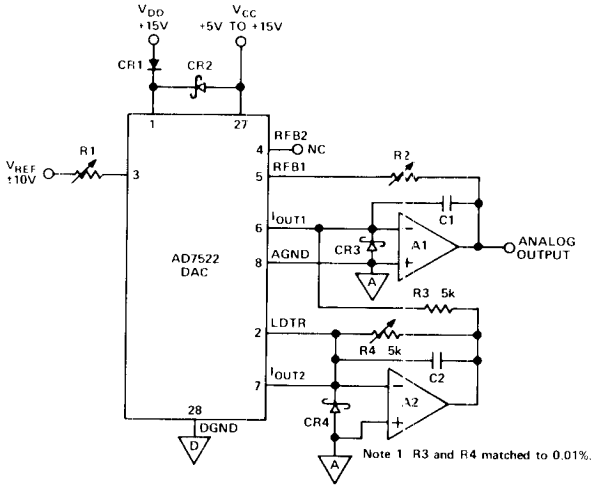


Figure 4. Bipolar Operation

Gain Adjustment

1. Load the DAC register with all "0's." Set R1 and R2 to 0Ω.
2. If analog out is greater than $+V_{REF}$, increase R2 until it reads precisely $+V_{REF}$. If analog out is less than $+V_{REF}$, increase R1 until it reads precisely V_{REF}.

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1 - 2^{-9})$
1000000001	$-V_{REF}(2^{-9})$
1000000000	0
0111111111	$V_{REF}(2^{-9})$
0000000001	$V_{REF}(1 - 2^{-9})$
0000000000	V_{REF}

Table 2. Bipolar Code Table

SINGLE BYTE PARALLEL LOADING

Figure 5 illustrates the logic connections for loading single byte parallel data into the input buffer. DB0 should be grounded on "K" and "T" versions, and DB0 and DB1 should be grounded on "J" and "S" versions for monotonic operation of the DAC. DB9 is always the MSB, whether 8-bit, 9-bit, or 10-bit linear AD7522's are used.

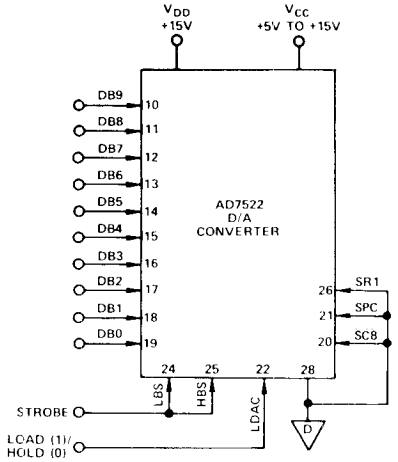


Figure 5. Single Byte Parallel Loading

When data is stable on the parallel inputs (DB0-DB9), it can be transferred into the input buffer on the positive edge of the strobe pulse.

Data is transferred from the input buffer to the DAC register when LDAC is a Logic "1." LDAC is a level-actuated (versus edge-triggered) function and must be held "high" at least 0.5μs for data transfer to occur.

TWO BYTE PARALLEL LOADING

Figures 6 and 7 show the logic connections and timing requirements for interfacing the AD7522 to an 8-bit data bus for two byte loading of a 10-bit word.

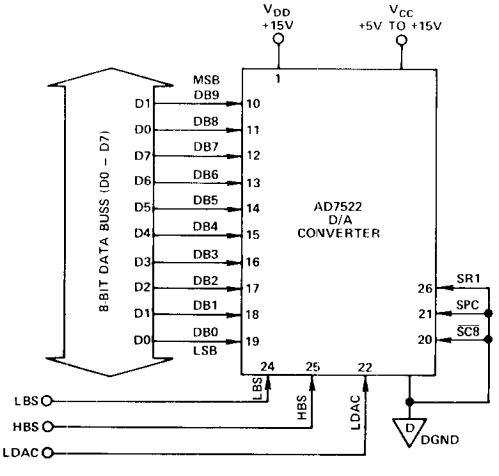


Figure 6. Two Byte Parallel Loading

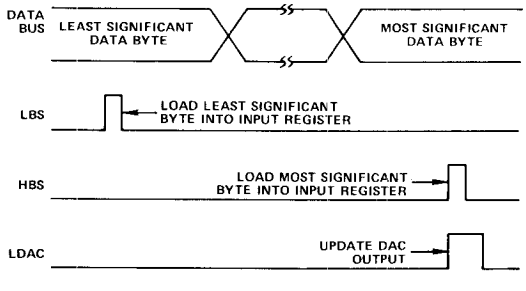


Figure 7. Timing Diagram

First, the least significant data byte (DB0 through DB7) is loaded into the input buffer on the positive edge of LBS. Subsequently, the data bus is used for status indication and

instruction fetching by the CPU. When the most significant data byte (DB8 and DB9) is available on the bus, the input buffer is loaded on the positive edge of HBS. The DAC register updates to the new 10-bit word when LDAC is "high." LDAC may be exercised coincident with, or at any time after HBS loads the second byte of data into the input buffer.

SERIAL LOADING

Figure 8 and Figure 9 show the connections and timing diagram for serial loading.

To load a 10-bit word ($\overline{SC8}$ = 1), HBS and LBS must be strobed simultaneously with exactly 10 positive edges to clock the serial data into the input buffer. For 8-bit words ($\overline{SC8}$ = 0), only 8 positive edges are required.

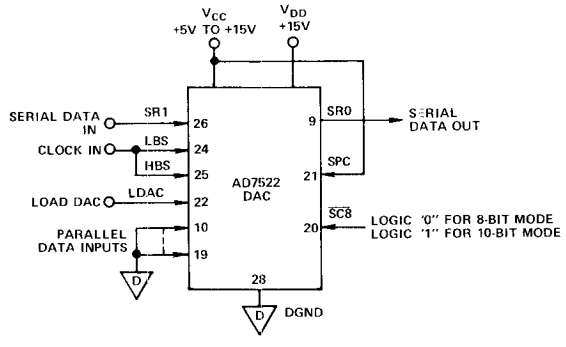


Figure 8. Serial 8- and 10-Bit Loading (Analog Outputs Not Shown for Clarity)

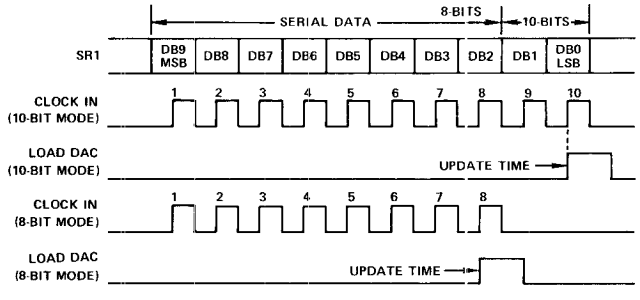


Figure 9. Timing Diagram for Serial 8- and 10-Bit Loading

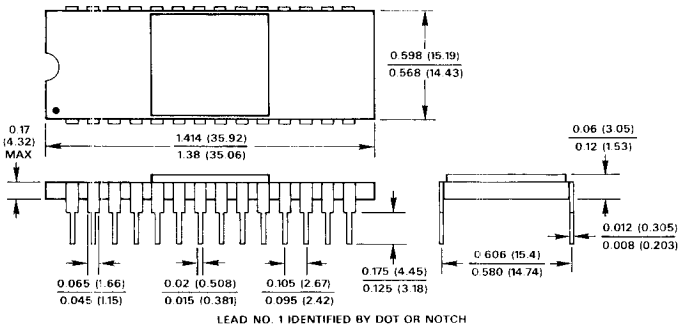
APPLICATION HINTS

1. CR1 and CR2 on Figures 3 and 4 protect the AD7522 against latch-up V_{CC} exceeds V_{DD}, and may be omitted if V_{DD} and V_{CC} are driven from the same voltage.
2. Diodes CR3 on Figure 3 and CR3 and CR4 on Figure 4 clamp the amplifier junction to -300mV if they attempt to swing negative during power up or power down. The input structures of some high-speed op amps can supply substantial current under the transient conditions encountered during power sequencing. It is recommended that the PC layout be able to accommodate the diodes.
3. Fast op amps will require phase compensation for stability due to the pole formed by C_{OUT1} or C_{OUT2} and $R_{FEEDBACK}$.
4. During serial loading, all data inputs (DB0 through BD9), should be grounded.

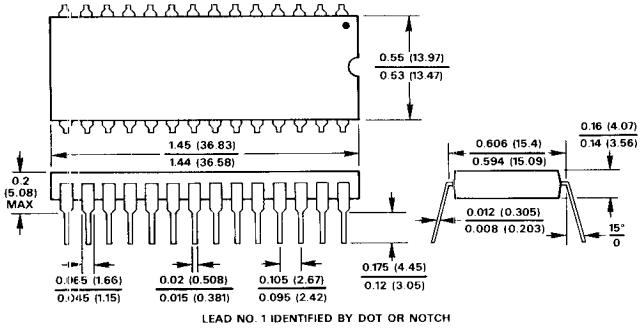
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28 PIN CERAMIC DIP



28 PIN PLASTIC DIP



BONDING DIAGRAM