ANALOG DEVICES

High Speed Analog to Digital Converter

FEATURES
High Speed: 10 Bits in 4μs Max
Error Relative to Full Scale: ±½LSB
User Choice of Unipolar or Bipolar Input
Small 2" x 3" x 0.4" Module

GENERAL DESCRIPTION

The ADC1109 is a high speed analog-to-digital converter packaged in a compact 2" x 3" x 0.4" module. It uses the successive approximations technique to perform complete 10 bit conversion in less than 4μs with ±½LSB relative accuracy.

The ADC1109 can be configured by the user to accept either unipolar or bipolar input signals and to produce Binary, Offset Binary, or Two's Complement coded outputs. The data outputs are fully DTL/TTL compatible and are available in both parallel and serial form.

TIMING

As shown in Figure 1, the "0" to "1" transition of the CONVERT COMMAND input sets the MSB output to Logic "0" and the STATUS, MSB, and BIT 2 through BIT 10 outputs to Logic "1". Nothing further happens until the CONVERT COMMAND returns to Logic "0", at which time the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 10 (LSB) comparison is completed. At this time the STATUS output returns to Logic ' 0" and the conversion cycle ends.

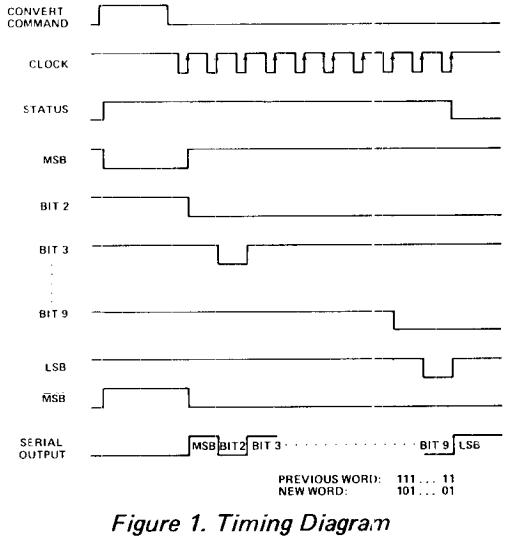


Figure 1. Timing Diagram

The SERIAL DATA output is of the non-return-to-zero (NRZ) type. The data is available, MSB first, 40ns after each of the ten "0" to "1" clock transitions.

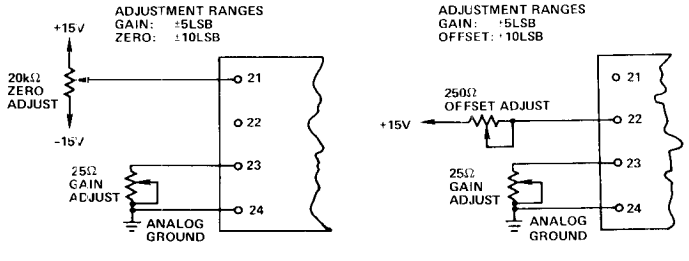
ZERO AND OFFSET CALIBRATION

For unipolar units set the input voltage precisely to +0.0049V and adjust the 20kΩ zero potentiometer until the converter is just on the verge of switching from 0000000000 to 0000000001.

For bipolar units set the input voltage precisely to -4.9951V and adjust the 250Ω variable offset resistor until Offset Binary coded units are just on the verge of switching from 0000000000 to 0000000001, and Two's Complement coded units are just on the verge of switching from 1000000000 to 1000000001.

GAIN CALIBRATION

Set the input voltage precisely to +9.9853 for unipolar units or +4.9853V for bipolar units. Note that these values are 1½LSB's less than nominal full scale. Adjust the 25Ω variable gain resistor until binary and offset binary coded units are just on the verge of switching from 1111111110 to 1111111111 and Two's Complement coded units are just on the verge of switching from 0111111110 to 0111111111.



UNIPOLAR **BIPOLAR**

ADJUSTMENT CONNECTIONS

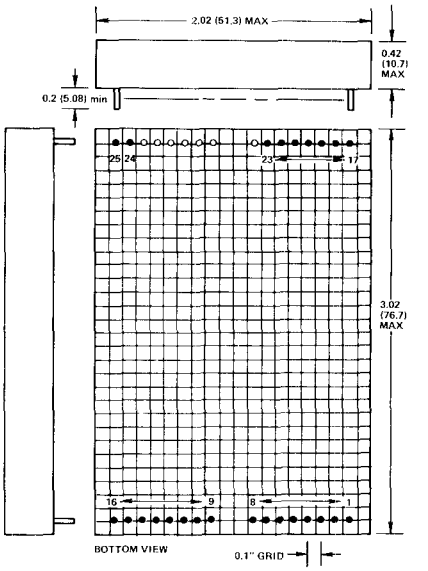
SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

MODEL	ADC1109
RESOLUTION	10 Bits
CONVERSION TIME[1]	3.8μs (4μs max)
ACCURACY[2]	
Error Relative to Full Scale	±½LSB
Quantization Error	±½LSB
Differential Nonlinearity Error	±½LSB
TEMPERATURE COEFFICIENTS	
Gain	±30ppm/°C of Reading (±50ppm/°C max)
Zero (Unipolar Inputs)	±200μV/°C (±500μV/°C max)
Offset (Bipolar Inputs)	±200μV/°C (±500μV/°C max)
Differential Nonlinearity	±7ppm/°C (±1.ppm/°C max)
INPUT VOLTAGE RANGES	±5V, 0 to +10V
INPUT IMPEDANCE	10kΩ
CONVERT COMMAND	Positive Pulse, TTL Compatible, 100ns min Width
PARALLEL DATA OUTPUT	
Unipolar Inputs	Positive True Binary
Bipolar Inputs	Positive True Offset Binary or Two's Complement
SERIAL DATA OUTPUT	
Unipolar Inputs	Positive True Binary
Bipolar Inputs	Positive True Offset Binary TTL Compatible, NRZ Format, MSB First
STATUS OUTPUT	Logic "1" During Conversion, TTL Compatible
CLOCK OUTPUT	TTL Compatible, 190ns Width
LOGIC FANOUTS AND LOADING	
Convert Command	1TTL Load
Parallel Data Outputs	5TTL Loads/Bit
Status Output	8TTL Loads
Serial Data Output	6TTL Loads
Clock Output	10TTL Loads
ADJUSTMENT RANGES	
Gain	±5LSB
Zero	±10LSB
Offset	±10LSB
POWER REQUIREMENTS	+5V dc ±5% @ 25mA (135mA, max) +15V dc ±3% @ 35mA (40mA, max)[3] −15V dc ±3% @ 35mA (40mA, max)
POWER SUPPLY SENSITIVITY	
Gain (to +15V Supply)	±7.5mV/V (±15mV/V, max)
Zero (to +15V Supply)	±15mV/V (±20mV/V, max)
(to −15V Supply)	±5mV/V (±10mV/V, max)
Offset (to +15V Supply)	±400mV/V (±500mV/V, max)
(to −15V Supply)	±5mV/V (±10mV/V, max)
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	−55°C to +85°C

[1] Conversion time is measured from trailing edge of the convert command to "1" to "0" transition of status output.
[2] Warmup time to rated accuracy is 5 minutes.
[3] Values shown are for the unipolar mode; values for the bipolar mode are 45mA (50mA, max).
Specifications subject to change without notice.

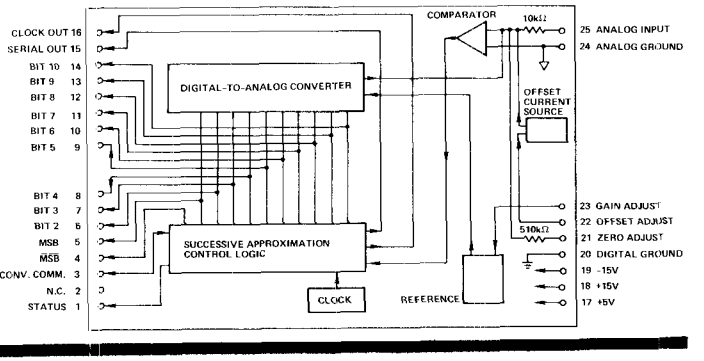
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Pins are installed only in shaded hole locations.
Pins are half hard brass, gold plated per MIL-G-45204B, Class I, Type II.
Pin Diameter is 0.019" (0.483mm) ±0.001" (0.025mm).
For plug-in mounting card 4.000" (101.6mm) x 4.500" (114.3mm), order Board No. AC-1520

BLOCK DIAGRAM AND PIN DESIGNATIONS



ANALOG INPUT	DIGITAL OUTPUT BINARY CODE
+9.9902V	1111111111
+5.0000V	1000000000
+1.2500V	0010000000
+0.0098V	0000000001
+0.0000V	0000000000

Table I. Nominal Unipolar Input-Output Relationships

ANALOG INPUT	DIGITAL OUTPUT	
	OFFSET BINARY	TWO'S COMPLEMENT
+4.9902	1111111111	0111111111
+2.5000	1100000000	0100000000
0.0000	1000000000	0000000000
−2.5000	0100000000	1100000000
−5.0000	0000000000	1000000000

Table II. Nominal Bipolar Input-Output Relationships

SERIAL DATA OUTPUT

The serial data output, available on pin 15, is of the non-return-to-zero format. The data is transmitted MSB first and is Binary coded for unipolar units and Offset Binary coded for bipolar units.

Figure 3, shown below, indicates one method for transmitting data serially using only three wires (plus a digital ground). The data is clocked into a receiving shift register using the delayed clock output of the ADC1109.

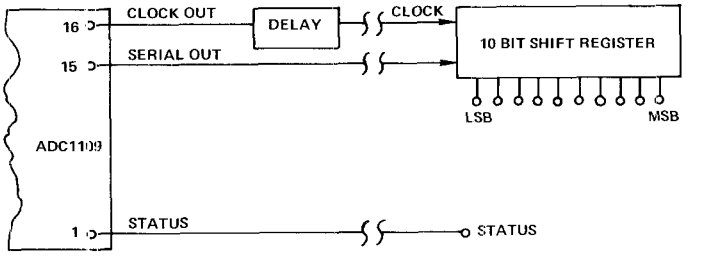


Figure 3. Serial Data Transmission