ANALOG DEVICES

Dual Slope Integrating ADC

ADC-141

FEATURES
- Excellent Stability
- 14 Binary Bits Plus Sign
- 4½BCD Digits Plus Sign
- 0.01% Accuracy
- Automatic Error Correction
- High Noise Rejection

APPLICATIONS
- Weighing Systems
- Analytical Ratiometric Measurements
- Bio-Medical/Oceanographic Data Transmission, Reduction and Display
- Process Control Instrumentation

GENERAL DESCRIPTION

The ADC-I is the first high resolution analog-to-digital converter using a dual-slope integrating technique to be contained in a 3" x 4" x 0.4" module. Two models offer a choice of either a 14-bit binary word output or a 4½ digit BCD output. Both models provide polarity and automatic overload outputs. Designed for applications where noise immunity is a critical requirement, the ADC-I features 0.01% accuracy, excellent temperature stability, automatic zero correction, and low cost.

INTEGRATING TECHNIQUE

Operation of the ADC-I is based on the time relationship between two integration intervals (see Figure 1). Upon convert command the analog input is integrated. After a known time interval, the polarity of the integrated input is determined. The counter is reset to zero and with a reference applied to the integrator, clock pulses are counted until a comparator detects a zero output. The counter then provides a digital representation of the analog input.

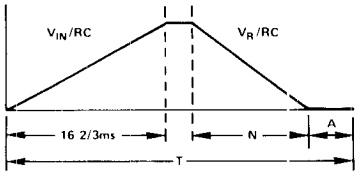


Figure 1. Simplified Timing Diagram

Internal control logic provides a polarity indication as the reference integration begins. An overload output occurs if the reference integration requires a longer time interval than the input integration.

Following the conversion cycle or after an overload is detected the integrator is automatically zeroed and ready for another conversion.

ADVANTAGES OF DUAL-SLOPE

In the successive approximation converter, where high speed is offered the major limitation is resolution and accuracy due to noise interference. In contrast to this approach, integrating

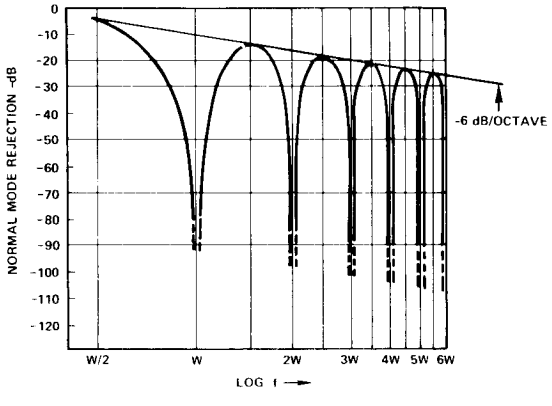


Figure 2. Normal Mode Rejection

SPECIFICATIONS (typical @ +25°C and rated supply unless otherwise noted)

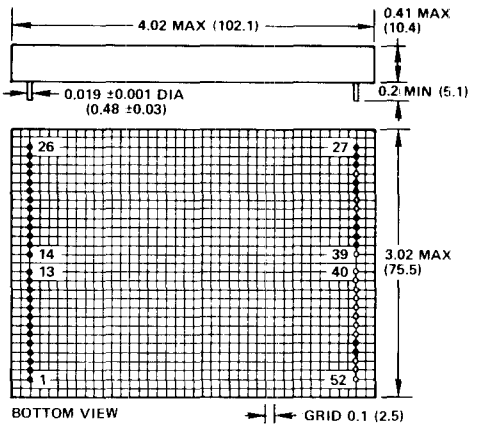
RESOLUTION	
ADC-14I	14 Binary Bits plus sign
ADC-17I	4½BCD digits plus sign
ACCURACY	
Relative	Adjustable to 0.01% of reading ±1 Bit
Calibration	Recommended 6 months calibration cycle
Monotonicity	Guaranteed
INPUT CHARACTERISTICS	
Analog Input	±10V FS (20% overrange on ADC-17I)
Continuous Overload	±100V max (with or without power)
Peak Series Mode	±75V max dynamic range
Series Mode Rejection	-70dB
Input Impedance	180kΩ
REFERENCE VOLTAGES	
Internal	±6.2V ±5%, balanced to 0.01%
	±2mA current drain
	< 1Ω output impedance
External	±7.5V max for ratiometric operation
	100kΩ input impedance
TEMPERATURE COEFFICIENT	
Zero	±10μV/°C (0 to +40°C)
	±30μV/°C (+40°C to +70°C)
Gain	±5ppm of reading/°C (exclusive of ref.)
Reference	
Positive Reference	5ppm/°C
Negative Reference	10ppm/°C
CONVERSION TIME	40ms max (see Table 1)
Input Integration	16-2/3ms (see Table 1)
Sample Rate	25/sec (see Table 1)
CONVERT COMMAND	Positive pulse, 100ns min, 100μs max
(TTL/DTL Compatible)	Leading edge resets previous data
	Trailing edge initiates conversion
CLOCK (TTL/DTL Compatible)	
Internal	720kHz (see Table 1)
Stability	200ppm/°C
External	1.2MHz max
Input Fan In	1 TTL load
OUTPUTS (TTL/DTL Compatible)	
Parallel Data	
Sign Plus Magnitude BCD	10.000V FS (11.999 with overrange)
Sign Plus Magnitude BIN	10V—LSB FS (MSB included)
Polarity (Fan Out 8)	Logic "0" indicates positive input
$\overline{\text{\quad\quad}}$ (Fan Out 2)	Logic "1" indicates negative input
$\overline{\text{Status}}$ (Fan Out 9)	Logic "0" during conversion
$\overline{\text{Ramp Up}}$ (Fan Out 2)	Logic "0" during ramp up
$\overline{\text{Ramp Down}}$ (Fan Out 2)	Logic "0" during ramp down
Overload (Fan Out 10)[1]	Logic "1" after conversion indicates overload
POWER SUPPLY REQUIREMENTS[2]	±15V dc @ 30mA
	+5V dc @ 200mA
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +125°C
ADJUSTMENTS	
Zero	Automatic Internal Compensation
Gain	(3) 200Ω Trim Pots
	See Adjustment Procedures
DIMENSIONS	3" x 4" x 0.4"

[1] Overload is Logic "1" during conversion. At the end of a normal (non-overload) conversion, i.e., when Status goes high "overload" goes to Logic "0". Overload remains Logic "1" at the end of an overload conversion.
[2] Recommended Power Supply: Analog Devices models 904 and 903.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

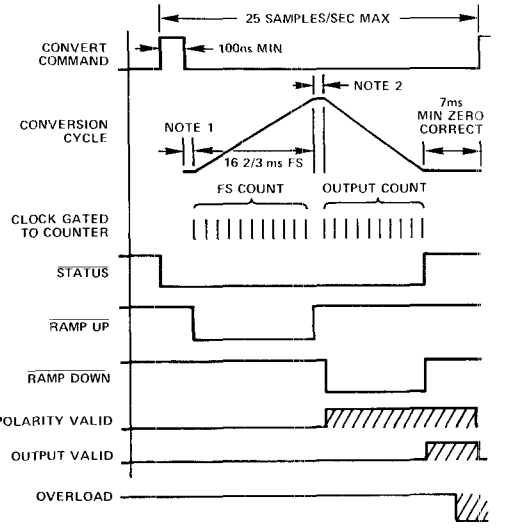
Dimensions are shown in inches and (mm).

ADC-17I



NOTE: On the ADC-14I;
Pins 6, 7 and 8 are omitted.
Bits 3 through 14 are located at pins 9 through 20, respectively.

TIMING DIAGRAM



[1] Maximum delay of one clock pulse to synchronize with clock.
[2] Delay of 1½ clock pulses to reset counter and strobe comparator for polarity data.

ORDERING GUIDE:

ADC – XX I
- 14 - 14 Binary Bits plus sign
- 17 - 4½BCD digits plus sign

the input sacrifices conversion speed but achieves high resolution due to the excellent noise rejection. The ADC-I integrates the analog input for exactly one ac line period – clearly the most prevalent source of noise error. Adjustment of this interval is possible by changing the clock frequency or through use of an external clock. This allows the user to obtain optimum noise rejection operating with a 60Hz or a 50Hz line frequency.

In addition to its ability to maintain resolution in the presence of noise the dual-slope technique offers excellent temperature performance. This is possible since errors due to drift in the integrator time constant or clock affect both integrations and are therefore cancelled. This reduces output error source almost solely to the accuracy of the reference voltages, allowing long term adjustment free operation.

GROUND CONNECTIONS

Analog ground and power ground are NOT internally connected and must be connected externally. Difference in potential must be $<0.1V$ at the module.

CLOCK OPERATION

An external clock may be connected directly to pin 24. The continuous running internal clock may be used by connecting pins 24 and 25. The internal clock frequency for binary and BCD models differs to maintain an input integration period of approximately 16-2/3ms. Optimum line noise rejection is achieved by adjustment of this frequency with an

Line Frequency	60Hz	50Hz
Clock Frequency		
ADC-14I	983kHz	819.2kHz
ADC-17I	720kHz	600kHz
Ramp Up Period	16-2/3ms	20ms
Conversion Time	40ms max	50ms max
Max Sample Rate	25/sec	20/sec

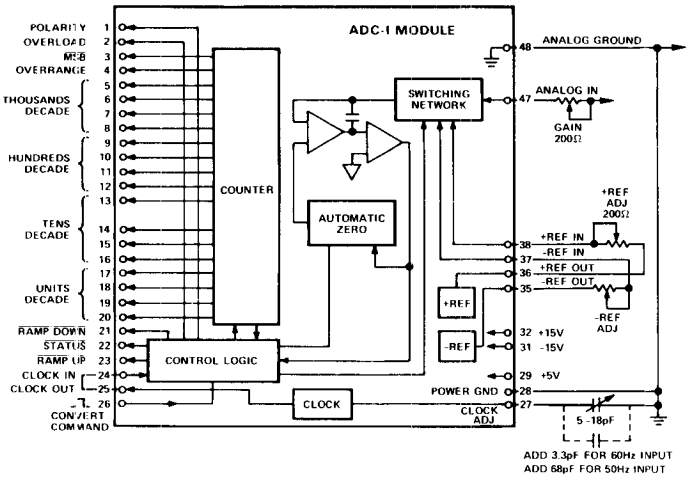
Table 1. Optimum Clock Frequencies

external trimmer capacitor between pins 27 and 28. A 68pF capacitor in parallel with the trimmer allows adjustment for 50Hz line operation. The adjustment can be made with a frequency counter or by measuring the RAMP UP period at pin 23. The latter method requires a convert command signal.

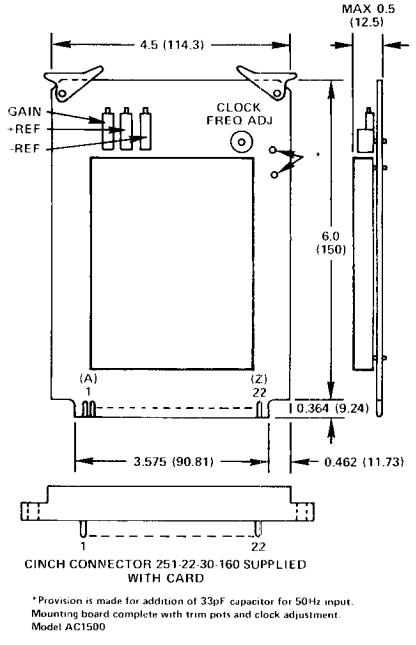
ACCURACY ADJUSTMENTS

Zero correction is automatically made after every conversion as indicated in the timing diagram. Trim pots shown in the block diagram allow for adjustment of gain. The reference adjustments are used to balance positive and negative outputs fro a known input. Future gain adjustment can then be made with the single pot in series with the analog input without affect on the polarity balance. With the gain pot set to center position the recommended procedure is to adjust the -REF with +8.7500V input, reverse the polarity of the input and adjust the +REF. The ideal outputs are:

ADC-14I (BIN) 11100 0
ADC-17I (BCD) 8750



Block Diagram and Pin Designations



*Provision is made for addition of 33pF capacitor for 50Hz input. Mounting board complete with trim pots and clock adjustment. Model AC1500

ADC-17I			
Analog Input	1	A	Analog Ground
Analog Ground	2	B	Analog Ground
+Ref In	3	C	+Ref Out
-Ref In	4	D	-Ref Out
Power Ground	5	E	Power Ground
Polarity	6	F	MSB Bit 1
Overload	7	H	Bit 2
MSB Bit 1	8	J	Bit 3
N.C.	9	K	Bit 4 (N.C.)
N.C.	10	L	Bit 5
N.C.	11	M	Bit 6 (Bit 3)
Ramp Down	12	N	Bit 7 (Bit 4)
Status	13	P	Bit 8 (Bit 5)
Ramp Up	14	R	Bit 9 (Bit 6)
Clock In	15	S	Bit 10 (Bit 7)
Clock Out	16	T	Bit 11 (Bit 8)
Convert Command	17	U	Bit 12 (Bit 9)
N.C.	18	V	Bit 13 (Bit 10)
+15V	19	W	Bit 14 (Bit 11)
-15V	20	X	Bit 15 (Bit 12)
N.C.	21	Y	Bit 16 (Bit 13)
+5V	22	Z	LSB Bit 17 (Bit 14)

NOTE: Changes for ADC-14I shown in parenthesis.

#AC1500 Mounting Board and Pin Connections. Dimensions shown in inches and (mm).

RATIOMETRIC OPERATION

The ADC-1 is ideally suited for ratiometric measurement analytical instrumentation, strain gages, or resistance bridges. This is easily implemented since normal operation of the converter is based on the ratio of two integration intervals.

A ratio measurement is performed in the same manner with the exception of the ramp down interval being determined by an external reference functioning as the Y input. To normalize the ratio to any required scaling, a series resistor (R_N) is added in this Reference Input. This should be a low T.C. (5ppm) wirewound or Vishay resistor. With R_N of approximately 54k a reading of 10000 will be obtained with X = Y. It should be noted that progressively less accurate division is obtained as Y → 0.

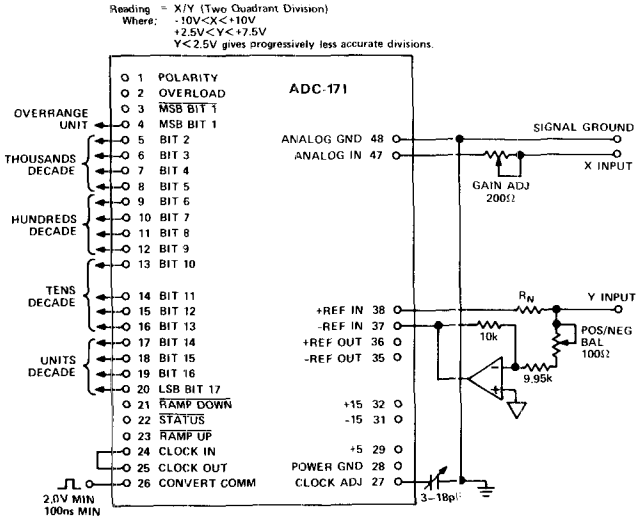


Figure 3. Ratiometric Operation With Adjustments

TWO QUADRANT RATIO

Use of an external unity gain inverter as shown in Figure 3, makes two quadrant ratio possible. For greatest accuracy and freedom from drift, this should be a chopper stabilized amplifier such as Analog Devices' 235, or 233; IC amplifiers, like the AD504 or AD508, may be used. The balance pot is adjusted for identical readings with both polarities of X input.

ONE QUADRANT RATIO

For one quadrant operation a Y input must be applied to the appropriate reference. When Analog Input (X) is positive a negative Y is required; when X is negative a positive Y is required.

SERIAL PULSE TRAIN OUTPUT

Gating the ramp down signal with the clock in signal gives an output pulse train during ramp down only. Use of 7400 series logic elements is recommended. The number of pulses out is equal to the ramp down count which is proportional to the input value, "X".

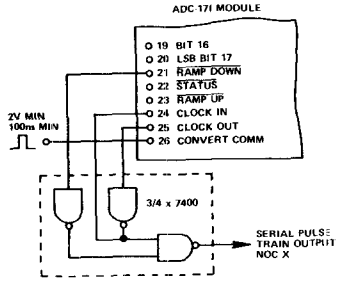


Figure 4. Serial Pulse Train Output

OUTPUT STORAGE REGISTER

An output storage register may be required for driving a non-blinking display, or where a conversion has to be separately called for (see Figure 5).

Data is transferred to the storage latches (7475), after conversion, during a ½μs strobe pulse provided by the monostable 74121. The 7440 is a buffer driver supplying the clock lines to the 7475 (which have a total fan in of 32). Complementary outputs are also available from the 7475.

A reset or load for an external counter may be provided before the pulse train by either of the following logic signals:

1. Conv. Command (Prior to Conversion)
2. Ramp Up (During Conversion)

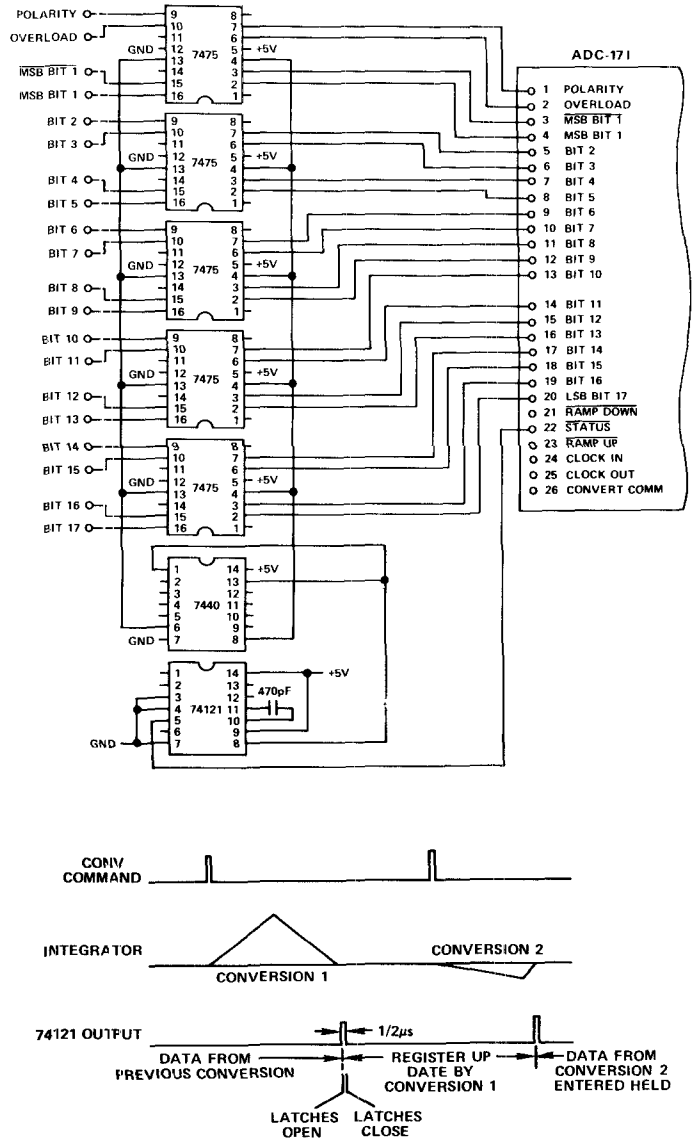


Figure 5. Storage Register Output and Timing Diagram