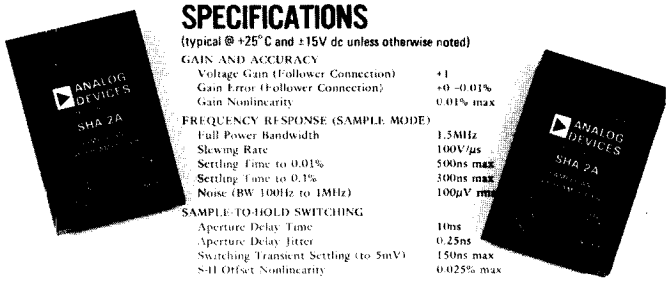
ANALOG DEVICES

Very High Speed 12 Bit Sample-and-Hold Amplifier

SHA-2A

FEATURES
±10V Range
10ns Aperture Delay
¼ns Aperture Jitter
300ns Settling Time
0.01% Linearity Error
Complete with Input Buffer

APPLICATIONS
Track and Hold
Peak Measurement Systems
Data Acquisition Systems
Simultaneous Sample-and-Hold



GENERAL DESCRIPTION

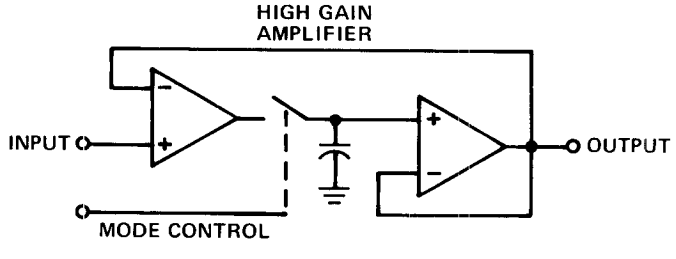
The SHA-2A is a very fast sample-and-hold module with accuracy and dynamic performance appropriate for application with very fast 12-bit A/D converters. In the "sample" mode, it acts as a fast amplifier, tracking the input signal. When switched to the "hold" mode, the output is held at a level corresponding to the input signal voltage at the instant of switching. The droop rate in "hold" mode is appropriate to allow 12-bit accurate conversion by very fast A/D converters, e.g. those having total conversion times of up to several microseconds.

DYNAMIC PERFORMANCE

The SHA-2A was designed for use with very fast A/D converters such as the Analog Devices' ADC11.03 series, which convert 12 bits in less than 4μs. Since such converters will often be used to acquire data for fast slewing signal sources, the dynamic parameters were designed with this in mind. Slewing rate is 100V/μs, and settling time to 0.01% is <500ns. The aperture time of <10ns, and aperture jitter of 0.25ns, means that an input signal slewing at 200mV/μs (3kHz) will be acquired to appreciably better than one LSB uncertainty for a 12-bit converter. The maximum droop rate of 100μV/μs means that when the SHA-2A is in "hold," its output is holding constant for the ADC input, changing <0.1LSB per conversion time for a 1μs 12-bit ADC. The fast settling of the sample-hold transient allows the following A/D converter to make an accurate MSB decision only 150ns after the "hold" command is applied.

UNIQUE CIRCUIT ARRANGEMENT

Most sample-and-hold amplifier modules have input terminals connected either to a unity gain buffer, or directly to the hold capacitor through a switch. In the SHA-2A an input buffer is used, but the feedback connection has been omitted in order to allow the user to connect the SHA-2A as a follower, for unity gain, or to provide gain in order to simplify signal conditioning in his system. We call the user's attention to the fact that the input buffer bandwidth will go down as gain is increased, as it does for all op amps. Performance data is given for the unity gain buffer connection.



Typical Block Diagram

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

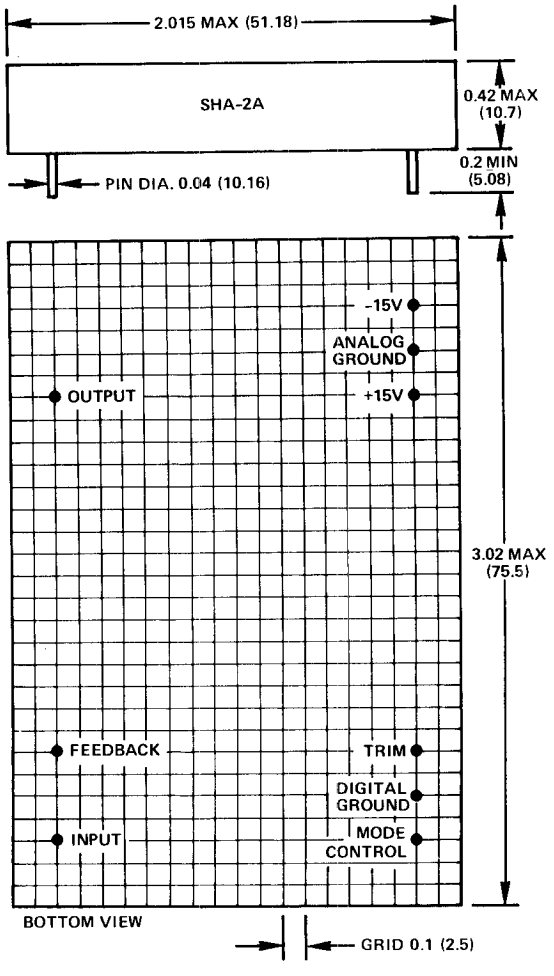
GAIN AND ACCURACY	
Voltage Gain (Follower Connection)	+1
Gain Error (Follower Connection)	+0 −0.01%
Gain Nonlinearity	0.01% max
INPUT CHARACTERISTICS	
Input Impedance	$10^{11}\Omega$ and 7pF
Input Bias Current	100pA max
Input Range	±10V min
Initial Offset Voltage	Adjustable to 0
Offset vs Temp	100μV/°C max
Offset vs Supply	500μV/%
FREQUENCY RESPONSE (SAMPLE MODE)	
Full Power Bandwidth	1.5MHz
Slewing Rate	100V/μs
Settling Time to 0.01%	500ns max
Settling Time to 0.1%	300ns max
Noise (BW 100Hz to 1MHz)	100μV rms
SAMPLE-TO-HOLD SWITCHING	
Aperture Delay Time	10ns
Aperture Delay Jitter	0.25ns
Switching Transient Settling (to 5mV)	150ns max
S-H Offset Nonlinearity	0.025% max
HOLDING CHARACTERISTICS	
Droop Rate	100μV/μs max
Feedthrough (10kHz, 20V p-p Input)	5mV p-p max
OUTPUT CHARACTERISTICS	
Output Voltage	±10V min
Output Current	±20mA min
Short Circuit Current	±70mA
Maximum Capacitive Load	200pF
DIGITAL CONTROL	
Logic Levels[1]	
Sample ("1")	>+2V @ 1μA to 3.7V @ 1mA
Hold ("0")	<0.8V 0 to 0.8V @ −7mA
POWER REQUIREMENTS	±15V ±2% @ 100mA
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	−25°C to +85°C
MATING SOCKET	AC1035

NOTE
[1] To achieve rated specifications, logic driving digital control input should be Schottky TTL.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Pins are half hard brass, gold plated per MIL-G-45204B, Class I, Type II - Pin Diameter is 0.040" (0.483mm) ±0.001" (0.025mm).

MATING SOCKET AC1035

The AC1035 is a simple socket assembly, 2" x 3", for mounting the SHA-2A.

MOUNTING BOARD AC1503

The AC1503 is a 2¼" x 4½" PC board with edge connector. It contains a trimmer pot for adjustment of offset, as well as a logic chip, needed to simulate terminal characteristics of the SHA-2. When the SHA-2A is mounted on the AC1503, the assembly is a pin-compatible replacement for the SHA-2.

CIRCUIT DESCRIPTION

The SHA-2A is a typical sample-and-hold module in that it consists of an input isolator, a fast switch, the storage element, and an output buffer. It differs from typical designs in two particular respects:

1. Speed – since it was designed to be compatible with very fast A/D converters of the 1μs total conversion time class, aperture delay time was reduced to 10ns, aperture jitter to 0.25ns, and settling time to 300ns for 10-bit performance.

2. Application versatility – the user completes the feedback circuit for the SHA-2A external to the module. Therefore, the module may be used in various input configurations and can easily be arranged to provide circuit gain of more than unity, to simplify signal conditioning in a subsystem.

FEEDBACK CONNECTIONS

A block diagram of the SHA-2A is shown in Figure 1. The input section acts as a voltage-to-current converter, providing the current needed to charge the "HOLD" capacitor. The output amplifier isolates the "HOLD" capacitor, and provides low output impedance for driving the load. Since feedback is not hardwired in the module, both inverting and noninverting input terminals are available, and the SHA-2A can be connected as a follower with unity gain or potentiometric gain, as well as an inverter or even a differential amplifier. Since the unity gain follower mode will be the most frequent application, performance data in the specifications is based on this operating mode.

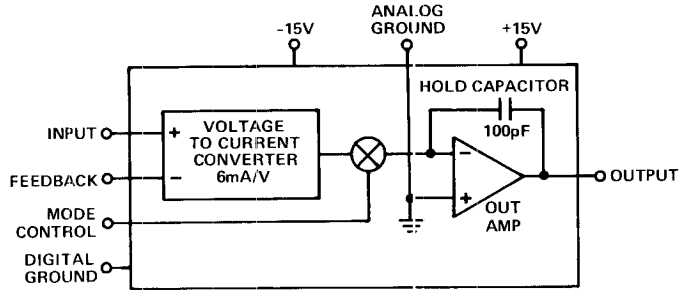


Figure 1. Block Diagram

1. Figure 2 shows feedback connections to the SHA-2A for the unity gain follower mode. Output (pin #3) is connected to feedback (or – input, pin #2). Input signal is applied to pin #1.

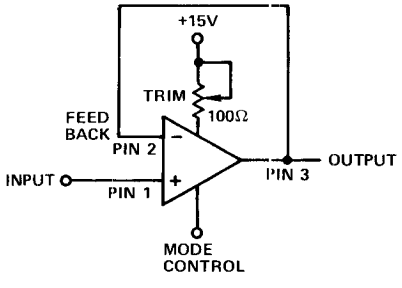


Figure 2.

2. Figure 3 shows feedback connections for noninverting operation with potentiometric gain. When the indicated values are installed, gain will be +5. As in all operational amplifiers, gain-bandwidth product is a constant for a given sample-and-hold. Effective 3dB bandwidth will be inversely proportional to gain.

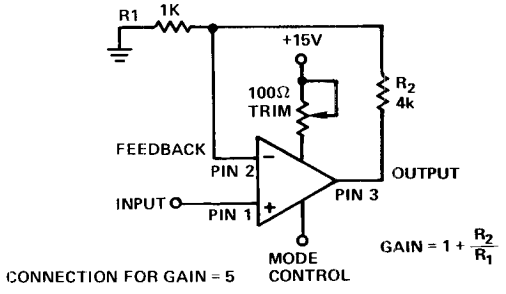


Figure 3.

3. By using conventional operational amplifier feedback connections, the SHA-2A can be connected for use as an inverter, with various gains (as determined by the R_F/R_I ratio), or as a differential amplifier.

CHARACTERISTICS OF REAL SAMPLE-HOLDS

In the ideal Sample-Hold of Figure 4a, tracking is error-free, acquisition and release occur instantaneously, settling times are zero, and hold is infinite. Commercially-available units are specified in terms of the extent to which they depart from the ideal. Here are some of the commonly-occuring deviations.

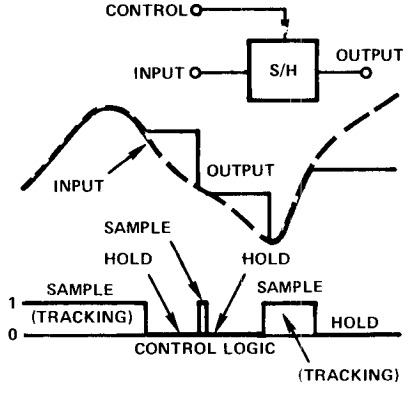


Figure 4a.

<u>During Sample (Figure 4b):</u>

Settling Time: The time required for the output to attain its final value within a specified fraction of full-scale when a full-scale input step is applied (0 to ±FS or -FS to +FS). See also *Acquisition Time* (Figure 4e).

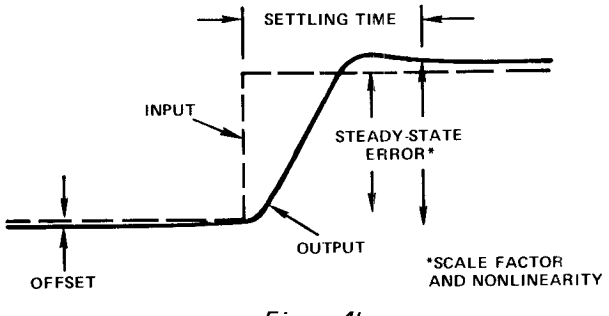


Figure 4b.

Sample to Hold (Figure 4c):

Aperture Time: The time elapsing between the command to *Hold* and the actual opening of the *Hold* switch. It has two components: a nominal time delay, and an uncertainty caused by jitter or variation from time-to-time or unit-to-unit. If a signal changing at a rate of 1V/μs must be resolved to within 0.1% of 10V (FS), the aperture *uncertainty* must be <10ns, provided that it is possible to anticipate the nominal delay and advance the command by an appropriate interval. In some sampled-data system applications, such as spectrum analyzers, auto- and cross-correlation function generators, the delay is unimportant, but the uncertainty directly affects uniformity of the sampling rate.

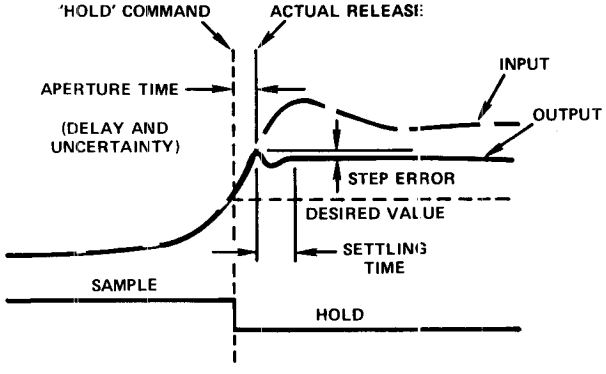


Figure 4c.

Switching Transients: At the time the switch opens, the circuit may not be in equilibrium – especially if the signal is changing rapidly – because of amplifier delay error, etc. This will cause transients at the time the switch opens.

Settling Time: The interval required for the output to attain its final value within a specified fraction of full scale, following the opening of the switch.

Sample-to-Hold Offset: A step error occurring at the initiation of the *Hold* mode caused by "dumping" of charge into the storage capacitor via the capacitance between the control circuit and the capacitor side of the switch (e.g., the gate-to-drain capacitance of a field-effect transistor).

During Hold (Figure 4d):

"DROOP": A drift of the output at an approximately constant rate caused by the flow of current through the storage capacitor (dV/dt = I/C). The current is the sum of the leakage across the switch and the amplifier's bias current.

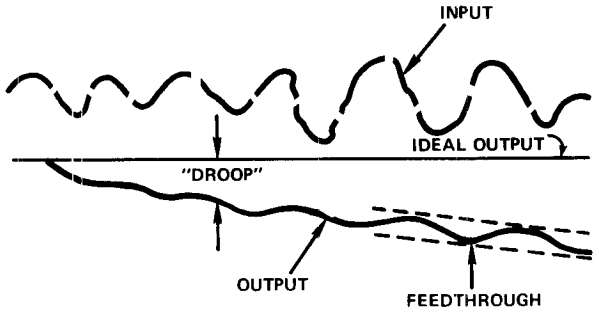


Figure 4d.

Feedthrough: The fraction of input signal that appears at the output in *Hold*, caused primarily by capacitance across the switch. Usually measured by applying a full-scale sinusoidal input at a fixed frequency (e.g., 20V p-p at 10kHz), and observing the output.

Dielectric Absorption: The tendency of charges within a capacitor to redistribute themselves over a period of time, resulting in "creep" to a new level when allowed to rest after large, fast changes. <0.01% for good polystyrene and teflon capacitors, as large as several percent for ceramic and mylar capacitors.

Hold to Sample (Figure 4e):

Acquisition Time: The time duration for which an input must be applied for sampling to the desired accuracy. Essentially the same as *Settling Time* for feedback types.

Hold-to-Sample Transients: Transients (e.g., spikes) occurring between the *Sample* command and final settling.

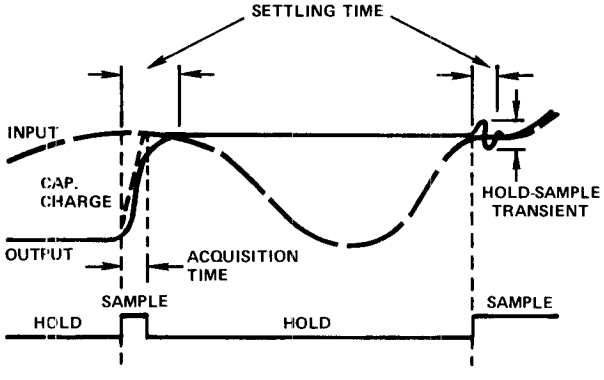


Figure 4e.