ANALOG DEVICES

High Resolution Sample-and-Hold

SHA-6

FEATURES
- Gain Range: 1 to 1000
- Gain Stability: 2ppm/month (Gain = 1)
- Linear Range: ±11V
- CMR: 80dB min at any gain
- Settling Time: 1ms to 0.00075% (Gain = 100)
- Offset Stability: ½ppm/°C
- Aperture Uncertainty: ~10ns
- Droop Rate in Hold: 10mV/sec max

GENERAL DESCRIPTION

The SHA-6 is a high accuracy wide dynamic range sample-and-hold module designed as a companion to the high resolution ADC-16Q A/D converter. It is designed to acquire an input signal to 16 bit accuracy, and to hold that signal fixed during the time that the following A/D is converting. Although sample and holds are most frequently used with unity gain, the gain of the SHA-6 is easily adjustable over the range 1 to 1000, by changing a single resistor in accordance with the specified gain formula. Since very high resolution A/D converters are likely to have moderate conversion speeds (because of the longer time needed by various amplifiers in the system to settle to 0.00075%), the SHA-6 has droop rate in "hold" of less than 10mV/sec.

PERFORMANCE CHARACTERISTICS

The SHA-6 was designed for use with A/D converters with resolution of up to 16 bits, consequently all operating parameters are defined in terms of high accuracy and stability, including effects of the instrumentation input buffer. Gain stability is 2ppm/°C and 2ppm/month. Offset stability (RTO) is ½ppm/°C and 2ppm/month. Settling time at unity gain is 5ms to 7.5ppm. Settling time decreases to 1ms to 7.5ppm for gain of 100. Recovery time from a 10 times overload is 150μs.

Signal processing characteristics unique to a sample and hold circuit were optimized to be truly appropriate for usage with 16 bit converters. Sample to hold offset is less than 75μV, while the switching transient is only 5mV (100kHzBW) and has decayed to 7.5ppm within 25μs. Aperture delay uncertainty is approximately 10ns, giving the SHA-6 the ability to acquire a signal slewing at 10V/ms to an uncertainty of 100μV, or two thirds of an LSB for the ADC-16Q.

HIGH PERFORMANCE INPUT BUFFER

It is next to impossible to supply any signal to a signal processing module completely free of common mode noise, and since 16 bit converter LSBs are only 152μV, it takes very little common mode noise to affect the accuracy of a reading. For this reason, the SHA-6 (as well as the ADC-16Q) has been provided with a true differential instrumentation amplifier as its input buffer. This buffer will allow the user to take full advantage of the high resolution and wide dynamic range capabilities of these fine system components.

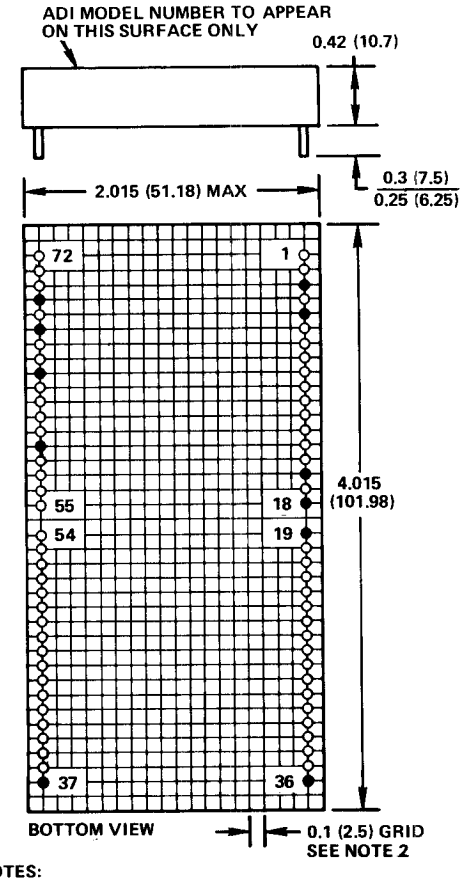
SPECIFICATIONS (typical @ +25°C and ±15V, unless otherwise noted)

GAIN AND STABILITY	
Gain Range (set by single resistor R_G)	1 to 1000
Gain Resistor Formula	$G = 1 + \frac{2x10^4}{R_G}$
Gain Error from Formula Value	0.2% max
Stability vs Time	±0.0002%/month
Stability vs Temp.	±0.0002%/°C
INPUT CHARACTERISTICS	
Impedance (Differential and Common Mode)	10^9 ohm (min) & 5pF (max)
Bias Current	80nA max
vs Temp.	250pA/°C max
Difference Current	40nA max
vs Temp.	100pA/°C max
Max Linear Differential and Common Mode	±11V
Max Safe Differential and Common Mode	$\pm V_S$
Common Mode Rejection (DC to 60Hz)	80dB min at any gain
DYNAMIC CHARACTERISTICS	
Unity Gain Small Signal BW	20kHz min
Full Power BW	2kHz min
Slew Rate	50V/ms
Settling Time to 0.00075%	
Gain = 1	5ms max
Gain = 10	3ms max
Gain = 100	1ms max
Recovery Time for x10 Overload	150μs max
SAMPLE-TO-HOLD SWITCHING	
Aperture Delay	-1.7μs
Aperture Uncertainty	10ns
Switching Transient Settling (to 75μV)	10μs max
Sample to Hold Offset	75μV max
HOLDING CHARACTERISTICS	
Feedthrough (DC to 10kHz)	-100dB min
Droop Rate	10mV/sec max
OUTPUT CHARACTERISTICS	
Output Voltage	±11V min @ 3mA min
Capacitive Load	1000pF min
Noise RTO (0.01Hz to 100kHz, 99.9% peak to peak, at any gain)	50μV max
Initial Offset	(1+G)mV max
Offset vs Temperature	5 (1+G)μV/°C max
Offset vs Supply	10 (1+G)μV/% max
Offset vs Time	20 (1+G)μV/mo max
DIGITAL CONTROL	
Logic Levels (TTL/DTL Compatible)	
Sample	0V to 0.8V @ 100μA max
Hold	+2.0V to +5.5V @ 10μA max
POWER SUPPLY	
Voltage, Rated Performance	±15V
Voltage, Operating	±(13-17)V
Current, Quiescent	±17mA max
TEMPERATURE	
Operating	0 to +70°C
Storage	-25°C to +100°C
MATING MOUNTING BOARD	AC1508

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:
1. PINS: 0.040 ±0.001 (10.16 ±0.03) DIA BRASS, GOLD PLATED PER MIL-G-45204B CLASS I, TYPE II
2. GRID AND MARKINGS NEXT TO PINS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT
3. MOUNTING CARD: UNIT MATES WITH AC1508 (NOT SUPPLIED WITH UNIT)

CONNECTING THE SHA-6

The SHA-6 is easily interconnected for operation with the ADC-16Q or other high resolution converters, as shown in the diagram of Figure 1. The input divider (R_1, and R_2) will be required only if total differential input signal exceeds ±10 Volts. If the divider is used, it is extremely important to have resistors R_1 precisely equal, in order to avoid unbalance of the input system and degradation of the common mode performance.

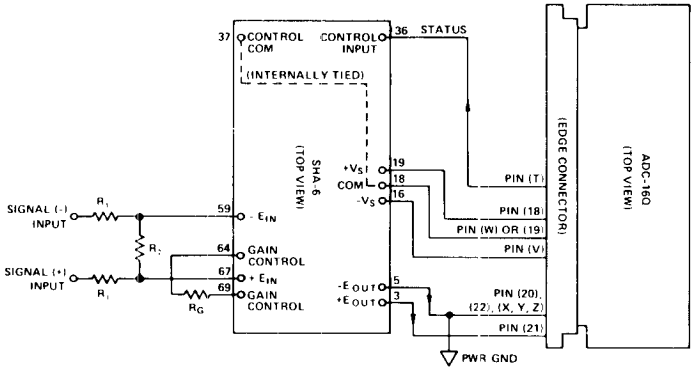


Figure 1. Interconnection of SHA-6 to an ADC-16Q

Because of its extreme stability, the SHA-6 is not provided with terminals for the adjustment of output offset. This adjustment can be made easily by a compensating adjustment of the offset in the following A/D converter, so long as the SHA-6 is operated at low gain, as is usually the case. If the SHA-6 is to be operated at high gain, the initial offset may be too great to allow compensation with the offset adjustment of the following converter. If that should be the case, we recommend the circuit of Figure 2 provide the needed adjustment. The SHA-6 linearity is not disturbed by the common mode signal appearing at its output, since the circuit has high CMR at both the input and the output.

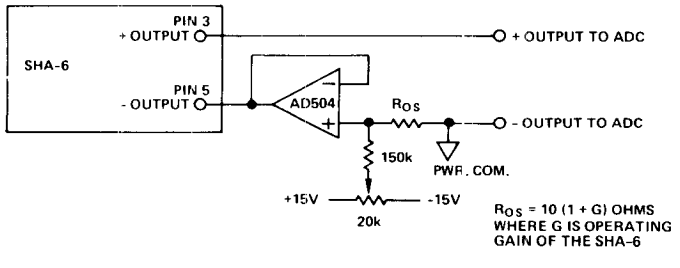


Figure 2. Offset Adjustment Circuit for High Gain Operation

ACCURACY AND INSTALLATION CONSIDERATIONS

The extremely high resolution and linearity of the SHA-6 demanded a systems approach to the design. Problems like common mode noise pickup in just a few feet of wire, or the thermocouple effect of connections of dissimilar materials, cannot be neglected in a 16-bit design. For these and other reasons, users of the SHA-6 should take exceptional care in planning installations, in order to minimize the effects of environmental conditions on system accuracy.

a. The unit and its connector and signal wiring should be located with an eye to optimum isolation from sources of RFI and EMI.
b. Special care must be observed in running input signal wiring to the buffer inputs, in order to avoid degrading the common mode rejection at ac.

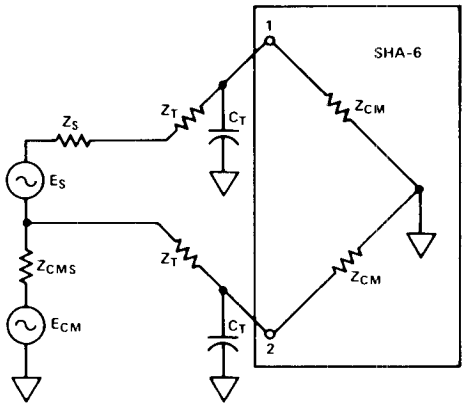
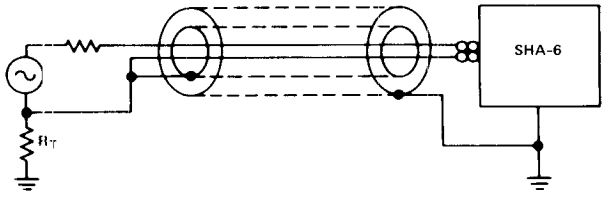


Figure 3. Simplified Equivalent Circuit-Differential Input System

Figure 3 shows a simplified equivalent circuit of the input system for common mode purposes, the points marked 1 and 2 being the input signal terminals, E_S and Z_S being the signal source and source resistance, and Z_T and C_T being the transmission line impedances. The circuit is a bridge, and if it is balanced there is no differential component of E_{CM} appearing across the input terminals.

It is clearly of great importance to maintain balance in Z_T and C_T when a signal source is wired to the converter input. Only a few pF of capacitance unbalance is enough to wipe out the common mode rejection at 60Hz.



Note: 2-wire double-shielded cable is Trompeter Electronics Inc. P/N QRC-78-2 or equivalent.

Figure 4. Shielding of Input Wiring

Figure 4 shows a recommended interconnection of a signal source to the SHA-6. Two-wire double-shielded cable should be used, with the inner shield connected to the "low" side of the signal, to act as a guard. Outer

shield is grounded, and a dc path from signal source to ground MUST be provided, if it is not inherent in the design. To optimize common mode rejection, the double-shielded cable should also be capacitance-balanced. (Such cables with a specification on maximum capacitance unbalance per unit length are available from several manufacturers.)

c. The unit, its connector and wiring should be located in a region of constant, stable temperature. Popular electronic wiring materials almost always involve use of more than one metal, and we must remember that junctions of two metals will act as thermocouples, and will generate error voltages proportional to temperature difference between junctions as well as to temperature gradients along wires. We cannot ignore these effects when the value of an LSB is 152μV!

There is still another dimension to the common-mode problem for high resolution products. Figure 5, the analog power distribution diagram, depicts the presence of a connector by showing its resistance. Typical edge connectors may have resistance of the order of 15 milliohms when mated. Note that the effect of 20mA of common circuit current flow would be the generation of 300μV across the connector! This 300μV appears as a common mode voltage between the SHA-6 *internal* power ground and its signal input terminals. It is therefore clear that, without a high common mode rejection input buffer, neither the SHA-6 nor the ADC-16Q would be able to operate to full linearity – the voltage drop in the connector causes 2LSB's of common mode!

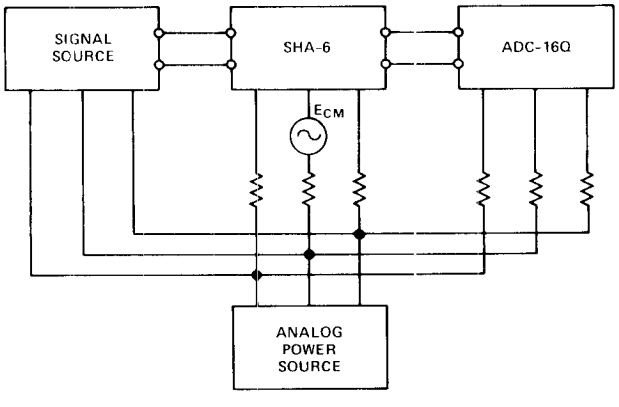


Figure 5. Analog Power Distribution Diagram for a High Resolution Converter Subsystem

With the high common mode rejection input buffers that are standard for both the SHA-6 and the ADC-16Q, not only are connector resistance problems avoided, but the user acquires practically complete flexibility in grounding the subsystem. In tests at our plant, we found no noticeable variation in subsystem performance as several possible grounding schemes were investigated.

THE AC1508 MOUNTING CARD

For the convenience of the SHA-6 user, the AC1508 mounting card is available. The 1508 is a simple edge-connector card with pin receptacles for plugging in the SHA-6. In addition, the AC1508 has provisions for connecting the gain control resistor and the offset adjustment components described in Figure 2. A mating receptacle for the edge connector is included in the price.

APERTURE DELAY DISCUSSION

In the SHA-6, the usual input buffer of the sample and hold is preceded by a high common mode instrumentation buffer. The signal phase delay through this buffer compensates for the aperture delay of the basic SHA circuit, resulting in a total aperture delay for the SHA-6 of –1.7μs. That is, the signal stored in the "hold" mode is that value that appeared at the input terminals 1.7μs *before* the hold command was applied.

HOLD CAPACITOR STORAGE EFFECTS

All known capacitors have storage effects, and cannot be totally discharged instantaneously. The capacitor used in the SHA-6 was especially selected for optimum dielectric polarization effect for this application. When used to condition the input signal for an ADC-16Q, the effect of this polarization will usually be less than one third of an LSB change in the held value during the conversion time plus settling time of the ADC-16Q.