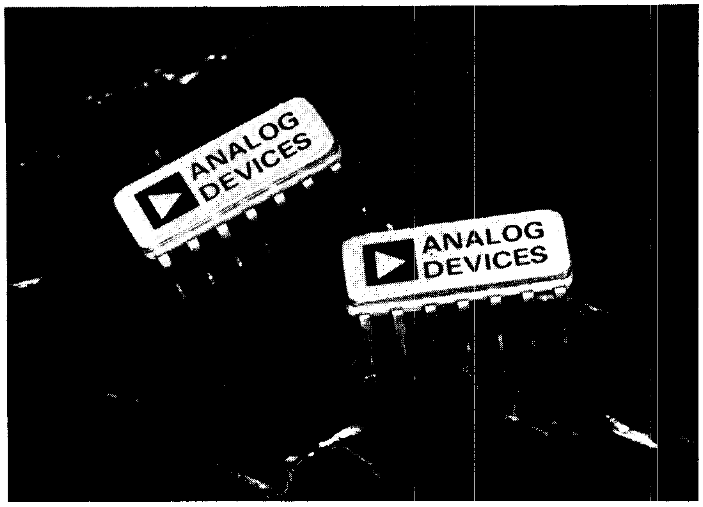
ANALOG DEVICES

Integrated Circuit Precision Instrumentation Amplifier

AD521

FEATURES
Programmable Gains from 0.1 to 1000
Floating Differential Inputs
High CMRR: 110dB min
Complete Input Protection, Power ON and Power OFF
Functionally Complete with the Addition of Two Resistors
Internally Compensated
Gain Bandwidth Product: 40MHz
Output Current Limited: 25mA
Extremely Low Cost



PRODUCT DESCRIPTION

The AD521 is the second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. A true instrumentation amplifier, the AD521 is a controlled gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521, like its predecessor the AD520, should not be confused with an operational amplifier, even though several manufacturers (including Analog Devices) offer op amps that can be used as building blocks in variable gain instrumentation amplifier circuits. An op amp is merely a high gain component requiring the addition of external feedback to complete the amplification function. Because of the limitations of resistor matching in the external feedback circuit and the relatively low input impedance resulting from the input resistors, an instrumentation amplifier circuit designed around op amps frequently provides less than satisfactory performance. Since the AD521 is a complete amplification circuit which does not depend upon external resistor matching for input/output isolation it maintains its high CMRR (110dB min) in any application. In addition, the high impedance inputs are fully protected against over voltages up to 15V greater than the supply voltage.

The AD521 can be operated at gains from 0.1 to greater than 1000 with the addition of only two programming resistors. Excellent dc characteristics are realized through the device's inherently low offset and gain drift and optional one-pot nulling. Dynamic performance is also outstanding with a gain bandwidth product of 40MHz, full peak response of 100kHz and a 10V/µs slew rate.

The AD521 IC instrumentation amplifier is available in three different versions, depending on accuracy and operating temperature range: the economical "J" specified from 0 to +70°C, the low drift "K", also specified from 0 to +70°C and the "S", guaranteed over the full MIL-temperature range, -55°C to +125°C. All versions are packaged in a 14 pin DIP.

PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
3. The AD521 is fully protected for input levels up to 15V beyond the supply voltage and 30V differential at the inputs.
4. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
5. Offset nulling can be achieved with an optional trim pot.
6. The AD521 offers superior dynamic performance with a gain bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5µs to 0.1% of a 10V step.
7. Every AD521 is baked for 40 hours at +150°C and temperature cycled ten times from -65°C to +150°C.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = 25°C unless otherwise specified)

MODEL	AD521J	AD521K	AD521S
GAIN			
Range (For Specified Operation, Note 1)	1 to 1000	*	*
Equation	G = R_S/R_G V/V	*	*
Error from Equation	(±0.25 –0.004G)%	*	*
Nonlinearity (Note 2)			
1≤G≤1000	0.1% max	*	*
Gain Temperature Coefficient	±(3 ±0.05G)ppm/°C	*	±(15 ±0.4G)ppm/°C
OUTPUT CHARACTERISTICS			
Rated Output	±10V, ±10mA min	*	*
Output at Maximum Operating Temperature	±10V @ 5mA min	*	*
Impedance	0.1Ω	*	*
DYNAMIC RESPONSE			
Small Signal Bandwidth (±3dB)			
G = 1	>2MHz	*	*
G = 10	300kHz	*	*
G = 100	200kHz	*	*
G = 1000	40kHz	*	*
Small Signal, ±1.0% Flatness			
G = 1	75kHz	*	*
G = 10	26kHz	*	*
G = 100	24kHz	*	*
G = 1000	6kHz	*	*
Full Peak Response (Note 3)	100kHz	*	*
Slew Rate, 1≤G≤1000	10V/μs	*	*
Settling Time (any 10V step to within 10mV of Final Value)			
G = 1	7μs	*	*
G = 10	5μs	*	*
G = 100	10μs	*	*
G = 1000	35μs	*	*
Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4)			
G = 1000	50μs	*	*
Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)			
G = 1000	10μs	*	*
VOLTAGE OFFSET (may be nulled)			
Input Offset Voltage (V_{OS_1})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	**
vs. Temperature	15μV/°C max (7μV/°C typ)	5μV/°C max (1.5μV/°C typ)	**
vs. Supply	3μV/%	*	*
Output Offset Voltage (V_{OS_O})	400mV max (200mV typ)	200mV max (30mV typ)	**
vs. Temperature	400μV/°C max (150μV/°C typ)	150μV/°C max (50μV/°C typ)	**
vs. Supply (Note 6)	0.005V_{OS_O}/%	*	*
INPUT CURRENTS			
Input Bias Current (either input)	80nA max	40nA max	**
vs. Temperature	1nA/°C max	500pA/°C max	**
vs. Supply	2%/V	*	*
Input Offset Current	20nA max	10nA max	**
vs. Temperature	250pA/°C max	125pA/°C max	**
INPUT			
Differential Input Impedance (Note 7)	3 x 10^9Ω‖1.8pF	*	*
Common Mode Input Impedance (Note 8)	6 x 10^{10}Ω‖3.0pF	*	*
Input Voltage Range for Specified Performance	±10V	*	*
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	*	*
Voltage at either input (Note 10)	V_S ±15V	*	*
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance			
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	**
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	**
G = 1000	100dB min (104dB typ)	104dB min (114dB typ)	**
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	**
NOISE			
Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.5G)^2 + (150)^2}$μV	*	*
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (30)^2}$μV	*	*
Input Current, rms, 10Hz to 10kHz	15pA(rms)	*	*
REFERENCE TERMINAL			
Bias Current	3μA	*	*
Input Resistance	10MΩ	*	*
Voltage Range	±10V	*	*
Gain to Output	1	*	*
POWER SUPPLY			
Operating Voltage Range	±5 to ±18	*	*
Quiescent Supply Current	5mA max	*	*
TEMPERATURE RANGE			
Specified Performance	0 to +70°C	*	-55°C to +125°C
Operating	-25°C to +85°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*

*Specification same as AD521J.
**Specification same as AD521K.

Specifications and prices subject to change without notice.

NOTES:

1. Gains below 1 and above 1000 are realized by simply adjusting the gain setting resistors. For best results, input voltage should be restricted to ±10V for gains equal to or less than 1.

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output of ±9 volts to 18 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the typical frequency below which the amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10μs pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, and an added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10μs pulse at a 1kHz rate. (When a common mode signal greater than V_S - 0.5V) is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, and an added thermal time constant, but will not damage the device.)

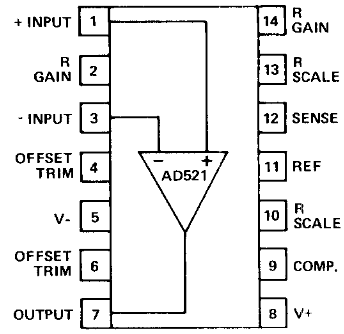
6. Output Offset Voltage versus Power Supply Change is a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when V_S = 0) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 separate 10 second periods with the test circuit of Figure 6.



TOP VIEW

Figure 1. AD521 Pin Configuration

TO-116

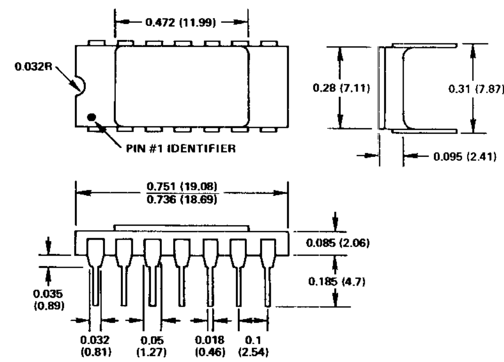
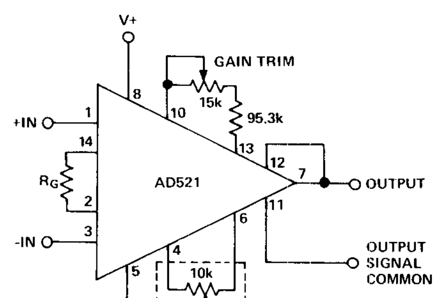


Figure 2. Physical Dimensions. Dimensions shown in inches and (mm).



GAIN	VALUE OF R_G
0.1	1MΩ
1	100kΩ
10	10kΩ
100	1kΩ
1000	100Ω

Figure 3. Operating Connections for AD521

INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output under any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain, can be classified as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the *total* output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or: 30mV + 100(-0.7mV) = -40mV.

By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error with respect to either the input or output by the following formulae:

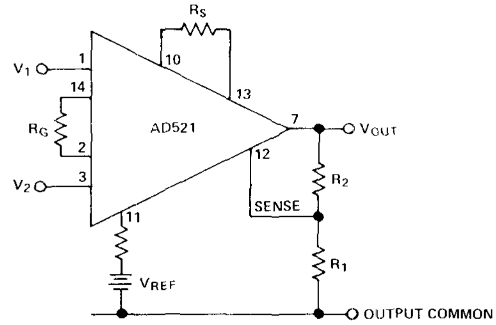
Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain x input error) + output error

As shown in Figure 4, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio, R_S/R_g). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by R_1 and R_2. This gain factor is $1 + R_2/R_1$.

Where offset errors are critical, a resistor equal to the parallel combination of R_1 and R_2 should be placed between pin 11 and V_{REF}. This minimized the offset errors resulting from the input currents at the sense terminal flowing in R_1 and R_2. Note that gain changes introduced by changing the R_1/R_2 attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired, V_{REF} can be placed in series with pin 11. This offset is then multiplied by the gain factor $1 + R_2/R_1$ as shown in the equation of Figure 4.



$$V_{OUT} = \left[V_{REF} + \left(\frac{R_S}{R_G}\right)(V_1 - V_2)\right]\left[\frac{R_1 + R_2}{R_1}\right]$$

Figure 4. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing R_1 and R_2 will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

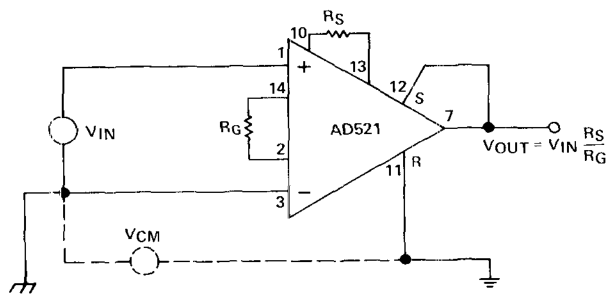


Figure 5. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the AD521.

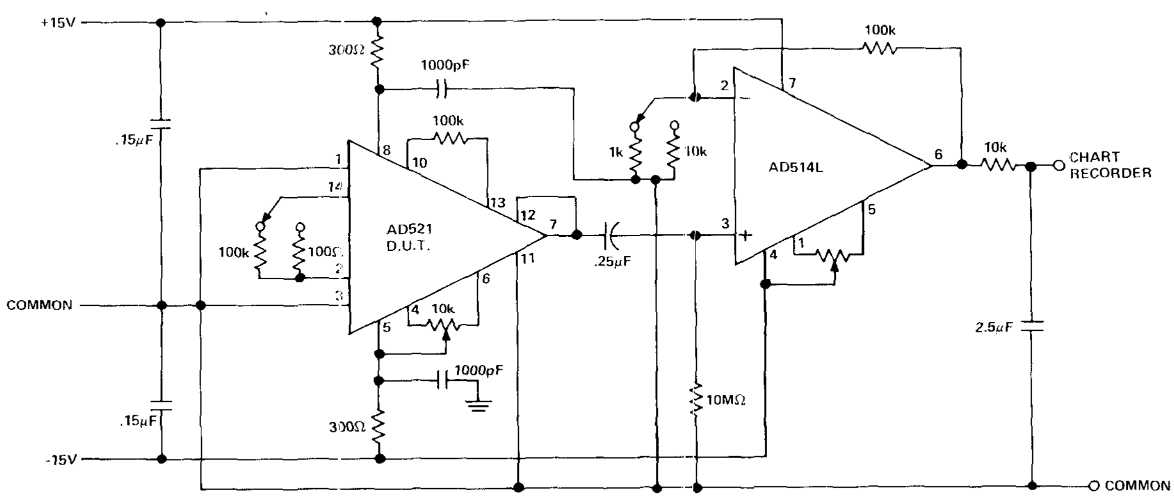


Figure 6. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.