ANALOG DEVICES

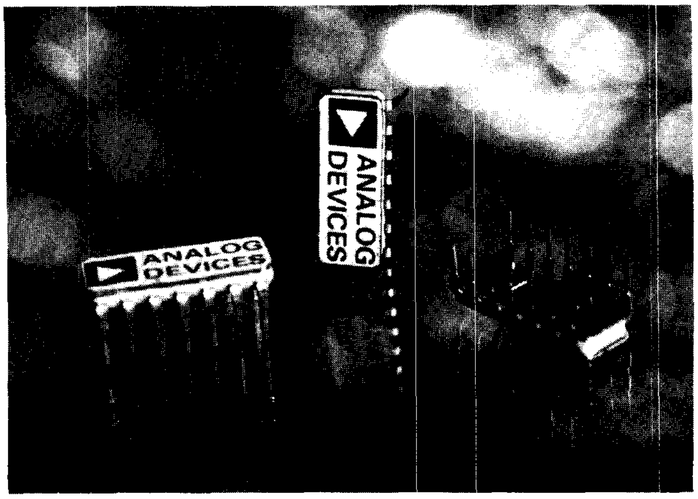
IC Programmable Multiplier Divider Computation Circuit

FEATURES

Transfer Function: XY/Z
Guaranteed ±0.5% max 4-Quadrant Error (AD531L)
Guaranteed Accuracy over Temperature (AD531L and AD531S)
High Speed: 45V/µs
Fully Protected Inputs and Output
Monolithic Construction

APPLICATIONS

Multiplication & Division
True rms-to-dc Conversion
Vector Computation
Absolute Value



GENERAL DESCRIPTION

The AD531 is the first monolithic programmable multiplier/divider to provide the true transfer function $V_X \cdot V_Y / kI_Z$ without the need for an external level shifting op amp at the output. Not just a multiplier, the AD531 is truly a computation circuit that is ideally suited to such applications as automatic gain control (AGC), true rms-to-dc conversion, ratio determination and vector operations; in addition, it provides the normal mathematical functions of four-quadrant multiplication, two-quadrant division and squaring, and square rooting. Flexibility of operation is achieved by means of the variable scale factor kI_Z, which can be set by an external resistor or varied dynamically by an externally derived reference current to obtain the overall transfer function $V_X \cdot V_Y / V_Z$. This provision for the direct computation of three variables greatly simplifies the design of such complex circuits as the true rms-to-dc converter and Flow Rate Computers. Further, multipliers less flexible than the AD531 must put the multiplying element in the feedback of an op amp to obtain division, often with significant sacrifice in accuracy and bandwidth.

The unique features of the AD531 include a differential V_X input with 75dB of common mode rejection, an internally derived stable reference for use in fixed scale applications, and a sense feedback terminal for simple load sensing or special applications. Further, the AD531's guaranteed accuracy, overall high performance and ease of use compare favorably with modular multipliers, while its IC construction provides significant advantages in size, reliability and economy.

The AD531 consists of a differential input transconductance multiplying element, a stable reference and an output amplifier on a single monolithic chip. The circuit's complement of required external components is limited to feedthrough and output zero adjusting trim pots and passive or active adjustment of the scaling current, I_Z.

The AD531J, AD531K and AD531L feature maximum multiplying errors of ±2%, ±1% and ±0.5% (I_Z = full scale) respectively at +25°C, and are rated for operation from 0 to +70°C. The AD531S has a maximum multiplying error of ±1% (I_Z = full scale) at +25°C and is rated for operation over the full military temperature range, −55°C to +125°C. All types are provided in the hermetically sealed TO-116 ceramic DIL package.

GUARANTEED TEMPERATURE PERFORMANCE

In addition to verification of accuracy at +25°C, the AD531L and AD531S are 100% tested for maximum error limits of ±1.5% and ±3.0% respectively at their extreme operating temperature limits (0 and +70°C for the L version; -55°C and +125°C for the S version).

SPECIFICATIONS

(typical @ +25°C, externally trimmed, $R_L \geqslant 2k\Omega$, sense terminal connected to output, and $V_S = \pm15V$ dc unless otherwise specified)

PARAMETER	CONDITIONS	AD531J	AD531K	AD531L	AD531S
ABSOLUTE MAX RATINGS					
Supply Voltage		±18V	*	*	±22V
Internal Power Dissipation		500mW	*	*	*
Input Voltage (Note 1)					
V_X, V_Y, Sense, C, Y_O, V_{OS}		$\pm V_S$	*	*	*
X_O		0V to $+V_S$	*	*	*
B input		$-V_S$ to ($-V_S$ +6V dc)	*	*	*
Input Current					
C input		+750μA	*	*	*
Rated Operating Temp Range		0 to +70°C	*	*	−55°C to +125°C
Storage Temp Range		−65°C to +150°C	*	*	*
Lead Temperature	60 sec. soldering	+300°C	*	*	*
Output Short Circuit	To ground	Indefinite	*	*	*
PERFORMANCE SPECIFICATIONS					
Transfer Function		$V_X V_Y / kI_Z$	*	*	*
Total Error (% of full scale)	$kI_Z = +10V$	±2.0% max [±1.5% typ]	±1.0% max [±0.7% typ]	±0.5% max [±0.3% typ]	±1.0% max [±0.5% typ]
	T_{min} to T_{max}, $kI_Z = +10V$	±2.5%	±1.5%	±1.5% max	±3.0% max
vs. Temperature	T_{min} to T_{max}, $kI_Z = +10V$	±0.04%/°C	±0.03%/°C	±0.01%/°C	±0.02%/°C max [±0.01%/°C typ]
Total Error	$kI_Z = +1V$ dc, $V_X = \pm1V$ dc	±2.0%	±1.0%	±0.5%	±1.0%
Nonlinearity					
X input (Note 2)	$V_X = V_O = 20V(p\text{-}p)$	±0.8%	±0.5%	±0.3%	±0.5%
Y input (Note 2)	$V_Y = V_O = 20V(p\text{-}p)$	±0.3%	±0.2%	**	**
I_Z input	$kI_Z = +1.0$ to $+10.0V$	±0.5%	*	*	*
Feedthrough					
X input	$kI_Z = +10V$, $V_X = 20V(p\text{-}p)$, $V_Y = 0$, f = 50Hz	150mV(p-p) max [50mV(p-p) typ]	80mV(p-p) max [30mV(p-p) typ]	40mV(p-p) max [20mV(p-p) typ]	80mV(p-p) max [30mV(p-p) typ]
Y input	$kI_Z = +10V$, $V_Y = 20V(p\text{-}p)$, $V_X = 0$, f = 50Hz	100mV(p-p) max [30mV(p-p) typ]	60mV(p-p) max [25mV(p-p) typ]	30mV(p-p) max [15mV(p-p) typ]	60mV(p-p) max [25mV(p-p) typ]
X or Y vs. Temperature	T_{min} to T_{max}	2.0mV(p-p)/°C	1.0mV(p-p)/°C	0.5mV(p-p)/°C	1.0mV(p-p)/°C
INPUT SPECIFICATIONS					
Input Resistance					
X input, common mode	$V_{cm} = \pm10V$	80MΩ‖8pF	*	*	*
X input, differential	$V_{diff} = \pm10V$	10MΩ‖4pF	*	*	*
Y input	$V_Y = \pm10V$	6MΩ‖4pF	*	*	*
Sense input		36kΩ	*	*	*
Input Bias Current					
X, Y inputs	$kI_Z = +10V$ dc	3μA	4μA max [1.5μA typ]	2μA max [1μA typ]	4μA max [1.5μA typ]
	T_{min} to T_{max}	10μA	8μA	4μA	8μA
Sense input		±10μA	±15μA max [±5μA typ]	**	**
	T_{min} to T_{max}	±30μA	±25μA	**	**
Input Offset Current					
X inputs	$kI_Z = +1.0$ to $+10.0V$	±0.3μA	±0.1μA	**	**
Common Mode Rejection					
X inputs	$V_{cm} = \pm10V$ dc	40dB min	40dB min [60dB typ]	60dB min [75dB typ]	40dB min [60dB typ]
Scaler Current I_Z					
C input	$kI_Z = +10V$ dc	300μA min [500μA max]	*	*	*
Input Voltage					
V_X, V_Y, V_{sense}	T_{min} to T_{max} for rated accuracy	±10V	*	*	*
V_X/kI_Z	T_{min} to T_{max} for rated accuracy	±1.0V	*	*	*
Null Input Voltage	max required to trim				
Y_O, V_{OS}		±15V max [±5V typ]	±10V max [±3V typ]	**	**
X_O		+15V max [+12.5V min]	*	*	*
DYNAMIC SPECIFICATIONS					
Small Signal, Unity Gain		1.0MHz	*	*	*
Full Power Bandwidth		750kHz	*	*	*
Slew Rate		45V/μs	*	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*	*
Small Signal 1% Vector Error	0.5° phase shift	5kHz	*	*	*
Settling Time	±10V step	1μs to 2%	*	*	*
Overload Recovery		2μs to 2%	*	*	*
OUTPUT AMPLIFIER SPECIFICATIONS					
Output Impedance	Open Loop	100Ω	*	*	*
Output Voltage Swing	T_{min} to T_{max} $R_L \geqslant 2k\Omega$, $C_L \leqslant 1000pF$	±10V min [±13V typ]	*	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*	*
Output Offset Voltage		trimmable to zero	*	*	*
vs. Temperature	T_{min} to T_{max}	0.7mV/°C	*	1.0mV/°C max	2.0mV/°C max
POWER SUPPLY SPECIFICATIONS					
Supply Voltage	rated performance	±15V	*	*	*
	operating	±15V to ±18V	±10V to ±18V	**	±10V to ±22V
Supply Current	quiescent	6.5mA max [5mA typ]	*	*	*
Power Supply Rejection	*includes* effects of recommended null pots				
Accuracy		±0.5%/%	*	*	*
Output Offset		±10mV/%	*	*	*
Scale Factor	internal reference	±0.1%/%	*	*	*
Feedthrough		±10mV/%	*	*	*

NOTES:
1. Max input voltage is zero when supplies are turned off.
2. See also Figure 6.

*Specifications same as AD531J.
**Specifications same as AD531K.

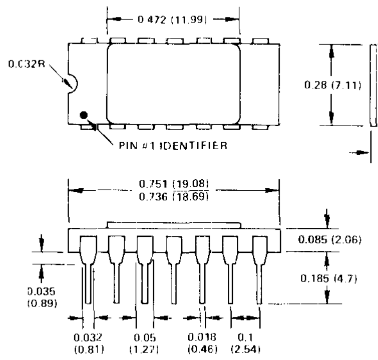
Specifications subject to change without notice. Ordering Guide on next page.

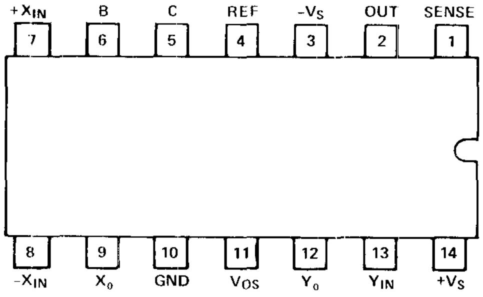
PIN CONFIGURATION & DIMENSIONS

Dimensions shown in inches and (mm).

AD531D

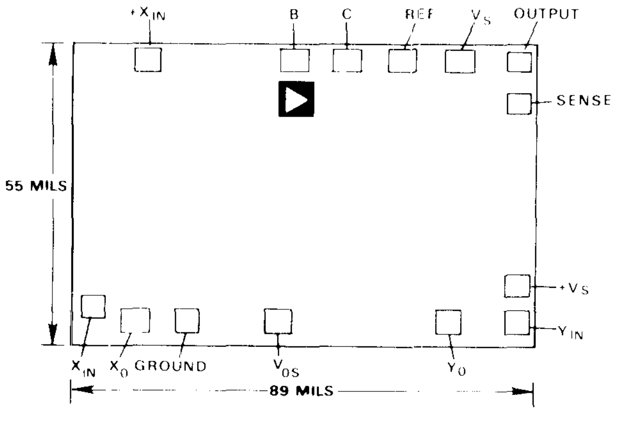
TO-116





BONDING DIAGRAM

The AD531 is available in chip or wafer form, fully tested at +25°C. Because of the critical nature of using unpackaged devices, it is suggested that the factory be contacted for specific information regarding price, delivery and testing.



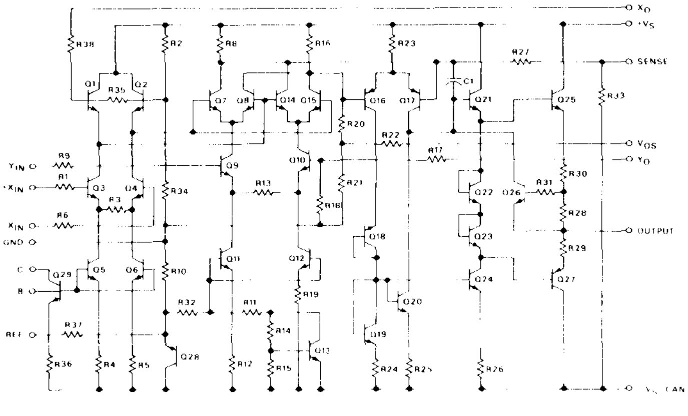


Figure 1a. AD531 Schematic Diagram

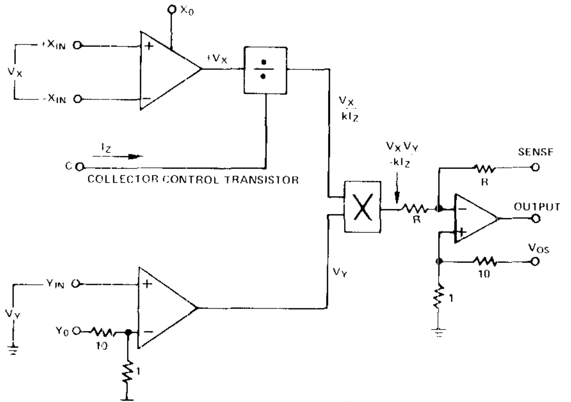


Figure 1b. AD531 Functional Diagram

FUNCTIONAL DESCRIPTION

The basic operation and terminal limits of the AD531 can be derived from the block diagram and complete circuit schematic shown in Figure 1.

The V_X input is fed to a high impedance differential amplifier featuring low distortion and good common mode rejection. The gain of the X channel is set by the externally programmed current source I_Z giving the transfer function V_X/kI_Z within the terminal limits $0 \leqslant V_X/kI_Z < \pm 2.5$ (where k is dimensioned in ohms). Voltage offset is adjusted out at X_O. The V_Y input is fed to one input of a high impedance differential amplifier; the other input being used to null its voltage offset.

The product of the V_X/kI_Z and V_Y terms is resolved in the multiplying cell using Gilbert's linearized transconductance technique. The built-in op amp converts the output of the multiplier cell to the more useful low impedance, single-ended voltage output format. The feedback sense pin provides for load sensing or special applications.

ORDERING GUIDE

ORDER NUMBER	MAX. ERROR	TEMP. RANGE
AD531JD	±2.0%	0 to +70°C
AD531KD	±1.0%	0 to +70°C
AD531LD	±0.5%	0 to +70°C
AD531SD	±1.0%	−55°C to +125°C
AD531S/883	±1.0%	−55°C to +125°C

TRIM PROCEDURE

The standard circuit configuration for computing the function $V_X \cdot V_Y / V_Z$ is shown in Figure 2. The scale factor circuitry has been refined over that shown in Figure 5(a) by adding a Z_O adjust to optimize the dynamic range in V_Z. [For fixed scale applications, the I_Z input can be derived with the circuit shown in Figure 5(b).]

The trim procedure outlined here is designed to provide an optimum set of adjustments with full scale input-output signals of ±10V and a 30dB dynamic range in V_Z (= kI_Z). For different ranges in inputs and/or scale factor (fixed or dynamically variable), the procedure should be modified to reflect the real application (e.g.; for fixed gain applications, trim the AD531 with kI_Z equal to the desired scale factor). Remember too that for best accuracy, V_X is restricted to $V_X/kI_Z \leqslant 1.0$.

The simplified circuit in Figure 3 offers one approach for trimming the AD531. The test equipment requirements are quite simple, a precision +10.0V dc reference, a signal generator for 20V(p-p) at 10Hz, a CRO, and 10kΩ and 15kΩ resistors to offset the output for the Gain and Z_O adjustments.

Three switches set the conditions for the inputs as noted in the Trim Table, while a fourth switch is used to connect the output to the CRO. Note that the CRO display is a cross-plot between the input 20V(p-p) sine wave generator and the resultant error signals at the output.

While the offset errors will be around zero, the Gain and Z_O adjustments must be made with V_{out} at full scale (±10V). The 10kΩ and 15kΩ resistor divider to the −15V supply is provided to bias the AD531 output to the CRO so that these adjustments can be accurately made around zero volts on the CRO.

Referring to the Trim Table in Figure 4, the output voltage offset V_{OS} is first adjusted to bring the output within normal range on the CRO. Note that the response to $kI_Z < 0V$ (negative half of sine wave) should be ignored as the scale input (I_Z) is bounded by the diode resistor clamp circuit at the output of the op amp. In the next steps, the voltage offset of the Y_{in} and X_{in} amplifiers are zeroed to minimize X_{in} and Y_{in} feedthrough respectively. In both cases, adjust for minimum average (p-p) ac response, ignoring the dc error. The output voltage offset V_{OS} is then readjusted to obtain the best average about dc over the range in kI_Z of interest. Again, ignore response for $kI_Z < 0V$. The Gain and Z_O pots are now adjusted to obtain the best average performance about 10V (zero volts on the offset CRO display) for the desired range in V_Z. For critical applications, recheck the feedthrough and offset adjustments.

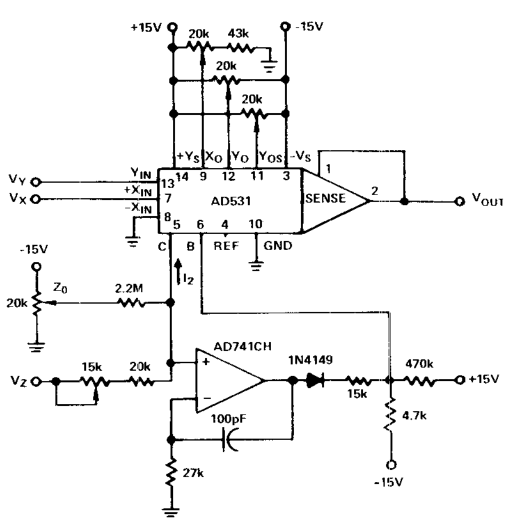


Figure 2. Trim Pot Connections

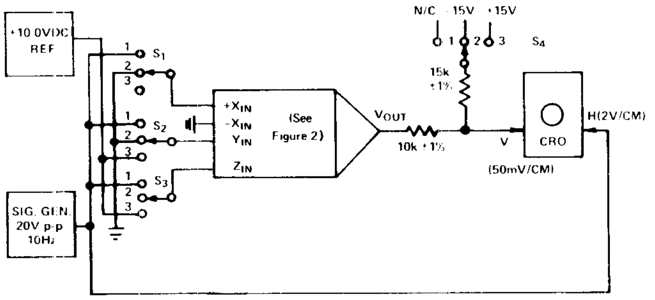


Figure 3. Test Setup

Finally, full scale gain can be fine adjusted to obtain the best average performance in the quadrants of interest. This is done by equalizing the full scale errors between the lowest and highest gain quadrants.

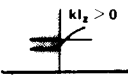
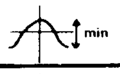
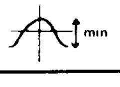
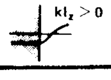
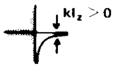
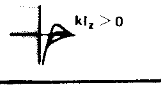
Step	$S_1/(V_X)$	$S_2/(V_Y)$	$S_3/(kI_Z = V_Z)$	S_4/(CRO)	Adjust	CRO Pattern
1	2/(0V)	2/(0V)	1/(20V p-p)	1/(Direct)	V_{OS}: Adjust for best avg dc error for $kI_Z > 0$.	
2	1/(20V p-p)	2/(0V)	3/(+10V)	1/(Direct)	Y_O: Min (p-p) ac response	
3	2/(0V)	1/(20V p-p)	3/(+10V)	1/(Direct)	X_O: Min (p-p) ac response	
4	2/(0V)	2/(0V)	1/(20V p-p)	1/(Direct)	V_{OS}: Adjust for best avg dc error for $kI_Z > 0$.	
5[1]	1/(20V p-p)	3/(+10V)	1/(20V p-p)	2/(Offset)	Gain: Min error at +10V (scope result about zero)	
6[2]	1/(20V p-p)	3/(+10V)	1/(20V p-p)	2/(Offset)	Z_O: Best accuracy for low value of kI_Z over range of interest	

Figure 4. Trim Table

NOTES:

[1] The small error introduced by the divider network to -15V (or +15V for four quadrant scaling) can be removed by fine trimming the divider or the supply to obtain 0V out with +10V (or -10V) in, or by calibrating the device separately at full scale. To optimize gain in two or more quadrants split the errors equally between the highest and lowest gain quadrants of interest.

[2] Step 6 may be omitted for Fixed Gain applications.

GAIN OR SCALE FACTOR ADJUST ($V_Z = kI_Z$)

The principle advantage the AD531 offers over standard transconductance multipliers is its dynamically adjustable gain or scale factor without significant degradation in overall bandwidth throughout its dynamic range. This feature allows for the implicit solution of many complex functions, such as true rms-to-dc conversion and Absolute Value, which will be discussed later under Applications. While standard multipliers can be configured as dividers or AGC loops by connecting the multiplying element in the feedback of an op amp, they are still restricted to the computation of two variables. Further, accuracy and bandwidth are adversely affected with decreasing denominator.

In the AD531 the gain through the X_{in} amplifier is inversely proportional to its "common mode" current, I_r. Thus, to achieve a variable scale factor, a control transistor Q_{29} has been provided to force this current to be equal to an externally derived scaler current I_Z, as shown in Figure 5(c).

FIXED SCALE FACTOR

For fixed scale applications the current I_Z can be set by shorting the Base-Collector (B and C) terminals of the control transistor Q_{29} together and connecting them to the built-in voltage reference V_{ref} through an external gain setting resistor as shown in Figure 5(b). The nominal resistor value is given by $R = [(V_{ref} - V_{BE})/I_Z] - 15k\Omega$, and its required adjustment range by variations in I_Z (= 300 to 500μA, full scale).

Alternatively, the scaling current can be derived by connecting the B and C terminals to ground through an adjustable resistor. This approach improves the overall T.C. in I_Z, but requires a well-regulated $-V_S$ supply.

VARIABLE SCALE FACTOR

For variable gain applications, the control transistor's collector current I_Z can be derived from a programmable current source, such as the voltage-to-current op amp circuit shown in Figure 5(a). The current I_Z is determined by V_Z/R, with the value for R set by both variations in I_Z (= 300 to 500μA, full scale) and the desired full scale response to V_Z. Note that V_Z must be unipolar and positive valued as shown. As the control transistor Q_{29} is inside the amplifier loop, the base of the transistor is servoed by the op amp to support the programmed collector current I_Z.

The non-inverting input of the op amp is used as the summing point because of the inherent inversion from base to collector in the reference transistor. A stabilizing capacitor (100pF) is recommended because there is active gain with Q_{29} inside the loop. Resistors R_1, R_2, R_3 and diode CR_1 are used to both level shift the op amp output to the nominal $-13V$ level at the base of the reference transistor and to prevent op amp latchup.

USER'S GUIDE TO PERFORMANCE SPECIFICATIONS

A clear understanding of the various error sources of the AD531 will assist the user in obtaining optimum performance under his particular operating conditions. The principle sources of error are feedthrough, nonlinearity, output offset, and scale factor (or gain) when using the internally derived reference. In addition, their variations attributable to changes in power supply voltage, operating frequency, and ambient temperature must be considered.

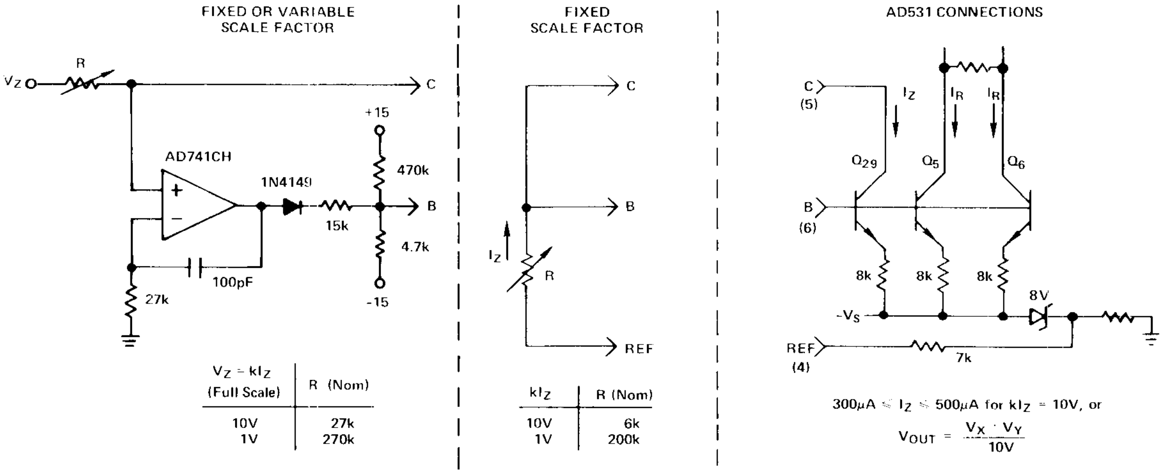
ACCURACY

Accuracy is defined in terms of total error at +25°C with the rated power supply. The value specified is in percent of full scale and includes X_{in} and Y_{in} nonlinearities, feedthrough, and quadrant-to-quadrant scale factor error with I_Z adjusted to full scale ($kI_Z = 10V$). To this must be added such application dependent error terms as power supply rejection, common mode rejection and temperature coefficients. (Worst-case error over temperature is specified for the AD531L and AD531S however). Total expected error is the rms sum of the individual components, since they are uncorrelated.

As the denominator is decreased ($kI_Z < 10V$), an additional error is introduced due to I_Z nonlinearity and feedthrough effects. The former is trimmed at Z_O; the latter at X_O (optional). Finally, additional nonlinearity is introduced as the ratio V_X/kI_Z is made greater than unity. The limiting value is about ±2.5 where the X-input amplifier saturates.

NONLINEARITY

While errors due to output offset, feedthrough and gain can be substantially reduced by external adjustments, nonlinearity remains a basic irreducible limitation to achievable accuracy. Nonlinearity is measured by setting two of the three inputs V_X, V_Y, kI_Z (actually V_X/kI_Z) to full scale and applying a low frequency sine wave of full scale amplitude to the third. The ac output is nulled against the ac input, the gain fine adjusted, and the reduced peak-to-peak error voltage is then a measure of nonlinearity referred to a best straight line.



$V_Z = kI_Z$ (Full Scale)	R (Nom)
10V	27k
1V	270k

kI_Z	R (Nom)
10V	6k
1V	200k

$300\mu A \leq I_Z \leq 500\mu A$ for $kI_Z = 10V$, or

$$V_{OUT} = \frac{V_X \cdot V_Y}{10V}$$

Figure 5. Scale Factor Adjustments

Typical curves for V_X and V_Y nonlinearity are shown in Figure 6. However, the actual wave shapes for each can vary significantly from that shown. The V_X/kI_Z nonlinearity is shown in Steps 5 and 6 of the trim procedure section.

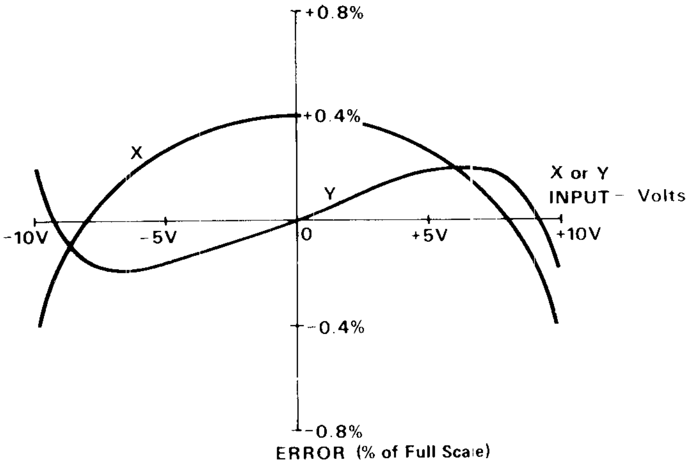


Figure 6. Typical X and Y Nonlinearity for $kI_Z = 10V$

FEEDTHROUGH

Ideally, the output of a multiplier should be zero when either of the inputs in the numerator is zero, regardless of the signals applied to any of the remaining inputs. Actually there is usually a small residual output that is proportional to the varying inputs and this error is defined as feedthrough.

Low frequency feedthrough is composed of two components, one of which can be trimmed to zero with two external null pots. The trimmable feedthrough error is attributable to the dc voltage offsets of the input differential amplifiers, and can be nulled at X_O and Y_O. (However, as X_O is used to adjust both V_Y and kI_Z feedthrough, the user may have to accept a compromise null point for best performance.)

The untrimmable component is due to the nonlinearity of the multiplier cell, and is the value shown in the electrical specifications. Figure 7 shows typical low frequency feedthrough performance before and after nulling.

At high frequencies, the circuit acts as if there were capacitive coupling between each input and the output. Therefore, at some corner frequency, feedthrough will rise with increasing frequency at 6dB/octave as illustrated in Figure 8, until other shunt capacitance begins to attenuate this effect. This high frequency feedthrough will primarily consist of the fundamental component and will vary in proportion to the nonzero input signal(s).

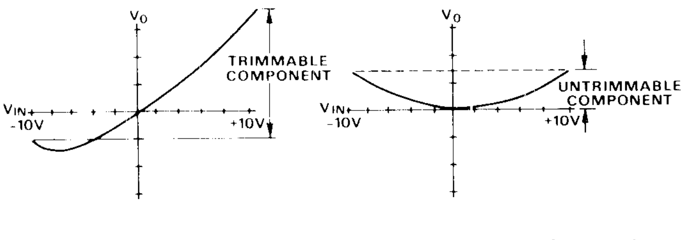


Figure 7. Typical X or Y Feedthrough Before and After Nulling

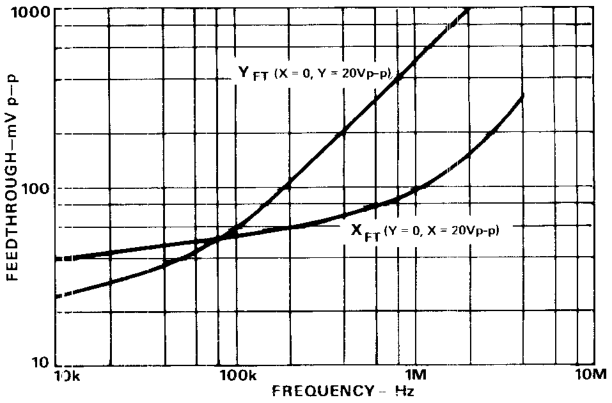


Figure 8. Typical Feedthrough vs. Frequency, $kI_Z = 10V$

OUTPUT OFFSET

This error obviously has the greatest percentage effect on accuracy for low level output signals. An external trimming pot is used with the AD531 to adjust the initial offset to zero. Output offset drift with temperature and supply voltage variation becomes the limit in accuracy for low level dc output signals.

SCALE FACTOR

The scale factor sets the gain of the multiplier and is represented by $1/kI_Z$. The magnitude and stability of the scaler are determined by the external circuitry or the internal temperature compensated reference source (drift 0.02% typ), if used. Specified overall performance assumes zero error contribution from this source.

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD531 in the multiplier mode typically exhibits a 3dB bandwidth of 1MHz and rolls at 6dB/octave thereafter, governed by the output op amp internal compensation. Response through all inputs is essentially identical and is shown in Figure 9 below.

Stable operation is maintained with capacitive loads up to 1000pF in all modes. Higher capacitive loads can be driven if a 100Ω resistor is used in series with the output for isolation.

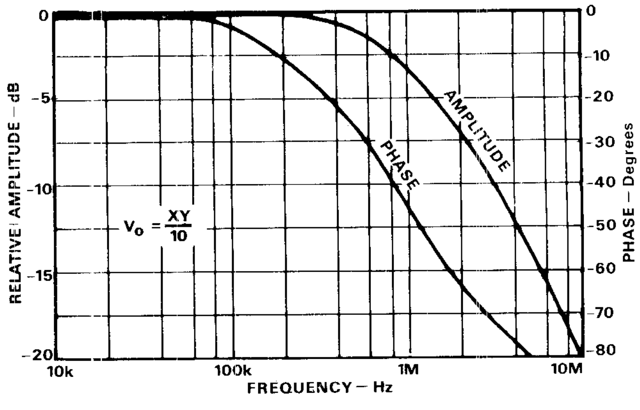


Figure 9. Typical Closed Loop Frequency and Phase Response

For some applications, the instantaneous (sometimes called the absolute) error between the output and input signals may be of primary concern. In this case, vector errors due to phase shift accumulate much more rapidly as a function of frequency than do amplitude or scaler errors. This follows since a phase shift of only 0.57° will cause a vector error of 1%, whereas the amplitude error is only 0.005% at this phase shift. The relationship between these errors is illustrated in the vector diagram of Figure 11.

POWER SUPPLY CONSIDERATIONS

Although the AD531 is tested and specified with ±15 volt supplies, the K and L versions may be operated at any supply voltage from ±10V to ±18V and the S version from ±10V to ±22V with little affect on overall performance. The input and output signals must be reduced proportionately to prevent saturation at supply voltages below ±15V (see Figure 10).

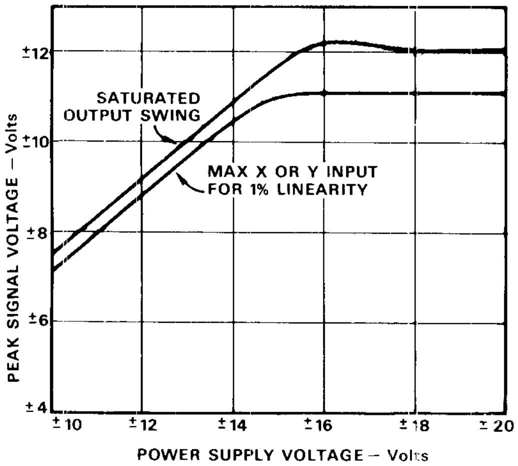


Figure 10. Typical Allowable Signal Swing vs. Supply Voltage, $kI_Z = 10V$

Power supply rejection figures are specified for accuracy, feedthrough, output offset and scale factor to enable the user to determine supply regulation requirements commensurate with his operating conditions. All the specifications include effects of the recommended null pots.

NOISE CHARACTERISTICS

All AD531's are screened on a sampling basis, both at the wafer stage and at final test, to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency characteristics are shown in Figure 12.

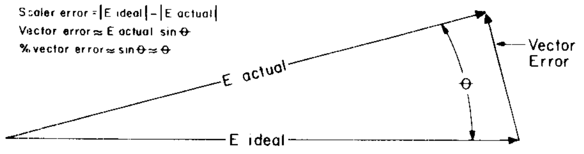


Figure 11. Relationship of Dynamic Errors

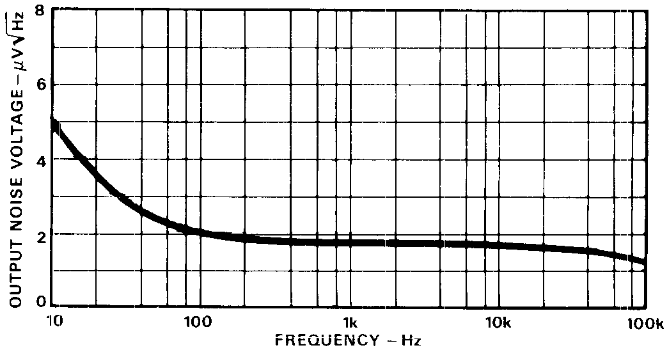


Figure 12. Typical Spot Noise vs. Frequency

APPLYING THE AD531

The differential input and variable gain or scale factor features of the AD531 bring new capability and flexibility to the design of multiplier-divider related circuits. The AD531 is especially well-suited to applications such as the AGC, True rms-to-dc Converter and Vector Computation circuits where the programmable gain feature allows for the implicit solution of these functions over a wide dynamic range of inputs.

The simple multiplier shown in Figure 13 demonstrates how the scale factor kI_Z can be set with a resistor. For squaring applications, simply short Y_{in} to either $+X_{in}$ or $-X_{in}$ (grounding the other) according to the desired polarity at the output. The I_Z linearity adjustments Z_O can be omitted for both cases. The Y_O feedthrough can also be eliminated for the squaring application as a single input offset adjustment is sufficient.

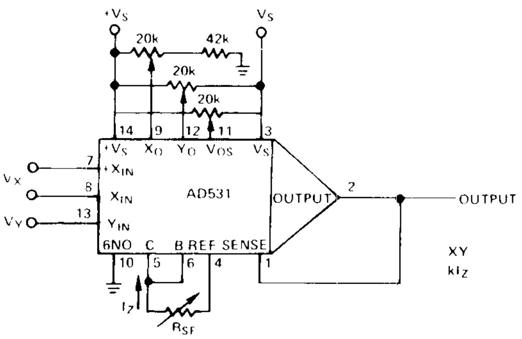


Figure 13. Multiplier/Squarer Connection

In Figure 14 the AD531 is combined with a simple filter to obtain the true rms value of an ac input signal. Unlike averaging circuits that are calibrated to read rms with sine wave inputs, accuracy is not degraded here by wave shape provided that the rms value is scaled to keep $V_X/kI_Z \leqslant 2.5$ and $V_A \leqslant 10V$ peak. The circuit is accurate for dc signals and ac inputs within the bandwidth $(100/2\pi RC) \leqslant f \leqslant 100kHz$. By scaling V_{out} = 10V dc for a ±10V dc input, this circuit will give a direct rms reading for 100Hz to 100kHz sine wave inputs from 0.2V to 7.0V peak. Larger input values can saturate the output of the multiplier.

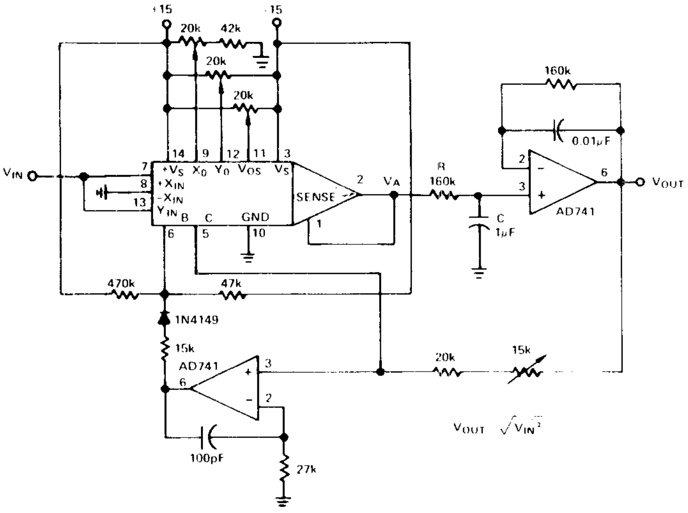


Figure 14. True rms Circuit

The amplitude stabilizing circuit of Figure 15 operates by rectifying the supposedly constant output signal, and comparing it with the voltage at the set level pot. The comparator output is then applied as the control signal (V_Z) to the AD531. The Y-input is biased at near full scale and the input is connected at $+X_{in}$. The X and Y feedthrough adjustments can be eliminated and all of the offset adjusted out at V_{OS}. Unlike standard multipliers connected as AGC loops, the bandwidth of the AD531 is not appreciably reduced with low level denominators. Thus, this circuit can regulate V_{out} to 3V(p-p) ±2% for inputs from 0.4V(p-p) to 6.0V(p-p) from 30Hz to 400kHz.

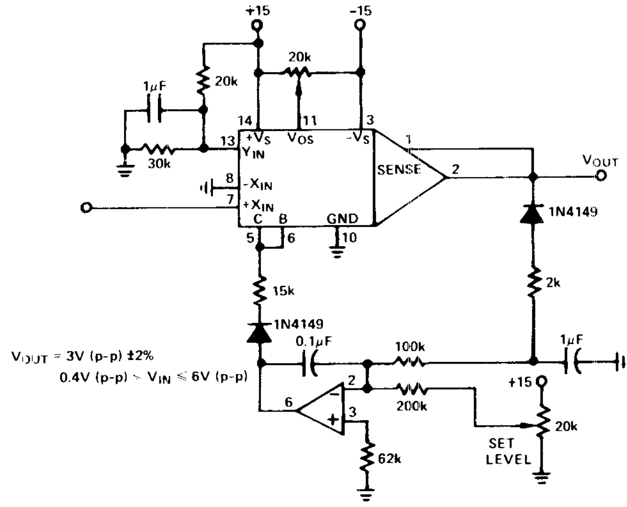


Figure 15. Precision AGC

The Vector Computation Circuit in Figure 16 uses two inexpensive op amps with the AD531 to derive the square root of the sum of the squares. The output of the AD531 is $V_A{}^2/V_Z$, which is summed with V_B in the output amplifier. As $V_Z = V_{out} + V_B$, the output will be servoed to achieve the identity . . . .

$$V_{out} = \sqrt{V_A{}^2 + V_B{}^2}$$

Operation is restricted to two quadrants, as V_B must be positive. Calibration is simplified by adjusting R_1 with V_A = 10V and V_B = 0V, and then adjusting R_2 with some mid value of V_A and V_B. The Z_O pot is adjusted for accuracy with low level inputs.

Of interest, connecting V_A to $-X_{in}$ and grounding $+X_{in}$ will result in the identity........

$$V_{out} = \sqrt{V_B{}^2 - V_A{}^2}$$

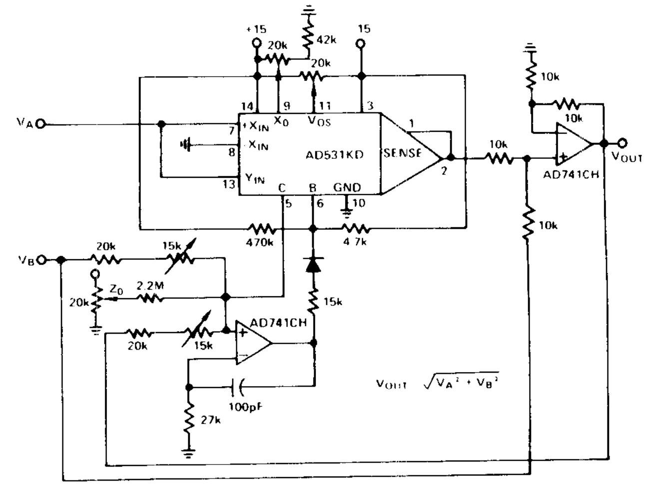


Figure 16. Vector Computer