3½ Digit BCD Monolithic CMOS Digitally Controlled Potentiometer

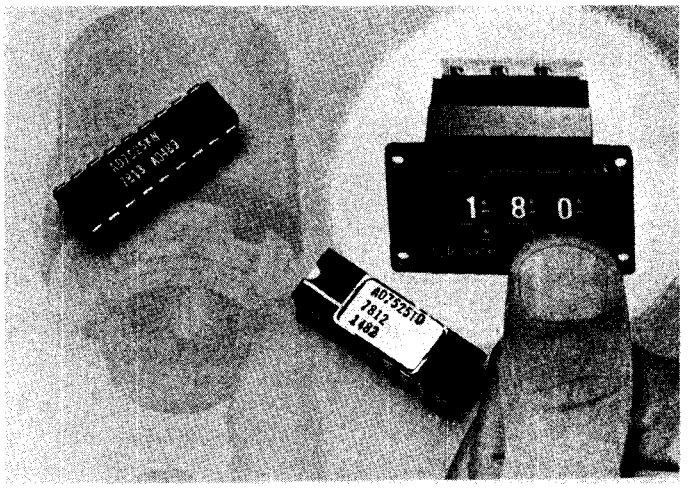
AD7525

FEATURES

Resolution: 3 1/2 Digit BCD (1999 Counts)
Accuracy: ±0.2%
Excellent Repeatability Accuracy
Low Power Dissipation

APPLICATIONS

Thumbwheel Switch Voltage Dividers
Digitally Controlled Gain Circuits
Digitally Controlled Attenuators
BCD Multiplying DAC's
Low Power Converters



GENERAL DESCRIPTION

The AD7525 is a monolithic CMOS 3½ digit BCD digitally controlled potentiometer designed for precision incremental voltage-divider applications.

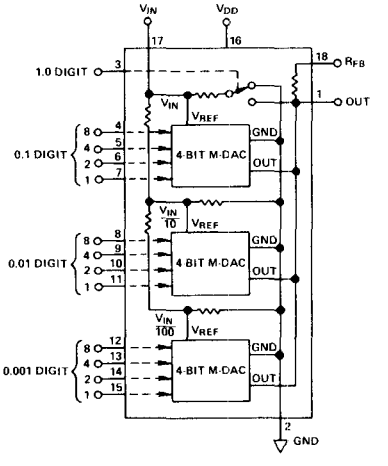
With the addition of an external op amp, the output can be digitally controlled from 0 to 19.99V in 10mV increments with a 10V input.

AC or DC voltage up to ±25V can be applied to the input providing high application flexibility in fields such as audio gain control, etc.

Digitial control, excellent repeatability and 0.2% accuracy make the AD7525 an ideal replacement for 10-turn potentiometers or thumbwheel switch voltage dividers using discrete resistor networks.

Packaged in an 18-pin DIP, the AD7525 uses an advanced CMOS fabrication process combined with wafer laser trimming.

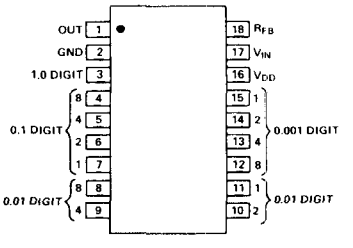
FUNCTIONAL DIAGRAM



ORDERING INFORMATION

Temperature Range and Package		
Plastic 0 to +70°C	**Ceramic -25°C to +85°C**	**Ceramic -55°C to +125°C**
AD7525KN	AD7525BD AD7525BD/883B	AD7525TD AD7525TD/883B

PIN CONFIGURATION



SPECIFICATIONS (V_{DD}=+15V; V_{PIN1} = 0V; V_{IN} = +10V unless otherwise stated)

PARAMETER	T_A = +25°C	T_A = Operating Temperature Range	CONDITION
ACCURACY			
Resolution[1]	1 part in 2000	1 part in 2000	
Absolute Accuracy Error[2]	±0.2%V_{IN} max	±0.3%V_{IN} max	BCD 0000 to 1999
DYNAMIC PERFORMANCE			
Switching Time	1μs max[3]	1μs max[4]	V_{IN} = +5V, R_{OUT} (pin 1) = 100Ω, Digital Inputs = V_{IL} to V_{IH} or V_{IH} to V_{IL} V_{PINS} measured from 10% to 90%
Feedthrough Error	±0.05%V_{IN} max[4]	±0.1%V_{IN} max[4]	V_{IN} = ±10V, 20kHz sinewave
ANALOG INPUT			
Input Resistance (pin 17)[5]	2kΩ min/10kΩ max	2kΩ min/10kΩ max	
V_{IN} Range (max recommended)	±10V max	±10V max	
ANALOG OUTPUT			
Output Capacitance			
C_{OUT} (pin 1)	60pF max[4]	60pF max[4]	Digital Inputs = BCD 0000
	200pF max[4]	200pF max[4]	Digital Inputs = BCD 1999
R_{FB} Resistance (pin 18 to pin 1)[5]	8kΩ min/32kΩ max	8kΩ min/32kΩ max	
DIGITIAL INPUTS			
Input HIGH Voltage			
V_{IH}	+14.5V min	+14.5V min	
Input LOW Voltage			
V_{IL}	+0.5V max	+0.5V max	
Input Leakage Current	±1μA max	±10μA max	Digital Input = 0V or V_{DD}
Input Capacitance	5pF max[4]	5pF max[4]	
Input Coding	3½ Digit BCD (1999 Counts)	3½ Digit BCD (1999 Counts)	
POWER SUPPLY			
V_{DD} Range	+5V to +17V	+5V to +17V	Functional with Degraded Performance
V_{DD}	+15V ±5%	+15V ±5%	Rated Accuracy
I_{DD}	500μA max	1mA max	Digital Inputs = V_{IL} or V_{IH}

NOTES:
[1] Commercial devices are sample tested over temperature.
[2] Absolute accuracy is measured using the AD7525 internal feedback resistor.
[3] AC parameter, sample tested at +25°C to ensure conformance to specification.
[4] Guaranteed, not tested.
[5] Thin film resistor temperature coefficient is approximately -300ppm/°C.

Specifications subject to change without notice.

CAUTION

1. ESD (electro-static discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.
2. Do not apply voltages more negative than GND or more positive than V_{DD} to any pin except V_{IN} (pin 17) and R_{FB} (pin 18).
3. The inputs of some IC amplifiers (especially high speed types) present a low impedance to V– during power sequencing. To prevent the AD7525 OUT terminal (pin 1) from exceeding –300mV (which causes catastrophic substrate current), a Schottky diode, HP5082-2811 or equivalent, is recommended. While not required for most amplifier types, provision for the diode should be made during layout. The diode should be connected between OUT (pin 1) and GND (pin 2) as shown in Figure 4, page 141S.

ABSOLUTE MAXIMUM RATINGS

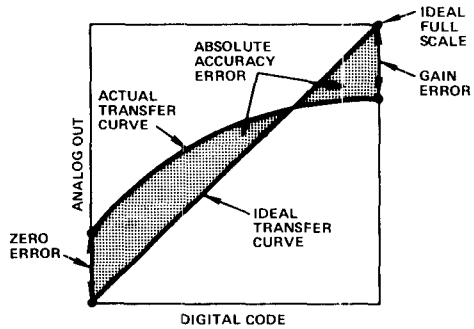
(T_A = 25°C unless otherwise noted)

V_{DD} (to GND)	–0.3V, +17V
V_{IN} (to GND)	±25V
R_{FB} (to GND)	±25V
Digital Input Voltage (to GND)	–0.3V to V_{DD}
V_{PIN1} (to GND)	–0.3V to V_{DD}
Power Dissipation (Package)	
Plastic (Suffix N)	
To +70°C	670mW
Derates above +70°C by	8.3mW/°C
Ceramic (Suffix D)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commercial Plastic (KN Version)	0°C to +70°C
Industrial Ceramic (BD Version)	–25°C to +85°C
Military Ceramic (TD Version)	–55°C to +125°C

TERMINOLOGY

SWITCHING TIME: In a D/A converter, the switching time is the time taken for an analog switch to change to a new state from the previous one. It includes delay time, and rise time from 10% to 90%, but does not include settling time, which is a function of the output amplifier used.

ABSOLUTE ACCURACY ERROR: Deviation of the actual transfer curve (uncalibrated) from the ideal transfer curve. It is expressed as a percentage of the input voltage.



Absolute Accuracy Error

OUTPUT CAPACITANCE: Capacitance from OUT terminal (pin 1) to ground.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{IN} (pin 17) to OUT (pin 1) with all digital inputs LOW.

PRINCIPLES OF OPERATION

CIRCUIT DESCRIPTION

The AD7525, a 3½ digit BCD multiplying DAC, consists of a thin-film R/2R ladder, interquad voltage dividers and 13 N-channel MOS SPDT current steering switches. Most applications require the addition of only an external operational amplifier.

Referring to Figure 1, the "1.0 Digit" is a 1-bit multiplying DAC (composed of SW_1 and R_1) while the 0.1, 0.01, and 0.001 digits are 4-bit multiplying DAC's (DAC1, DAC2, and DAC3) connected by 10:1 dividers (composed of R_{IN2}, R_2, R_3 and R_{IN3}, R_4, R_5.

DAC1 is expanded to show the R/2R ladder and switch network. With input voltage V_{IN}, the currents in each shunt arm are (starting at the left) $V_{IN}/2R$, $V_{IN}/4R$, $V_{IN}/8R$ and $V_{IN}/16R$. A logic ONE applied to a digital input steers that shunt arm's current to OUT, while a logic ZERO steers the current to GND.

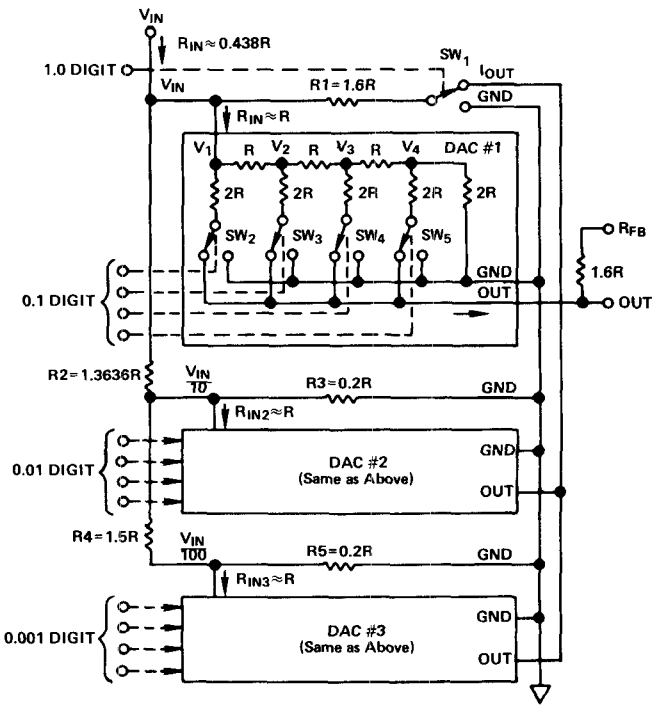


Figure 1. AD7525 Circuit Diagram

EQUIVALENT CIRCUIT

As shown in Figure 2, the AD7525 is a digitally controlled π-network attenuator with signal input "V_{IN}" (pin 17), signal output "OUT" (pin 1), signal common "GND" (pin 2) and digital control "BCD input" (pins 3–15).

With OUT (pin 1) terminated at op amp virtual ground and R_{FB} (pin 18) connected to the op amp output, the nominal transfer equation is:

$$V_{OUT} = -V_{IN}\,BCD$$
$$\text{where } 0.000 \leqslant BCD \leqslant 1.999$$

Table 1 shows the various circuit elements of Figure 2 as a function of the BCD input (where applicable). BCD code dependent elements are shown connected by dotted lines in Figure 2.

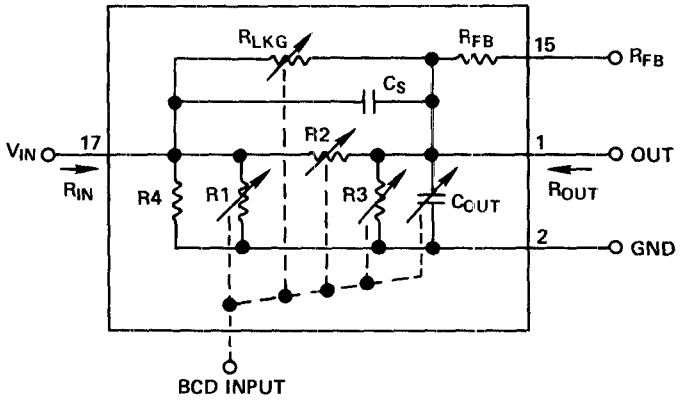


Figure 2. Functional Equivalent Circuit

OUTPUT AMPLIFIER CONSIDERATIONS

Amplifier Offset

From Table 1, the output resistance at OUT (pin 1) is code dependent, varying between ∞ to 0.35 R_{LDR}. For a fixed feedback resistor of value 1.6 R_{LDR} (Figure 3), the output error for a fixed amplifier offset (V_{OS}) is:

$$V_{ERROR} = \left(1 + \frac{R_{FB}}{R_{OUT}}\right) V_{OS}$$

Case 1: ($R_{OUT} = \infty$)

$$V_{ERROR} = \left(1 + \frac{R_{FB}}{\infty}\right) V_{OS}$$

$$V_{ERROR} = V_{OS}$$

Case 2: ($R_{OUT} = 0.35\,R_{LDR}$)

$$V_{ERROR} = \left(1 + \frac{1.6\,R_{LDR}}{0.35 R_{LDR}}\right) V_{OS}$$

$$V_{ERROR} = (1 + 4.6)V_{OS} = 5.6\,V_{OS}$$

Cases 1 and 2 show that amplifier offset in conjunction with a changing output resistance at OUT (pin 1) create nonlinearity error, in addition to a simple offset term.

It is therefore recommended that amplifier initial offset be adjusted to less than 100μV (as measured between the amplifier input terminals). The offset voltage over the temperature range of interest should not exceed 250μV.

It is important to realize that offset is caused by including the usual bias current compensation resistor in the amplifier noninverting terminal. This should not be included; rather, the amplifier should have a bias current which is low over the temperature range of interest. Bias current causes "output offset" of magnitude $(I_B)R_{FB}$.

High Frequency Amplifiers

R_{FB} and C_{OUT} create a phase lag in the output amplifier's feedback circuit. This phase lag, in conjunction with the amplifier's phase lag, may cause ringing or oscillation. When using a high speed amplifier, shunting the amplifier input to output with 5–20pF of feedback capacitance ensures stability.

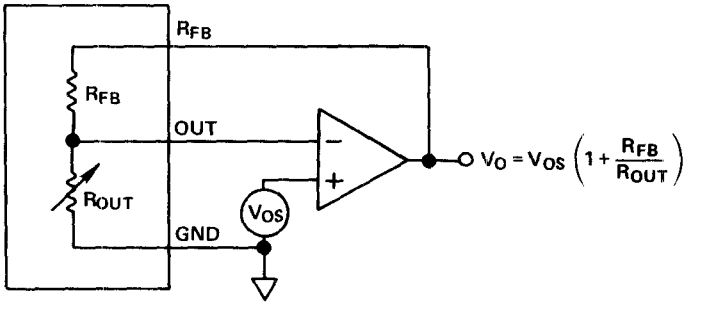


Figure 3. Noise Gain Equivalent Circuit

CIRCUIT ELEMENT	VALUE
R_{IN} (pin 17)	$R_{IN} = R_1 \parallel R_2 \parallel R_4 = 0.438 R_{LDR}$ (note 1)
R_4	$R_4 = 0.838\,R_{LDR}$ (note 1)
R_1	$R_1 = R_{FB}\left(\frac{1}{BCD} - 0.5002\right)$ $0.000 \leqslant BCD \leqslant 1.999$
R_2	$R_2 = \frac{R_{FB}}{BCD}$ for $0.000 \leqslant BCD \leqslant 1.999$
R_{OUT} (pin 1)	Varies nonlinearly with input codes. Range ∞ to $0.35\,R_{LDR}$ (note 1) $R_{OUT} = R_2 \parallel R_3$
R_{IN}	$R_{IN} = 0.438\,R_{LDR}$ (note 1)
R_{LKG}	$R_{LKG} \approx 50M\Omega$ (note 2)
C_{OUT1}	$C_{OUT} \approx [(50pF)(BCD) + 30pF]$ $0.000 \leqslant BCD \leqslant 1.999$
C_S	$C_S \approx 0.2pF$ (package capacitance)

NOTES:
1. R_{LDR} is R/2R ladder characteristic resistance, min 5kΩ, max 20kΩ, typically 10kΩ.
2. 50MΩ corresponds to an OUT (pin 1) leakage of 200nA (as shown in specification table) and a V_{IN} of 10V.

Table 1. Equivalent Circuit Element Values

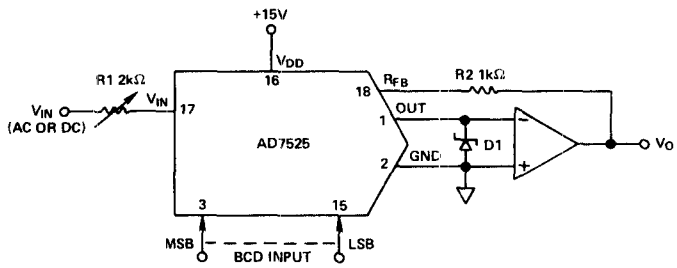


Figure 4. Digitally Controlled Attenuator Circuit

BCD INPUT					ANALOG OUTPUT	
Digital Input				Equivalent Decimal Input	V_O/V_{IN}	V_O
1.0	0.1	0.01	0.001			
1	1001	1001	1001	1.999	-1.999	$-1.999V_{IN}$
1	0000	0000	0001	1.001	-1.001	$-1.001V_{IN}$
1	0000	0000	0000	1.000	-1.000	$-1.000V_{IN}$
0	1001	1001	1001	0.999	-0.999	$-0.999V_{IN}$
0	0101	0000	0000	0.500	-0.500	$-0.500V_{IN}$
0	0000	0000	0000	0.000	0	0

Note 1:
For proper BCD coding, the 0.1 digit, 0.01 digit or 0.001 digit must not exceed BCD "9" (1001).

Table 2. Analog Input/Output Relationship vs. Digital Input

CALIBRATION PROCEDURE

Offset Adjustment:

1. Apply BCD code 0.000 (0 0000 0000 0000) to the AD7525 digital inputs.
2. Connect a high resolution, high impedance voltmeter between pins 1 and 2 of the AD7525.
3. Adjust amplifier's trimpot for minimum reading on the voltmeter (<100μV).

Gain Adjustment:

1. Apply BCD code 1.000 (1 0000 0000 0000) to the AD7525 digital input.
2. Apply +10V to the V_{IN} input of Figure 1.
3. Connect the voltmeter between V_O (amplifier output) and pin 2 of the AD7525.
4. Adjust R_1 until $V_O = -10V$.

APPLICATION – THUMBWHEEL SWITCH ATTENUATOR

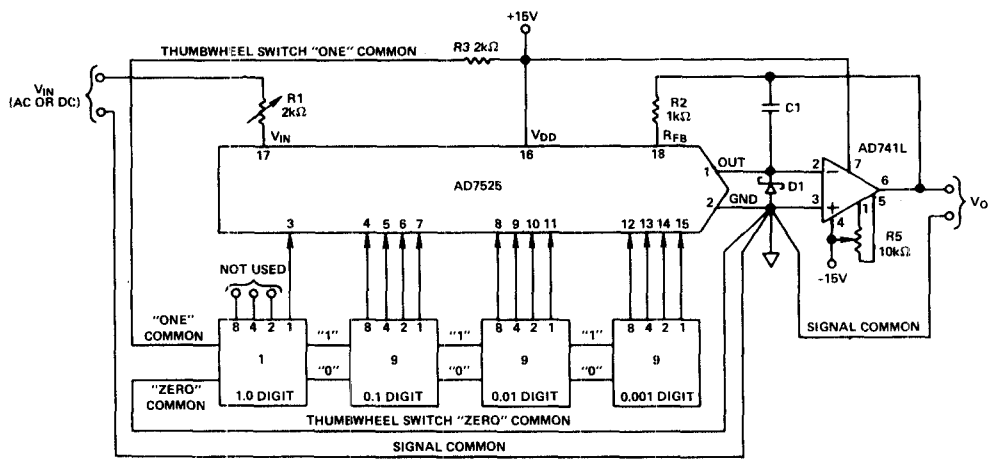


Figure 5. Thumbwheel Switch Attenuator

The circuit shown in Figure 5 is a precision voltage divider similar to 10-turn pots and thumbwheel switch incremental-voltage-divider assemblies. Advantages of the circuit are:

- ☐ Economy
- ☐ Low Output Impedance
- ☐ Resolution 0.1% V_{IN}
- ☐ Excellent Repeatability Accuracy
- ☐ 1000 - Count Overrange

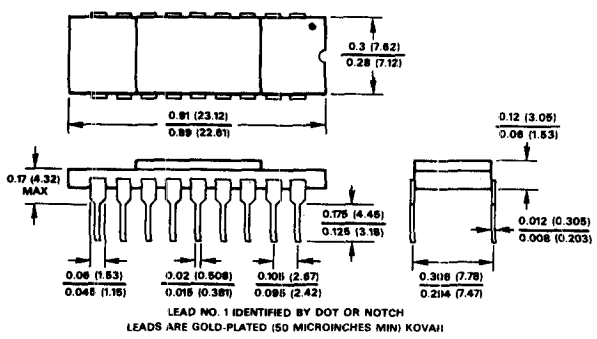
The BCD coded thumbwheel assembly applies BCD data to the AD7525 digital inputs. The switch assembly shown has single-pole-double-throw action, thus the BCD inputs are pulled either to +15V or GND (available from AMP, Harrisburg, PA; CHERRY, Waukegun, Illinois; or SAE, Santa Clara, California). Resistor R_3 limits current if make-before-break switches are used. SPST switch assemblies can be used, however appropriate pull-up or pull-down resistors must be used on each digital input, depending upon whether the switch coding is BCD or complementary BCD. This ensures each digital input has appropriate V_{IH} or V_{IL} levels applied.

Resistors R_1 and R_2 provide gain adjustment capability. R_5 is used to adjust the amplifier offset voltage (as measured between the amplifier input terminals) to less than 100μV. Diode D_1 (HP5082-2811) provides AD7525 output protection (see Caution note 3, page 139S).

MECHANICAL INFORMATION

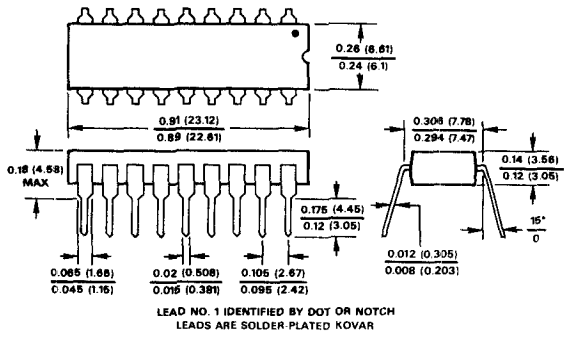
Dimensions shown in inches and (mm).

18 PIN CERAMIC DIP



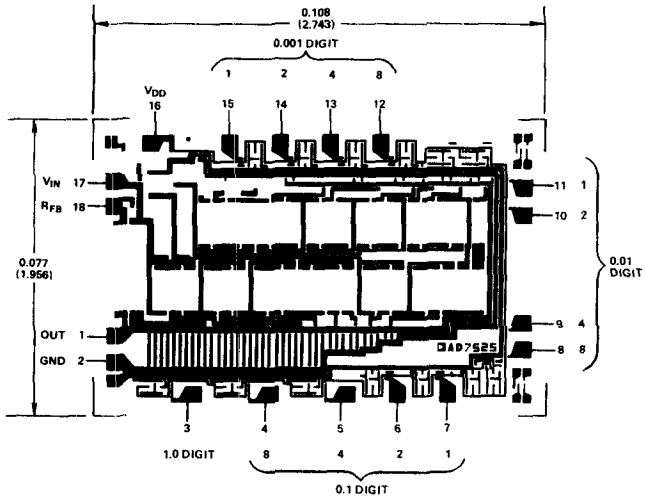
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD-PLATED (50 MICROINCHES MIN) KOVAR

18 PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER-PLATED KOVAR

BONDING DIAGRAM



NOTES:
1. PAD NUMBERS CORRESPOND TO PIN NUMBERS SHOWN IN PIN CONFIGURATION.
2. PAD 2 (GND) SHOULD BE BONDED FIRST TO MINIMIZE ESD HAZARDS.
3. PADS ARE 0.004in × 0.004in (0.102mm × 0.102mm).