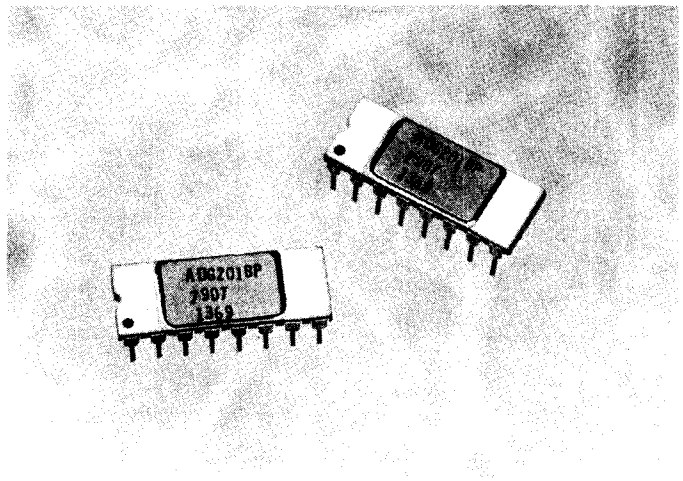
DI CMOS
Protected Quad SPST Analog Switch

ADG201

FEATURES
- Latch-Proof DI CMOS
- Overvoltage Proof to 25V Beyond Supplies
- Superior DG201 Replacement
- Break-Before-Make Switching Action
- Low R_{ON}: 80Ω
- Low Power Dissipation: 30mW max
- Direct TTL or CMOS Interfacing



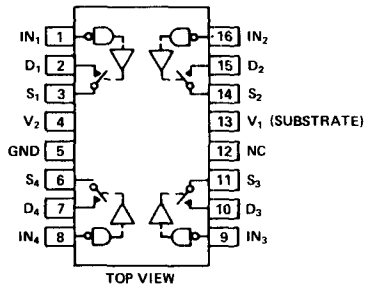
GENERAL DESCRIPTION

The ADG201 is a quad SPST analog switch. In the ON state, the switch conducts current in either direction, maintaining nearly constant ON resistance over its signal handling range. In the OFF state, it blocks voltages equal to the switch V+ and V– supplies. Switch action is break-before-make.

The digital inputs interface directly to TTL or CMOS logic over the full operating temperature range.

Fabricated with an advanced monolithic dielectrically-isolated CMOS process, the ADG201 is a superior plug in replacement for the DG201. ADG201 advantages over other designs include: lower R_{ON}, lower power dissipation, faster switching time, overvoltage protection (25V beyond power supplies), and latch-free operation.

PIN CONFIGURATION



TOP VIEW

SWITCH IS OPEN FOR LOGIC "1" (POSITIVE TRUE) INPUT

ORDERING INFORMATION

Commercial 0 to +70°C	Industrial -25°C to +85°C	Military -55°C to +125°
Plastic	Ceramic	Ceramic
ADG201CJ	ADG201BP	ADG201AP ADG201AP/883[1]

NOTE: "/883" version is 100% screened to MIL-STD-883, class B as per note 7, page 314S.

SPECIFICATIONS

CHARACTERISTIC		TYP[1] +25°C	MAX LIMITS AP SUFFIX -55°C[2]	AP SUFFIX +25°C	AP SUFFIX +125°C	BP, CJ SUFFIX -25/0°C[2]	BP, CJ SUFFIX +25°C	BP, CJ SUFFIX +85/70°C[2]	UNITS	TEST CONDITIONS[8] Unless Noted V_1 = +15V, V_2 = -15V, GND = 0V	
SWITCH											
$r_{DS(ON)}$	Drain-Source ON Resistance	60 40	80 80	80 80	125 125	100 100	100 100	125 125	Ω	V_D = 10V V_D = -10V	V_{IN} = 0.8V I_S = -1mA
$I_{S(OFF)}$	Source OFF Leakage Current	0.2 -0.2	500 -500	1 -1	500 -500	250 -250	5 -5	250 -250	nA	V_S = 10V, V_D = -10V V_S = -10V, V_D = 10V	V_{IN} = 2.4V
$I_{D(OFF)}$	Drain OFF Leakage Current	0.3 -0.3	500 -500	1 -1	500 -500	250 -250	5 -5	250 -250	nA	V_D = 10V, V_S = -10V V_D = -10V, V_S = 10V	V_{IN} = 2.4V
$I_{D(ON)}$[3]	Drain ON Leakage Current	0.1 -0.1	500 -500	1 -1	500 -500	250 -250	5 -5	250 -250	nA	V_D = V_S = 10V V_D = V_S = -10V	V_{IN} = 0.8V
INPUT											
I_{INH}	Input Current Input Voltage High		-10 10	-1 1	-10 10	-10 10	-1 1	-10 10	μA	V_{IN} = 2.4V V_{IN} = 15V	
$I_{IN(PEAK)}$[4]	Peak Input Current Required for Transition	NOT APPLICABLE[4]									
I_{INL}	Input Current Input Voltage Low		-10	-1	-10	-10	-1	-10	μA	V_{IN} = 0V	
DYNAMIC											
t_{ON}	Turn-ON Time[2,5]	260		1000			1000		ns	V_{IN} = 3.5V to 0V	R_L = 1kΩ, C_L = 35pF
t_{OFF}	Turn-OFF Time[2,5]	130		500			500		ns	V_{IN} = 0V to 3.5V	V_S = ±5V
$C_{S(OFF)}$	Source OFF Capacitance	9							pF	V_S = 0V, V_{IN} = 5V	
$C_{D(OFF)}$	Drain OFF Capacitance	9							pF	V_D = 0V, V_{IN} = 5V	
$C_{D(ON)} + C_{S(ON)}$	Channel ON Capacitance	21							pF	V_D = V_S = 0V V_{IN} = 0V	
OFF Isolation[6]		65							dB	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF V_S = 7V_{rms}, f = 500kHz	
SUPPLY											
I_1	Positive Supply Current	0.015	2	1	2	2	1	2	mA	One Channel ON, V_{IN} = 0V	
I_2	Negative Supply Current	-0.015	-2	-1	-2	-2	-1	-2	mA		
I_1	Positive Supply Current	0.2	2	1	2	2	1	2	mA	All Channels OFF, V_{IN} = 5V	
I_2	Negative Supply Current	-0.015	-2	-1	-2	-2	-1	-2	mA		

NOTES:
[1] Typical values for information only, not guaranteed or production tested.
[2] Guaranteed, not subject to 100% production test.
[3] I_D(ON) is leakage from driver gate into ON switch.
[4] Digital inputs are MOS gates. Typical leakage (+25°C) is less than 1 nanoamp. This is in contrast to other designs which require typically 150μA to switch.
[5] Switch action is guaranteed break-before-make.
[6] OFF isolation (dB) = 20 log V_S/V_D where V_S = input to OFF switch and V_D = output.

[8] Functional operation is possible for supply voltages less than ±15V, but the input switching threshold will shift (see page 316S).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{IN} (Digital Input) to Ground . . . . . -0.3V, V_1
V_S or V_D to V_1
(1 second surge) . . . . . +25V, -40V
(continuous) . . . . . +20V, -35V
V_S or V_D to V_2
(1 second surge) . . . . . -25V, +40V
(continuous) . . . . . -20V, +35V
V_1 to Ground . . . . . -0.3V, +17V
V_2 to Ground . . . . . +0.3V, -17V
Current, any terminal except S or D 30mA
Continuous Current, S or D 50mA
Peak Current, S or D
(pulsed at 1ms, 10% duty cycle max) 150mA

Operating Temperature
(AP Suffix) . . . . . -55°C to +125°C
(BP Suffix) . . . . . -25°C to +85°C
(CJ Suffix) . . . . . 0°C to +70°C
Storage Temperature
(AP, BP Suffix) . . . . . -65°C to +150°C
(CJ Suffix) . . . . . -65°C to +125°C
Power Dissipation (Package)*
16 Pin Ceramic DIP** 900mW
16 Pin Plastic DIP*** 470mW

* Device mounted with all leads soldered or welded to PC board
** Derate 12mW/°C above +75°C
*** Derate 6.5mW/°C above +25°C

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed for insertion.

CIRCUIT DESCRIPTION

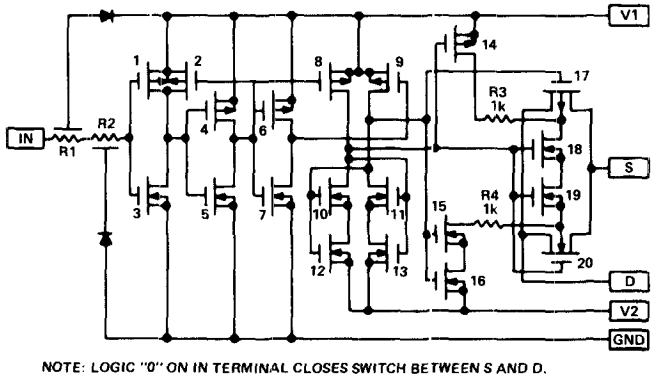


Figure 1. Schematic Diagram, 1 of 4 Channels

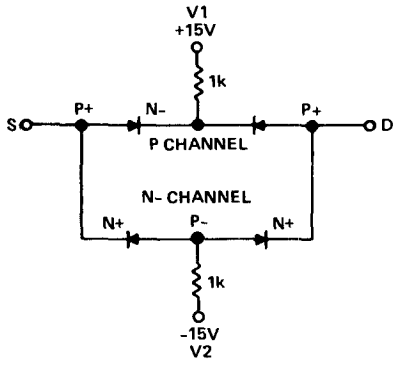


Figure 2. ADG201 Output Switch Diode Equivalent Circuit

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitate protection circuitry. However, these protection circuits either cause degradation of important switch parameters such as R_{ON} or leakage, or provide only limited protection in the event of overvoltage.

The ADG201 switch utilizes a dielectrically-isolated CMOS fabrication process to eliminate the four-layer structure found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. The output switching element consists of device numbers 17 and 20. Operation is as follows: for an "ON" switch, the gate of device 20 is V_1 and the gate of device 17 is V_2 from the driver circuits. Device numbers 14, 15, and 16 are "OFF" and numbers 18 and 19 are "ON". Hence, the back-gates of the P- and N-channel output devices (numbers 17 and 20) are tied together and floating. Floating the output switch back-gates with the signal input provides a flatter R_{ON} versus V_S response.

For an "OFF" switch, device numbers 18 and 19 are "OFF", and the back-gates of devices 17 and 20 are tied through 1kΩ resistors R_3 and R_4 to the respective supply voltages through the "ON" devices 14, 15 and 16.

If a voltage is applied to the S or D terminals which exceeds V_1 or V_2, the S- or D-to-back-gate diode is forward biased; however, R_3 and R_4 provide current limiting action (Fig. 2).

Consequently, without external current limiting resistance (or increased R_{ON}), the ADG201 series switches provide:

1. Latch-proof operation.
2. Overvoltage protection 25V beyond the V_1 or V_2 supply voltage.

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices-*not* in series with the signal path between the S & D terminals.

In some applications it is possible to turn on a parasitic NPN (drain to back-gate to source of the N-channel) transistor which causes device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or the output of op amps will prevent damage to the device.

TYPICAL PERFORMANCE CHARACTERISTICS

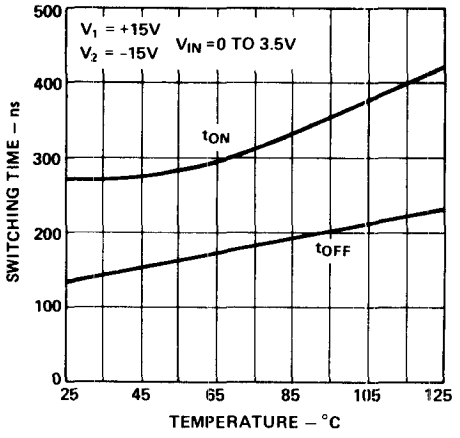


Figure 3. Switching Time vs. Temperature

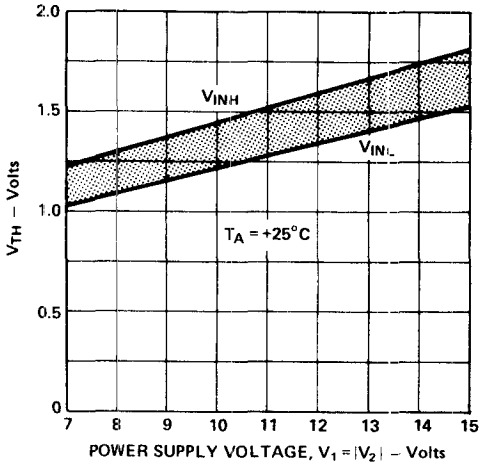
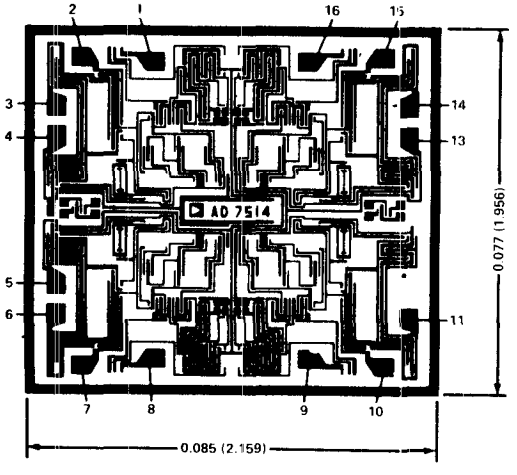


Figure 4. Input Logic Threshold vs. Power Supply Voltage

BONDING DIAGRAM

Dimensions shown in inches and (mm).

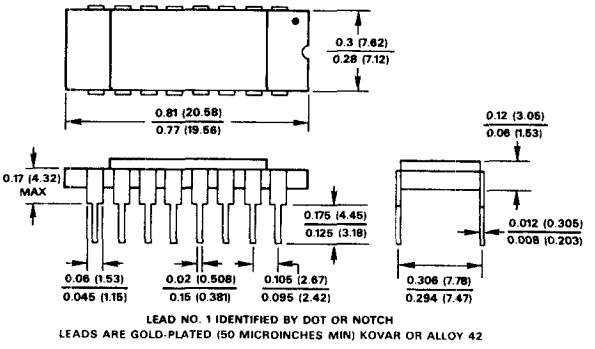


NOTES:
1. PADS ARE 0.004 × 0.004 INCHES (0.102 × 0.102mm) MIN.
2. TO MINIMIZE ESD HAZARD, BOND PIN 5 FIRST
3. PAD NUMBERS CORRESPOND TO PIN NUMBERS SHOWN ON PIN CONFIGURATION.

MECHANICAL INFORMATION

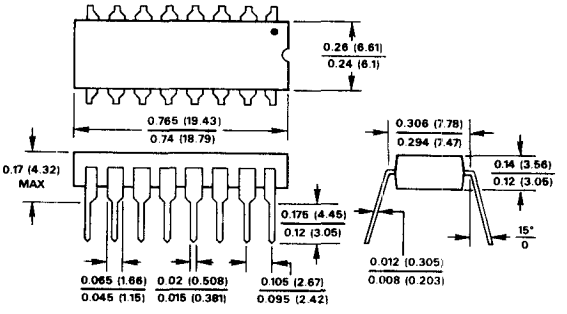
Dimensions shown in inches and (mm).

16 PIN CERAMIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD-PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

16 PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER-PLATED KOVAR OR ALLOY 42