High Resolution 16- and 18-Bit Digital to Analog Converters

DAC1136/1137/1138

FEATURES

DAC1138
- 18-Bit Resolution and Accuracy (38μV, 1 Part in 262,144)
- Integral Nonlinearity 1/2LSB
- Differential Nonlinearity 1/2LSB
- Settling to 1/2LSB (0.0002%) in 10μs
- Hermetically-Sealed Semiconductors

DAC1137
- 18-Bit Resolution, 16-Bit Accuracy
- Lowest Cost 18-Bit DAC
- Settling to 1/2LSB (0.0002%) in 10μs

DAC1136
- 16-Bit Resolution and Accuracy
- Low Cost
- Nonlinearity 1/2LSB
- Settling to 1/2LSB (0.0008%) in 6μs

DEGLITCHER IV
- Virtually Eliminates DAC Glitches
- Available on DAC1136/1137/1138 Card-Mounted Assembly

GENERAL DESCRIPTION

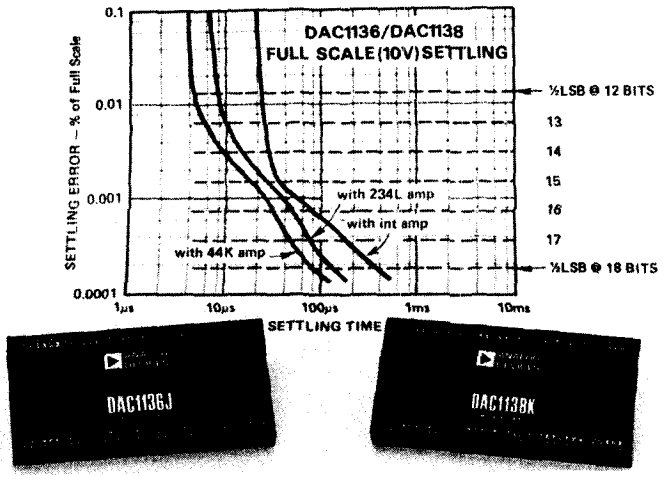
The DAC1136/1137/1138 are complete self-contained voltage or current output modular digital to analog converters with resolutions and accuracies of 16 and 18 bits. These modules are constructed in a compact 2″ X 4″ X 0.4″ package and share the same pin-out as the popular DAC-14QM and DAC-16QM.

The DAC1136/1137/1138 combine precision current sources with state-of-the-art steering switches to produce a very linear output. Inputs to these converters are compatible with TTL levels. The converters have a current output of 2mA full scale. A voltage output can be obtained by connecting the internal amplifier to the current output by means of jumpers. By using additional jumpers, the user can select any one of the following output ranges: 0 to +5V, 0 to +10V, ±5V, or ±10V.

The DAC1136/1137/1138 are available as card-mounted assemblies. In this configuration, selectable options include: input codes, output amplifiers, and a high speed transient-suppressing Deglitcher Module, Deglitcher IV.

WHERE TO USE HIGH RESOLUTION DAC'S

The DAC1136/1137/1138 deliver exceptional accuracies for a broad range of display, test, and instrumentation applications. The DAC1136, with a resolution of 16 bits or 1 part in 65536, and the DAC1137/1138 with a resolution of 18 bits or 1 part in 262,144 are ideally suited for applications requiring wide dynamic range measurement and control. Applications include data distribution systems, high resolution CRT displays, automatic semiconductor testing, photo-typesetting, frequency synthesis and nuclear reactor control.



CERTIFICATE OF CALIBRATION

Each DAC1138 has been calibrated with equipment and methods that are traceable to the National Bureau of Standards (NBS). A Certificate of Performance is sent with each unit, which includes 1000 hour stability data for the reference zener and linearity test data.

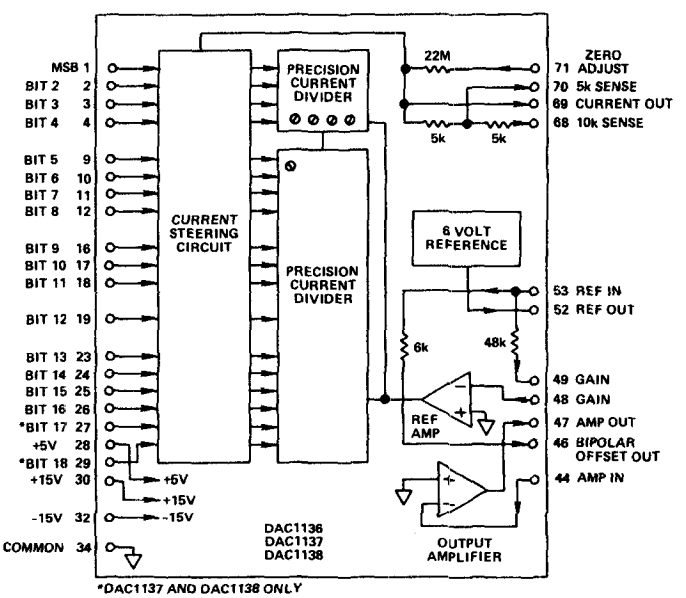


Figure 1. Block Diagram and Pin Designations

SPECIFICATIONS (typical @ +25°C, and rated supply voltage, unless otherwise noted)

Model	DAC1136 J	DAC1136 K	DAC1136 L	DAC1136 CARD-MOUNTED ASSY W/Internal Amp	W/44K	W/234L
RESOLUTION	16 Bits			Specifications are the same as		
Magnitude of 1LSB (10V range)	152μV			module unless otherwise noted		
DIGITAL INPUTS	TTL/See Figure 2					
Input Codes						
Unipolar	Complementary Binary			See Ordering Guide		
Bipolar	Complementary Offset Binary			See Ordering Guide		
Strobe	N.A.			See Note 1		
ACCURACY						
Integral and Differential Nonlinearity (max)	1LSB	0.5LSB	0.5LSB			
Zero Offset	Adjustable to Zero					
Gain	Adjustable to Full Scale					
Reference Voltage[2]	6.00V ± 0.4% max					
TEMPERATURE COEFFICIENTS (ppm/°C)						
Integral Nonlinearity	1	1	1.5 max			
Differential Nonlinearity	1	1	1.5 max			
Offset						
Unipolar		0.5		2	0.5	
Bipolar		5				
Gain[3]	6	6	8 max			
Reference Voltage		3				
STABILITY LONG TERM (ppm/10³ hr)						
Offset		6		30	6	
Gain[3]		12				
Reference Voltage		7				
POWER SUPPLY REJ						
Voltage						
Offset[4]		75dB		80dB	100dB	
Gain		80dB				
DYNAMIC CHARACTERISTICS						
Settling Time to ±1/2LSB						
Voltage						
Full Scale Step						
Unipolar		30μs		15μs	25μs	
Bipolar		40μs		25μs	35μs	
LSB Step		6μs		5μs	7μs	
Current						
Full Scale Step		8μs		VOLTAGE OUTPUT ONLY		
LSB Step		6μs				
Noise (rms 10Hz - 100kHz)						
Voltage		30μV		35μV	40μV	
Current		1nA		VOLTAGE OUTPUT ONLY		
ANALOG OUTPUTS						
Voltage						
Output Range	0 to +5V, 0 to +10V, ±5V, ±10V			See Ordering Guide		
Rated Output Current		4mA		±20mA	±5mA	
Output Impedance	See Characteristic Curves			See Characteristic Curves		
Current						
Output Range						
Unipolar	-2mA to 0mA					
Bipolar	-1mA to +1mA					
VOLTAGE COMPLIANCE						
Rated Accuracy		±2mV		VOLTAGE OUTPUT		
Clamp Limits[5]		±500mV		ONLY		
Source Resistance						
Unipolar		>33kΩ				
Bipolar		>5kΩ				
Source Capacitance		150pF				
POWER SUPPLY REQUIREMENTS[6]						
+5V dc ±5%		9mA		See Note 7		
±15V dc ±5%		30mA		40mA	37mA	
TEMPERATURE RANGE						
Operating Temperature[8]		0 to +70°C				
Storage Temperature		-55°C to +85°C				

NOTES:
[1] Positive going transition (Logic "0" to Logic "1") will clock data into series 74LS, input, latching registers.
[2] The reference output is high impedance ($Z_{out} \approx 200\Omega$)
[3] Exclusive of reference.
[4] Unipolar and bipolar.
[5] Clamp limits are set by Schottky diodes.
[6] Recommended power supply: Analog Devices model 923.
[7] 95mA using mounting card with input latching resigers, see ordering guide.
[8] 5% to 95% relative humidity noncondensing.

Specifications subject to change without notice.

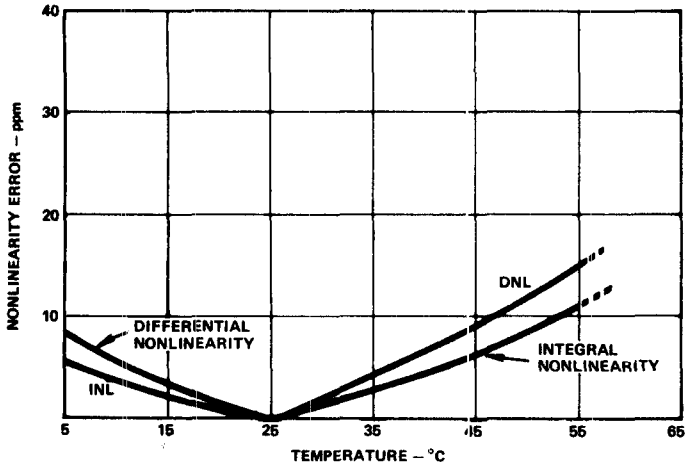
Model	DAC1137	DAC1138 J	DAC1138 K	DAC1137/1138 Card-Mounted Assy W/Internal Amp	DAC1137/1138 Card-Mounted Assy W/234L
RESOLUTION	18 Bits			Specifications are the same as	
Magnitude of 1LSB (10V range)	38μV			module unless otherwise noted	
DIGITAL INPUTS	TTL/See Figure 2				
Input Codes					
Unipolar	Complementary Binary			See Ordering Guide	
Bipolar	Complementary Offset Binary			See Ordering Guide	
Strobe	N.A.			See Note 1	
ACCURACY					
Integral and Differential Nonlinearity (max)	±0.5LSB[2]	±1LSB	±0.5LSB		
Zero Offset Error	Adjustable to Zero				
Gain Error	Adjustable to Full Scale				
Reference Voltage[3] (max)	6.0V±0.25%	6.0V±0.13%	*		
TEMPERATURE COEFFICIENTS (ppm/°C)[4]					
Integral Nonlinearity	±0.5 max	±0.3	*		
Differential Nonlinearity	±0.5 max	±0.4	*		
Offset					
Unipolar	±0.5	±0.5	*		
Bipolar	±3	±1	*		
Gain[5]	±5 max	±0.8	*		
Reference Voltage	±3	±2	*		
STABILITY LONG TERM (ppm/10[3] hr)					
Offset	±3	±2	*		6
Gain[5]	±5	±2	*		
Reference Voltage	±7	±10 max	*		
POWER SUPPLY REJ					
Voltage					
Offset[6]	75dB				100dB
Gain	80dB				
DYNAMIC CHARACTERISTICS					
Settling Time to ±1/2LSB					
Voltage					
Full Scale Step					
Unipolar	250μs				130μs
Bipolar	3ms				200μs
LSB Step	18μs				20μs
Current					
Full Scale Step	10μs			VOLTAGE OUTPUT ONLY	
LSB Step	8μs				
Noise (rms 10Hz - 100kHz)					
Voltage	30μV				40μV
Current	1nA			VOLTAGE OUTPUT ONLY	
ANALOG OUTPUTS					
Voltage					
Output Range	0 to +5V, 0 to +10V, ±5V, ±10V			See Ordering Guide	
Rated Output Current	4mA max				±5mA
Output Impedance	See Characteristic Curves				
Current					
Output Range					
Unipolar	−2mA to 0mA				
Bipolar	−1mA to +1mA				
VOLTAGE COMPLIANCE					
Rated Accuracy	±200μV			VOLTAGE OUTPUT ONLY	
Clamp Limits[7]	±500mV				
Source Resistance					
Unipolar	>33kΩ				
Bipolar	>5kΩ				
Source Capacitance	150pF				
POWER SUPPLY REQUIREMENTS[8,9]					
+5V dc ±5%	9mA			See Note 10	
±15V dc ±5%	30mA				37mA
TEMPERATURE RANGE					
Operating Temperature[11]	0 to +70°C				
Storage Temperature	−55°C to +85°C				

NOTES:
[1] Positive going transition (Logic "0" to Logic "1") will clock data into logic series 74LS network.
[2] DAC1137 has 18-bit resolution and 16-bit accuracy, therefore LSB values are referred to 16 bits.
[3] The reference output is high impedance, maximum load 1μA, $Z_{out} \approx 200\Omega$.
[4] See characteristic curves for performance over temperature.
[5] Exclusive of reference.
[6] Unipolar and bipolar
[7] Clamp limits are set by Schottky diodes.
[8] Recommended power supply: Analog Devices model 923.
[9] Change in differential linearity from factory setting due to power supply voltage variation from nominal is ≅ 3.5ppm/VΔV_S.
[10] 95mA using mounting card with input latching registers, see ordering guide.
[11] 5% to 95% relative humidity noncondensing.

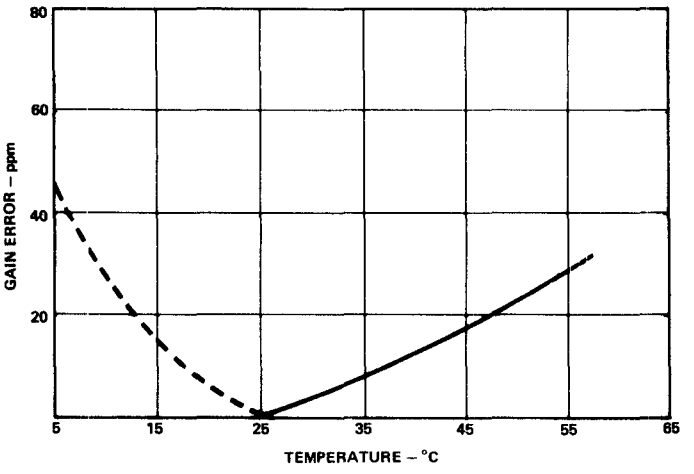
*Specifications same as DAC1138J.

Specifications subject to change without notice.

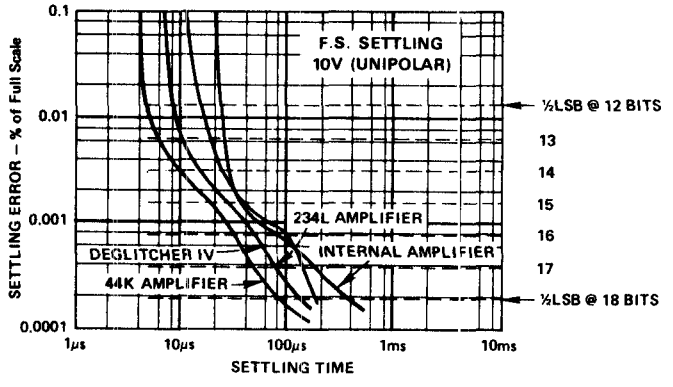
Characteristic Curves*



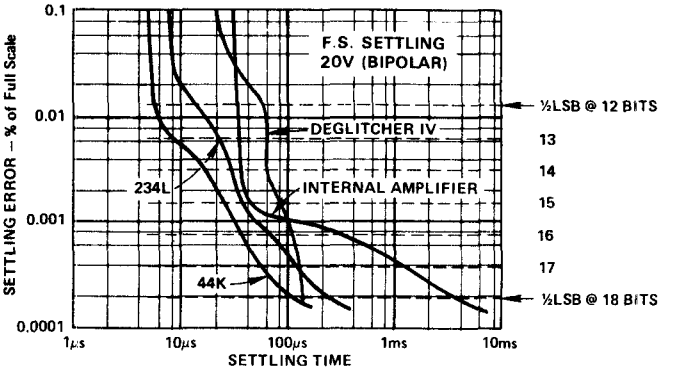
DAC1138 Nonlinearity vs. Temperature



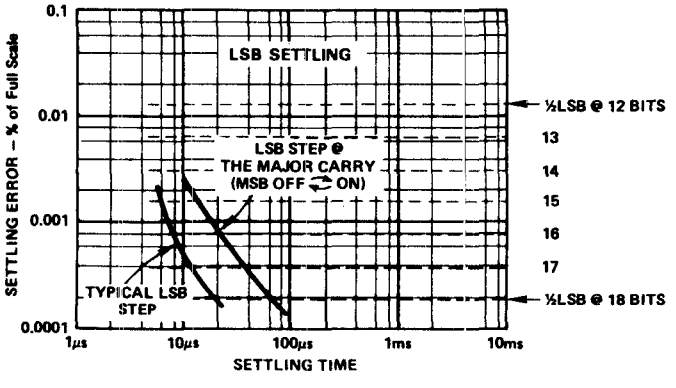
DAC1138 Gain Error vs. Temperature



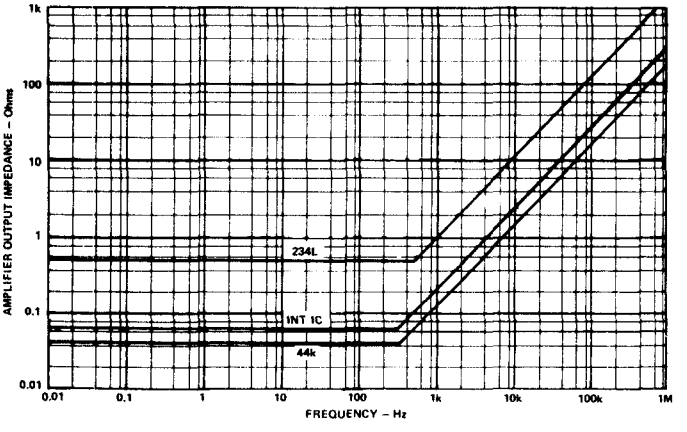
Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for 10V Output Step (0V ⇄ +10V)



Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for 20V Output Step (+10V ⇄ -10V)



Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for LSB Steps (Essentially Independent of Amplifier Used)



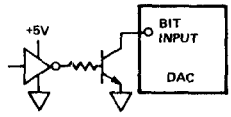
Amplifier Output Impedance vs. Frequency

*NOTE: All curves typical at rated supply voltage.
F.S. = Full Scale

INPUT CONSIDERATIONS

The DAC1136/1137/1138 may be driven by TTL or CMOS as shown in Figure 2. Note that the TTL input is shown with inputs for both a direct "totem pole" TTL gate and open collector (or "pull-up") configurations.

2a. TTL Totem Pole *2b. Switch or Relay Input*[2]



2c. CMOS Input

1. FOR TTL WITH OPEN COLLECTOR, DO NOT USE EXTERNAL PULL-UP. CONVERTERS HAVE INTERNAL 10kΩ PULL-UP ON EACH INPUT TO 3.8V.
2. USE SPST SWITCH OR REPLAY TO GROUND. WHEN SWITCH IS OPEN, INTERNAL 10kΩ WILL PULL INPUT UP TO 3.8V.

Figure 2. Input Connections

OUTPUT CONNECTIONS AND GUARDING

The DAC1136/1137/1138 output connections for various voltage ranges are shown in Figure 3.

Since an LSB is only 38μV (at 10 volts full scale for the DAC1138), care must be exercised to properly guard the current output of the converter from leakage current. Any connection made to the DAC's current output (pin 69) should be guarded. Suggested printed circuit board guarding is shown in Figure 3. The optional card-mounted assemblies of the DAC1136/1137/1138 have been carefully designed for optimum guarding and performance.

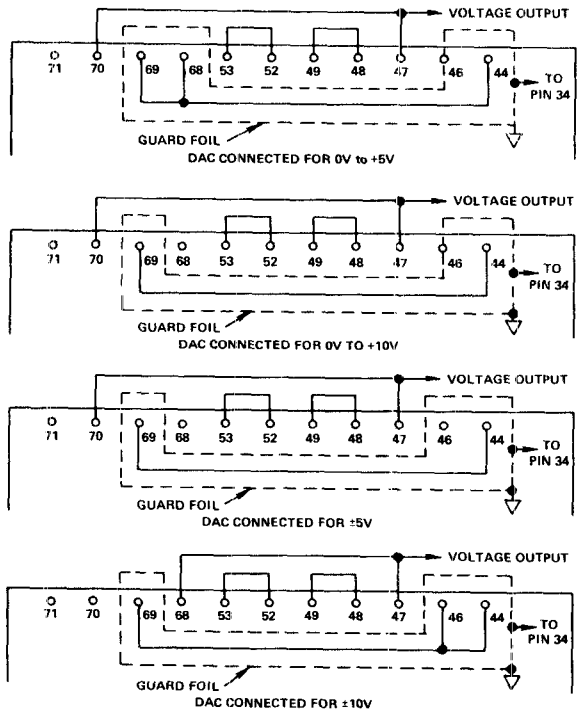
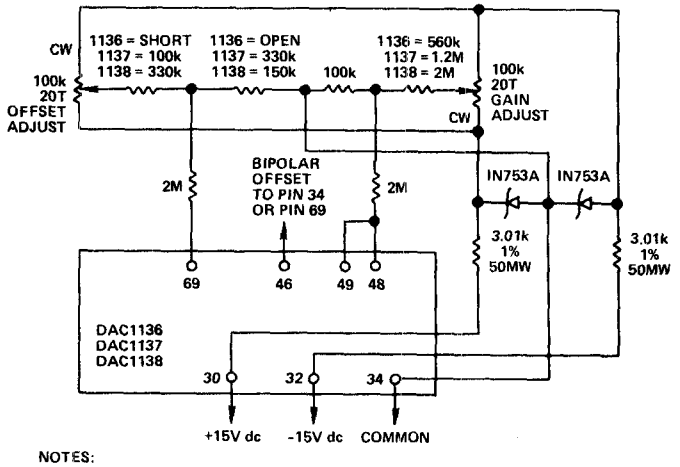


Figure 3. Output Voltage Connections and Suggested PCB Guarding (Unipolar and Bipolar)

GAIN AND OFFSET ADJUSTMENTS

The gain and offset adjustments are made with external potentiometers which the user supplies. With the appropriate digital inputs applied, these potentiometers are adjusted until the desired output voltage is obtained. The proper connections for offset and gain are shown in Figure 4. The voltmeter used to measure the output should be capable of stable resolution of 1/4LSB in the region of zero and full scale. Because of the interaction between offset and gain adjustments, the adjustment procedure described below should be carefully followed. Offset adjustment affects gain, but gain adjustment does not affect offset.



NOTES:
1. ALL FIXED RESISTORS ARE 5% CARBON COMP, UNLESS OTHERWISE NOTED.
2. ALL POTENTIOMETERS ARE 20-TURN INFINITE RESOLUTION TYPE.

Figure 4. Gain and Offset Adjustments

For unipolar mode, apply a digital input of all "1's" (complementary binary code for zero output) and adjust the offset potentiometer until a 0.00000V output is obtained (see Table 1). Once the appropriate offset adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output is obtained (see Table 1).

For bipolar mode, apply a digital input of all "1's" (complementary offset binary code for minus full scale) and adjust the offset potentiometer for the proper minus full scale output voltage (see Table 1). Once the appropriate minus full scale adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output shown below is obtained.

RANGE	IDEAL OUTPUT		
		DAC1137/ 1138	DAC1136
Unipolar:	All 11...1	All 00...0	
0V→+10V	0.00000V	+9.999962V	+9.999848V
0V→+5V	0.00000V	+4.999981V	+4.999924V
Bipolar:			
-10V→+10V	-10.00000V	+9.999934V	+9.999695V
-5V → +5V	-5.00000V	+4.999962V	+9.999848V
To adjust:	Adjust ZERO pot	Adjust GAIN pot	

Table 1. Full Scale Output

DIFFERENTIAL LINEARITY ADJUSTMENT

Each DAC1136/1137/1138 has been factory calibrated and tested to achieve the performance indicated in the electrical specifications. Should it be necessary to readjust the linearity of these units, the user can do so. Before attempting this recalibration, it is imperative that the circuit be checked to confirm that all previously described precautions have been taken to insure proper application at the 16- or 18-bit level. Basically, the DAC is trimmed by comparing a bit to the sum of all lower bits, and adjusting, if necessary, for a one LSB positive difference. The top 4 major carries, i.e., MSB minus the sum of bits 2-through-the-LSB, down through bit 4 minus the sum of bits 5-through-the-LSB, can be trimmed using the procedure outlined below. The setup for this adjustment is shown in Figure 5. In this procedure, an LSB is referred to as 38μV, implying that the DAC1137/1138 is being used on the 10V range. For the DAC1136 an LSB is 152μV on the 10V range.

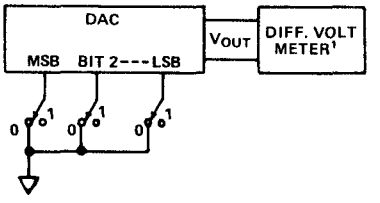
1. Bit 4 Trim
   a. Set bit inputs to 11110 . . . . 0.
   b. Read the output voltage by nulling the voltmeter.
   c. Set bit inputs to 11101 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 1b plus 1LSB. Adjust bit 4 if required (see B4, Figure 7).

2. Bit 3 Trim
   a. Set bit inputs to 1110 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set inputs to 1101 . . . . 1.
   d. Read voltage by nulling the voltmeter. This reading should be equal to that of step 2b plus 1LSB. Adjust bit 3 if required (see B3, Figure 7).

3. Bit 2 Trim
   a. Set bit inputs to 110 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set bit inputs to 101 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 3b plus 1LSB. Adjust bit 2 if required (see B2, Figure 7).

4. Bit 1 (MSB) Trim
   a. Set bit switches to 100 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set bit switches to 011 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 4b plus 1LSB. Adjust bit 1 (MSB) if required (see MSB, Figure 7).

If insufficient range exists on any adjustment, then a separate adjustment for the weight of bits 5-through-the-LSB (see Sum B5 LSB, Figure 7) should be performed. This condition will probably not occur on bit 2, 3 and 4 but might occur on the MSB. If adjustment of the sum of bits 5-through-the-LSB is made, the trim procedure for all bits should be repeated. Obviously, since the procedure affects the weight of individual bits, it affects the overall gain of the DAC. The final step should be adjustment of gain (user supplied adjustment external to module or pot at edge of mounting card).



1. A DIFFERENTIAL VOLTMETER CAPABLE OF 100μV FULL SCALE SHOULD BE USED. THIS WILL RESOLVE AN LSB, WHICH AT 18 BITS IS 38μV (10V RANGE). A FLUKE 895A, OR EQUIVALENT IS RECOMMENDED.

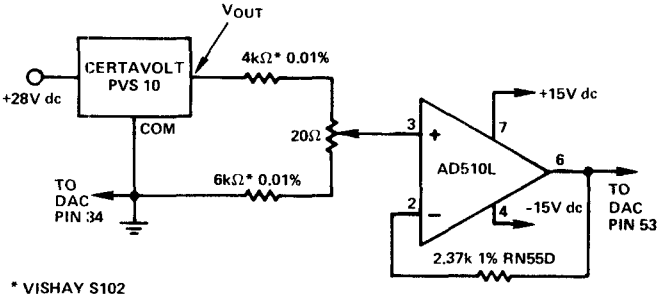
Figure 5. Differential Linearity Adjustment

IMPROVING LONG TERM-STABILITY AND REFERENCE TEMPERATURE COEFFICIENT

The DAC1136/1137/1138 can be operated with an external reference connected to pin 53 of the module. The current drain on the external reference will be 1.125mA in bipolar mode or 0.125mA in unipolar mode (pin 46 should be left open and not grounded when using an external reference in the unipolar mode). When external reference is used, pin 52, the output of the internal reference is left open.

Codi Semiconductor manufactures a reference module called Certavolt[1] with a 10 volt output accurate to 0.001%. This output is temperature compensated to within 1ppm/°C from +15°C to +55°C. The Certavolt requires a power supply of +28V dc @ 20mA. To convert the +10 volt output of the Certavolt to the +6 volt required by the DAC, the circuit shown in Figure 6 is recommended.

[1] Certavolt is a registered trade name by Codi Semiconductor.

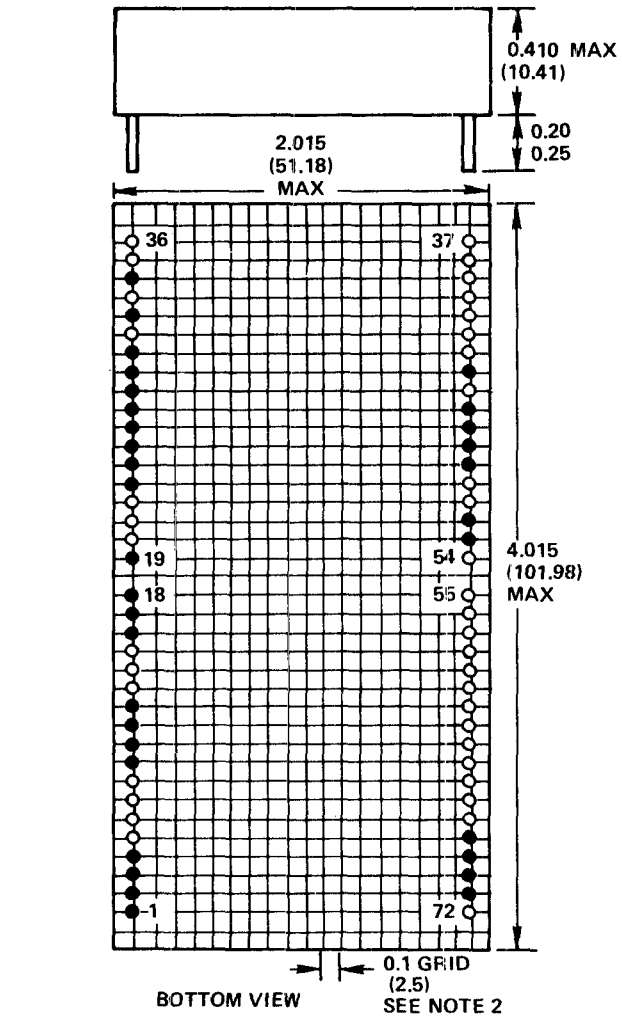


* VISHAY S102

Figure 6. DAC1136/1137/1138 with External Precision Reference

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



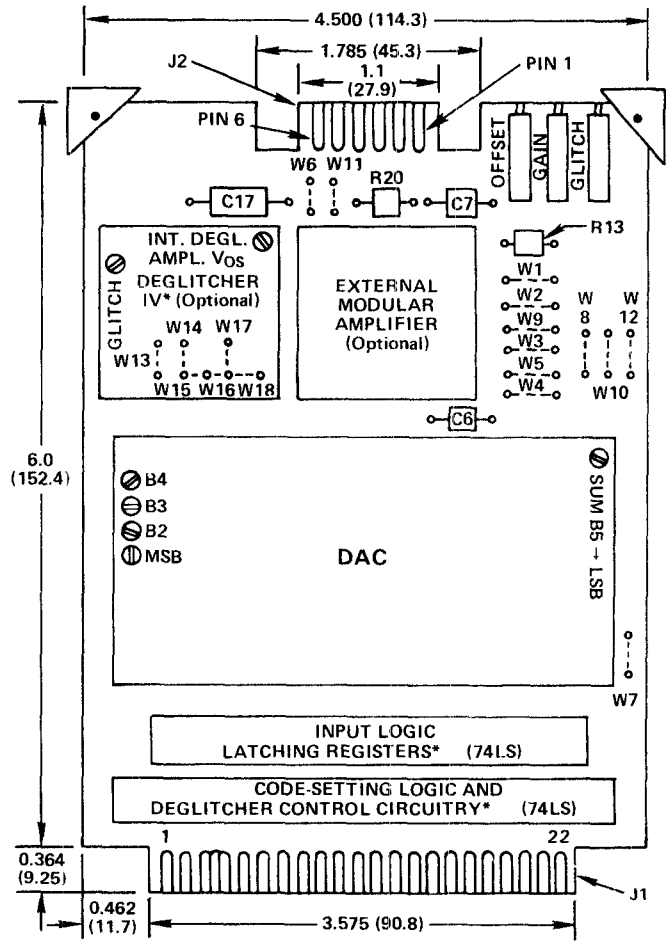
NOTES:

1. PINS: 0.019 ±0.001 DIA HALF HARD BRASS, GOLD PLATED PER MIL-G-45204B CLASS I, TYPE II.
2. GRID AND MARKINGS NEXT TO PINS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT.
3. PINS 27 AND 29 ARE NOT PRESENT ON DAC1136.

OPTIONAL CARD MOUNTED ASSEMBLY

The high resolution of the DAC1136/1137/1138 demands that considerable thought be given to the wiring connections to the module, even when simply evaluating the unit in a temporary laboratory bench set-up. Analog Devices offers an optional card mounted assembly designed to provide optimum performance at the 18-bit level. As shown in Figure 7, this 4 1/2" X 6" printed circuit card can be ordered with input and output options to suit most applications.

The card includes the appropriate DAC, gain and offset adjustment potentiometers, and power supply bypass capacitors. In addition, the card mounted assembly can be ordered with input registers and code-setting logic, external output amplifiers, and a deglitcher. For optimum performance, the card mounted assembly has been designed with a separate analog and digital connector, which are supplied with the unit.



*THESE ITEMS ARE NOT AVAILABLE ON THE "DIRECT" CARD-MOUNTED ASSEMBLY (W'S INDICATE JUMPER POSITIONS).

Figure 7. Card Mounted Assembly

CONNECTOR J1

PIN	FUNCTION	PIN	FUNCTION
A	BIT 1	U	STROBE
B	BIT 2	V	BIT 18[1]
C	BIT 3	W	+5V
D	BIT 4	X	+15V
E	BIT 5	Y	-15V
F	BIT 6	Z	DIGITAL GND
H	BIT 7	1-4	NC
J	BIT 8	5	INTERLOCK
K	BIT 9	6	INTERLOCK
L	BIT 10	7-16	NC
M	BIT 11	17	BIT 17[1]
N	BIT 12	18	
P	BIT 13	19	
R	BIT 14	20	
S	BIT 15	21	
T	BIT 16	22	

J1 MATES WITH CINCH P.N. 251-22-30-160 (SUPPLIED).
[1] DAC 1137/1138 ONLY

CONNECTOR J2

PIN	FUNCTION
1	ANALOG SENSE LOW
2	ANALOG SOURCE LOW
3	NC
4	ANALOG SOURCE HIGH
5	ANALOG SENSE HIGH
6	ANALOG REF. IN/OUT
A	ANALOG REF. IN/OUT
B	ANALOG SENSE HIGH
C	ANALOG SOURCE HIGH
D	NC
E	ANALOG SOURCE LOW
F	ANALOG SENSE LOW

J2 MATES WITH CINCH P.N. 251-06-30-160 (SUPPLIED).

Mounting Card Connector Designations

INPUT OPTIONS

The card-mounted assembly can be ordered with or without input registers. When the direct input option is chosen, the card-mounted assembly will be shipped without input registers. Input registers are mounted on the card when any other digital input code option is selected. The input code ordered by the user is set at the factory by means of various jumpers in the logic circuitry. See ordering guide for details.

When the card mounted assembly contains input registers the system utilizes a dynamic strobe circuit. Strobe characteristics of input registers are:

1. Strobe Pulse: One Std. series 74LS load, Leading-Edge-Triggered. Positive pulse should remain HI for ⩾ 100ns.
2. The digital input code can be changed at any time up to and including that instant when the strobe command goes HI.
3. The actual transfer of the input code to the DAC will occur ≈ 3μs after the strobe command; during this 3μs the digital input code to the card assembly should not be changed, in order to prevent the possible coupling of logic noise into the DAC output.

OUTPUT OPTIONS

The card assembly for the DAC1136/1137/1138 allows for several user-selectable output configurations:

1. Internal IC Output Amplifier built into the DAC.
2. Analog Devices model 234L; for low noise, low drift applications (2μV, ±0.1μV/°C).
3. Analog Devices model 44K; recommended only for high speed or high current applications (75μs settling to 0.0002%, 20mA).
4. Deglitcher IV with self-contained output amplifier.
5. Deglitcher IV with model 234L output amplifier.
6. Deglitcher IV with model 44K output amplifier.

DEGLITCHER IV

The Deglitcher IV is a precision high-speed, high-isolation sample-and-hold circuit which eliminates the glitches that occur whenever a DAC is dithered through a major carry. Such momentary transients can be of concern in applications such as high-resolution CRT beam positioning, where glitch-free code transitions are often required for optimum display quality and legibility. Oscilloscope photographs in Figures 8a and 8b below show the output of a DAC1136 being dithered up and down through the major carry, between codes 1000000000000000 and 0111111111111111. In Figure 8b, the Deglitcher IV is turned on, virtually eliminating the glitches and allowing the 152μV LSB step to be clearly seen.

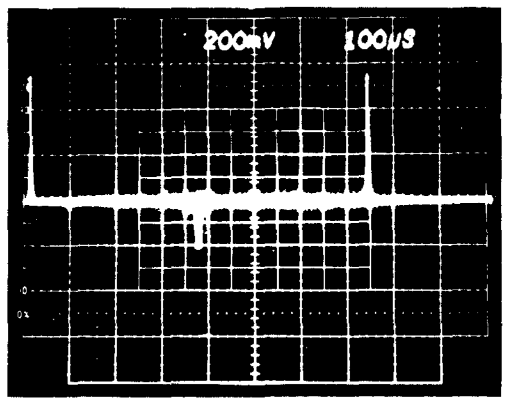


Figure 8a. DAC1136; Major-Carry Dither without Deglitcher IV (BW = 1MHz)

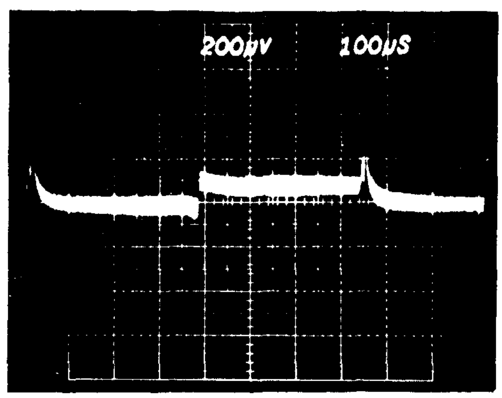


Figure 8b. Same Major-Carry Dither with Deglitcher IV (BW = 1MHz)

The Deglitcher IV utilizes a proprietary sampling technique which isolates the output amplifier during the critical 10μs period immediately following a code change. The only discernible difference in DAC performance when used with Deglitcher IV is a delay of approximately 13μs after the strobe goes HI before the (deglitched) DAC output voltages starts slewing toward the new value.

GLITCH ADJUSTMENT

There are two glitch adjustment potentiometers on the mounting card assembly. With the DAC updating on the major carry, adjust the external glitch potentiometer for optium glitch. If necessary, glitch adjustment can also be made with glitch potentiometer internal to Deglitcher IV.

CARD-MOUNTED ASSEMBLY JUMPER DESIGNATIONS

The output voltage range, reference source, amplifier and deglitcher configuration can be programmed by the user, if necessary, by means of jumpers, resistors and capacitors, as shown below.

Output Voltage Range	Install Jumpers
±10V	W10, W5
±5V	W12, W5
+10V	W12, W3

Reference	Install Jumpers
Internal	W2
External	W1

Amplifier	Install Jumpers
Internal	W4, W9
External[1]	W8, W13
Deglitcher IV[2]	W8, W15, W17, W18
Deg. IV with Ext Amp[3]	W8, W14, W16

NOTES:

[1] With a 234L amplifier install C7 (0.01μF, 10%, ceramic capacitor). With a 44K amplifier use a variable resistor (typ value ≈ 499Ω, 0.1W, 1%) to adjust the output voltage for a ±100μV reading as measured between pins 69 and 34 of the DAC (this step sets voltage compliance); install this value resistor (R13 position).

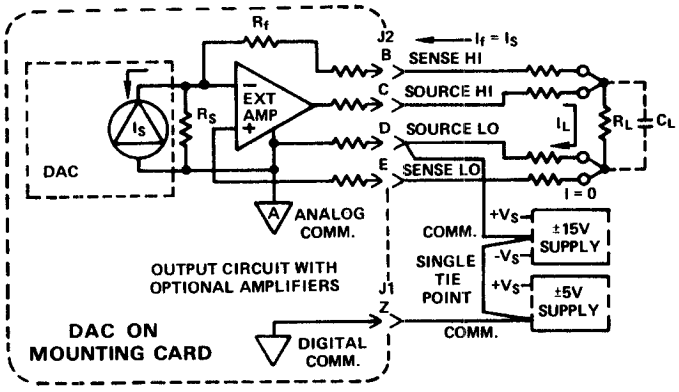
[2] With Deglitcher IV remove R20 (100Ω) and replace the resistor with a jumper.

[3] With Deglitcher IV and a 234L amplifier install: C7 (0.01μF, 10% ceramic capacitor), C6 (220pF, 10%, ceramic capacitor), C17 (1000pF, 10%, polystyrene capacitor) and replace R20 (100Ω) with a jumper. With Deglitcher IV and a 44K amplifier perform the operation described in note 1 and install: C6 (220pF, 10%, ceramic capacitor), C17 (1000pF, 10%, polystyrene capacitor) and replace R20 (100Ω) with a jumper.

To isolate analog and digital grounds, W7 is omitted (refer to Figure 7 for recommended ground tie point).

W6 and W11 are not installed on standard units; this allows 4-wire connection to J2 when either a 44K or 234L amplifier is used.

When using an external amplifier, a four terminal output connection can be utilized on the card assembly in order to allow for compensation of connector contact resistance. See Figure 9.



NOTE:
1. VOLTAGE DROP BETWEEN SOURCE LO AND SENSE LO MUST OBSERVE CURRENT MODE COMPLIANCE LIMITS FOR RATED ACCURACY.
2. THIS CONNECTION SCHEME CANNOT BE USED WITH INTERNAL AMPLIFIER OF THE DAC OR DEGLITCHER IV.

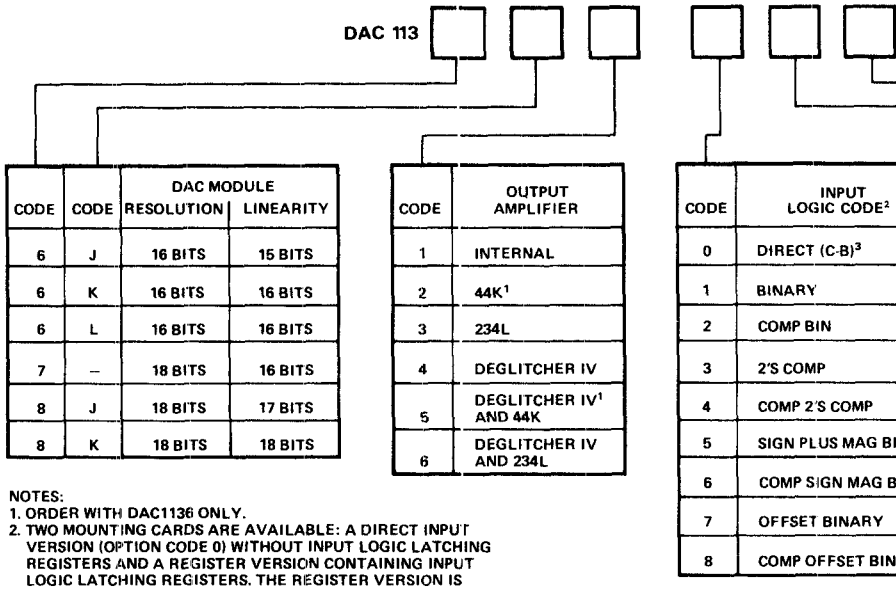
Figure 9. Output Circuit with Optional Amplifiers

ORDERING GUIDE

WHEN ORDERING THE DAC1136/1137/1138 WITHOUT THE CARD ASSEMBLY, ORDER EITHER

DAC1136J	DAC1137	DAC1138J
DAC1136K		DAC1138K
DAC1136L		

When ordering the DAC1136/1137/1138 as a Card-Mounted Assembly, the part must be described with 6 suffixes as shown on next page.



CODE	CODE	DAC MODULE RESOLUTION	LINEARITY
6	J	16 BITS	15 BITS
6	K	16 BITS	16 BITS
6	L	16 BITS	16 BITS
7	–	18 BITS	16 BITS
8	J	18 BITS	17 BITS
8	K	18 BITS	18 BITS

CODE	OUTPUT AMPLIFIER
1	INTERNAL
2	44K[1]
3	234L
4	DEGLITCHER IV
5	DEGLITCHER IV[1] AND 44K
6	DEGLITCHER IV AND 234L

CODE	INPUT LOGIC CODE[2]
0	DIRECT (C-B)[3]
1	BINARY
2	COMP BIN
3	2'S COMP
4	COMP 2'S COMP
5	SIGN PLUS MAG BIN
6	COMP SIGN MAG BIN
7	OFFSET BINARY
8	COMP OFFSET BINARY

CODE	OUTPUT VOLTAGE RANGE
1	+10V
2	±5V
3	±10V

CODE	DAC VOLTAGE REFERENCE
1	INTERNAL
2	EXTERNAL

NOTES:
1. ORDER WITH DAC1136 ONLY.
2. TWO MOUNTING CARDS ARE AVAILABLE: A DIRECT INPUT VERSION (OPTION CODE 0) WITHOUT INPUT LOGIC LATCHING REGISTERS AND A REGISTER VERSION CONTAINING INPUT LOGIC LATCHING REGISTERS. THE REGISTER VERSION IS SUPPLIED WHEN CODES 1 THRU 8 ARE ORDERED.
3. NOT AVAILABLE ON CARD ASSEMBLIES ORDERED WITH DEGLITCHER IV