INTERSIL

M2114L
4096 Bit (1024x4) NMOS Static RAM

FEATURES

- *Cycle Time Equal to Access Time*
- Completely Static-No Clock Required
- Common Data Input and Output
- TTL Compatible Inputs and Outputs
- 883A Class B Processing Available
- Single +5 Volt Power Supply
- Maximum Access Time:
  - 200 ns (-2)
  - 300 ns (-3)
- Maximum Power Dissipation: -495mW
- Pin Compatible with Intel M2114
- Military Temperature Operation:
  -55°C to +125°C

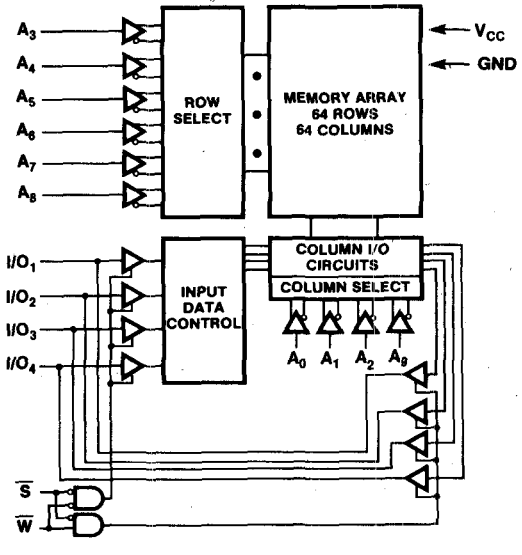
DESCRIPTION

The M2114L is a 4096-bit static Random Access Memory organized 1024 words x 4 bits. The storage cells and decode and control circuitry are completely static therefore, no clocks or refresh operations are required. Memory access occurs within the specified access time after all address inputs are stable. A Chip Select input is provided for simple memory array *expansion.*

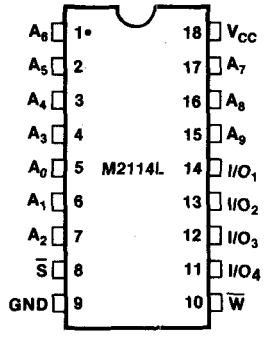
The M2114L is pin and functionally compatible with the Intel M2114 series, and operations at 90mA over a 5V ± 10% range. The worst-case access time is 450ns with speeds of 300 ns (-3) and 200ns (-2) available.

The device is assembled in a standard 18-pin DIP for *maximum system packing density.*

BLOCK DIAGRAM

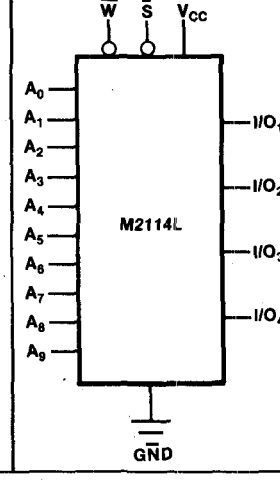


PIN CONFIGURATION



(outline dwg JN)

LOGIC SYMBOL



PIN NAMES

A_0-A_9	ADDRESS INPUTS
I/O_1-I/O_4	DATA INPUT/OUTPUT
$\overline{W}$	WRITE ENABLE
$\overline{S}$	CHIP SELECT

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE
MD2114L2	200ns	CERDIP
MD2114L3	300ns	CERDIP
MD2114L	450ns	CERDIP

8

ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin to Ground ..... −0.5V to +7V
Power Dissipation 1W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Input Load Current	I_{INLD}	V_{IN} = 0V to 5.5V		10	μA
Output Leakage Current	$\|I_{OLK}\|$	$\overline{S}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}		10	μA
Power Supply Current	I_{CC1}	V_{IN} = 5.5V, $I_{I/O}$ = 0mA, T_A = +25°C		65	mA
Power Supply Current	I_{CC2}	V_{IN} = 5.5V, $I_{I/O}$ = 0mA, T_A = −55°C		90	mA
Input Low Voltage	V_{IL}		−0.5	0.8	V
Input High Voltage	V_{IH}		2.0	V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA		0.4	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4	V_{CC}	V

CAPACITANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF

8

NOTE: These parameters are periodically sampled, not 100% tested.

DEVICE OPERATION

When $\overline{W}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{W}$ remains high, the data stored cannot be changed by the addresses, Chip Select, or data I/O voltage levels and timing transitions. The block diagram also shows data storage cannot be changed by $\overline{W}$, the addresses, or the input data as long as $\overline{S}$ is high. Either $\overline{S}$ or $\overline{W}$ by itself, or in conjuction with the other, can prevent the extraneous writing due to signal transitions.

A read occurs during the overlap of $\overline{S}$ low and $\overline{W}$ high. Data within the array can only be changed during a Write time, defined as the overlap of $\overline{S}$ low and $\overline{W}$ low. To prevent the loss of data, the addresses must be properly established during the entire Write time plus t_{wr}.

AC CHARACTERISTICS

TEST CONDITIONS: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$
$t_r = t_f = 10ns$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$, Output Load = 1 TTL Gate and 100pF
Input and Output Timing Reference Level = 1.5V

READ CYCLE

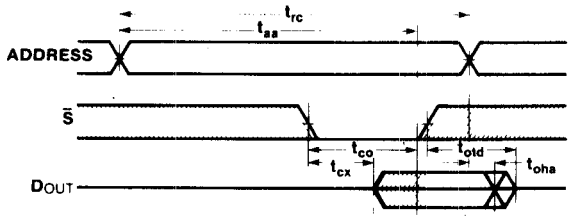
PARAMETER	SYMBOL	M2114L2		M2114L3		M2114L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{rc}	200		300		450		ns
Access Time	t_{aa}		200		300		450	
$\overline{S}$ to Output Valid	t_{co}		70		100		100	
$\overline{S}$ to Output Active	t_{cx}	20		20		20		
Output Three-State from Deselect	t_{otd}	0	60	0	80	0	100	
Output Hold from Address Change	t_{oha}	50		50		50		

WRITE CYCLE

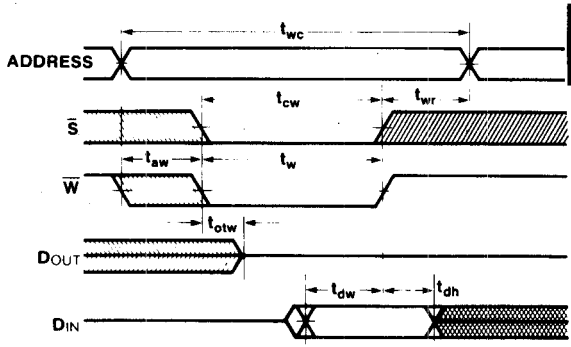
PARAMETER	SYMBOL	M2114L2		M2114L3		M2114L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{wc}	200		300		450		ns
Write Time	t_w	120		150		200		
Write Release Time	t_{wr}	0		0		0		
Output Three-State from Write	t_{otw}	0	60	0	80	0	100	
Data to Write Time Overlap	t_{dw}	120		150		200		
Data Hold from Write Time	t_{dh}	0		0		0		
Address Setup Time	t_{aw}	0		0		0		
$\overline{S}$ Select Pulse Width	t_{cw}	120		150		200		

TIMING DIAGRAMS

READ CYCLE (1)

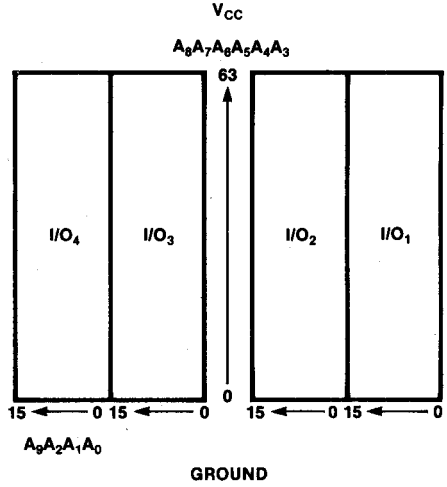


WRITE CYCLE



Note: 1. $\overline{W}$ is high for a READ cycle.

2114 BIT MAP DIAGRAM



8