INTERSIL

# 2N5515-2N5524 Monolithic Dual N-Channel JFET

1

## ABSOLUTE MAXIMUM RATINGS (Note 1)

@25°C (unless otherwise noted)

Maximum Temperatures

| | |
|---|---|
| Storage Temperature | -65°C to +200°C |

| Maximum Power Dissipation | ONE SIDE | BOTH SIDES |
|---|---|---|
| Device Dissipation | 250 mW | 500 mW |
| @ Free Air Temperature | 85°C | 85°C |
| Linear Derating | 3.85 mW/°C | 7.7 mW/°C |

Maximum Voltages & Current

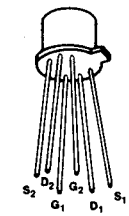
| | |
|---|---|
| $V_{GS}$ Gate to Source Voltage | -40 V |
| $V_{GD}$ Gate to Drain Voltage | -40 V |
| $I_G$ Gate Current | 50 mA |

## FEATURES

- Tight Temperature Tracking – $\Delta V_{GS} < 5\ \mu V/°C$
- Tight Matching –
  - $V_{GS} < 5$ mV
  - $I_G < 10$ nA @ 125°C
  - $g_{fs} < 3\%$
  - $g_{oss} < .1\ \mu$mho
- High Common Mode-Rejection – CMRR < 100 db
- Low Noise – $e_n < 15$ nV / √Hz @10 Hz

## PIN CONFIGURATION

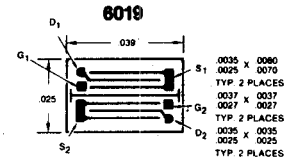
TO-71




## CHIP TOPOGRAPHY

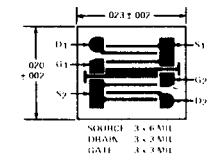
(2N5520-24)

**6019**




(2N5515-19)

**6017**




## ORDERING INFORMATION

| TO-72 | WAFER | DICE |
|---|---|---|
| 2N5515 | 2N5515/W | 2N5515/D |
| 2N5516 | 2N5516/W | 2N5516/D |
| 2N5517 | 2N5517/W | 2N5517/D |
| 2N5518 | 2N5518/W | 2N5518/D |
| 2N5519 | 2N5519/W | 2N5519/D |
| 2N5520 | 2N5520/W | 2N5520/D |
| 2N5521 | 2N5521/W | 2N5521/D |
| 2N5522 | 2N5522/W | 2N5522/D |
| 2N5523 | 2N5523/W | 2N5523/D |
| 2N5524 | 2N5524/W | 2N5524/D |
| 2N5525 | 2N5525/W | 2N5525/d |

1

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| PARAMETER | | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| $I_{GSS}$ | Gate Reverse Current (+ 25°C) (+150°C) | | -250 -250 | pA nA | $V_{GS}$ = -30 V, $V_{DS}$ = 0 |
| $BV_{GSS}$ | Gate-Source Breakdown Voltage | -40 | | V | $I_G$ = 1 μA, $V_{DS}$ = 0 |
| $V_P$ | Gate-Source Pinch-Off Voltage | -0.7 | -4 | V | $V_{DS}$ = 20 V, $I_D$ = 1 nA |
| $I_{DSS}$ | Drain Current at Zero Gate Voltage (Note 2) | 0.5 | 7.5 | mA | $V_{DS}$ = 20 V, $V_{GS}$ = 0 |
| $g_{fs}$ | Common-Source Forward Transconductance (Note 2) | 1000 | 4000 | μmho | $V_{DS}$ = 20 V, $V_{GS}$ = 0 f = 1 kHz |
| $g_{oss}$ | Common-Source Output Conductance | | 10 | μmho | $V_{DS}$ = 20 V, $V_{GS}$ = 0 f = 1 kHz |
| $C_{rss}$ | Common-Source Reverse Transfer Capacitance | | 5 | pF | $V_{DS}$ = 20 V, $V_{GS}$ = 0 f = 1 MHz |
| $C_{iss}$ | Common-Source Input Capacitance | | 25 | pF | $V_{DS}$ = 20 V, $V_{GS}$ = 0 f = 1 MHz |
| $\bar{e}_n$ | Equivalent Input Noise Voltage 2N5515-19 | | 30 | nV/√Hz | $V_{DG}$ = 20 V, $I_D$ = 200 μA f = 10 Hz |
| | 2N5520-24 | | 15 | nV/√Hz | $V_{DG}$ = 20 V, $I_D$ = 200 μA f = 10 Hz |
| | 2N5515-24 | | 10 | nV/√Hz | $V_{DG}$ = 20 V, $I_D$ = 200 μA f = 1 kHz |
| $I_G$ | Gate Current (+ 25°C) (+125°C) | | -100 -100 | pA nA | $V_{DG}$ = 20 V, $I_D$ = 200 μA |
| $V_{GS}$ | Gate Source Voltage | -0.2 | -3.8 | V | $V_{DG}$ = 20 V, $I_D$ = 200 μA |
| $g_{fs}$ | Common-Source Forward Transconductance (Note 2) | 500 | 1000 | μmho | $V_{DG}$ = 20 V, $I_D$ = 200 μA f = 1 kHz |
| $g_{oss}$ | Common-Source Output Conductance | | 1 | μmho | $V_{DG}$ = 20 V, $I_D$ = 200 μA |

## MATCHING CHARACTERISTICS (25°C unless otherwise noted)

| PARAMETER | | 2N5515,20 | | 2N5516,21 | | 2N5517,22 | | 2N5518,23 | | 2N5519,24 | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| $I_{DSS1}$ / $I_{DSS2}$ | Drain Current Ratio at Zero Gate Voltage (Note 2) | 0.95 | 1 | 0.95 | 1 | 0.95 | 1 | 0.95 | 1 | 0.90 | 1 | | $V_{DS}$ = 20 V, $V_{GS}$ = 0 |
| $\lvert I_{G1} - I_{G2} \rvert$ | Differential Gate Current (+125°C) | | 10 | | 10 | | 10 | | 10 | | 10 | nA | $V_{DG}$ = 20 V, $I_D$ = 200 μA |
| $g_{fs1}$ / $g_{fs2}$ | Transconductance Ratio (Note 2) | 0.97 | 1 | 0.97 | 1 | 0.95 | 1 | 0.95 | 1 | 0.90 | 1 | | $V_{DG}$ = 20 V, $I_D$ = 200 μA f = 1 KHz |
| $\lvert g_{oss1} - g_{oss2} \rvert$ | Differential Output Conductance | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | 0.1 | μmho | $V_{DG}$ = 20 V, $I_D$ = 200 μA f = 1 KHz |
| $\lvert V_{GS1} - V_{GS2} \rvert$ | Differential Gate-Source Voltage | | 5 | | 5 | | 10 | | 15 | | 15 | mV | $V_{DG}$ = 20 V, $I_D$ = 200 μA |
| $\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$ | Gate-Source Voltage Differential Drift ($T_A$ = +25°C to +125°C) | | 5 | | 10 | | 20 | | 40 | | 80 | μV/°C | $V_{DG}$ = 20 V, $I_D$ = 200 μA |
| $\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$ | Gate-Source Voltage Differential Drift ($T_A$ = +25 to -55°C) | | 5 | | 10 | | 20 | | 40 | | 80 | μV/°C | $V_{DG}$ = 20 V, $I_D$ = 200 μA |
| CMRR | Common Mode Rejection Ratio (Note 3) | 100 | | 100 | | 90 | | | | | | dB | $V_{DD}$ = 10 to 20 V, $I_D$ = 200 μA |

**NOTES:**

1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 28mS used during test.
3. CMRR = $20 \log_{10} \Delta V_{DD} / \Delta \lvert V_{GS1} - V_{GS2} \rvert$, ($\Delta V_{DD}$ = 10V)