INTERSIL

DG201/IH5201
Quad SPST CMOS Analog Switches

FEATURES
- **Switches Greater Than 28V_{p-p} Signals With ±15V Supplies**
- **Quiescent Current Less Than 100μA**
- **Break-Before-Make Switching t_{off} = 100nsec, t_{on} = Typically 500nsec**
- **TTL, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**
- **Industry Standard (DG201)**
- **Improved Performance Version IH5201**

GENERAL DESCRIPTION
The DG201/IH5201 solid-state analog gates are designed using an improved, high-voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid-state switches. Destructive latch-up of solid-state analog gates has been eliminated by INTERSIL's CMOS technology.

Key performance advantages of these devices are TTL compatibility, low-power operation (quiescent current less than 100μA), and guaranteed break-before-make switching.

The DG201 is completely spec and pin-out compatible with the industry standard device, while the IH5201 offers significantly enhanced specifications with respect to ON and OFF leakage currents, switching times, and supply current.

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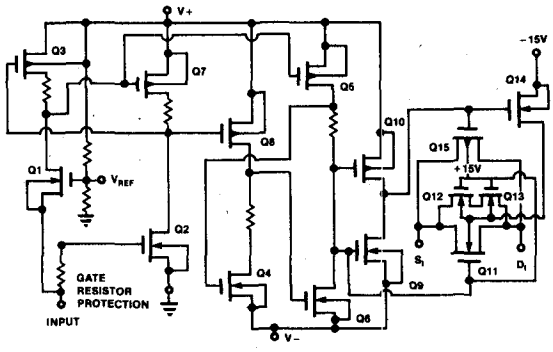
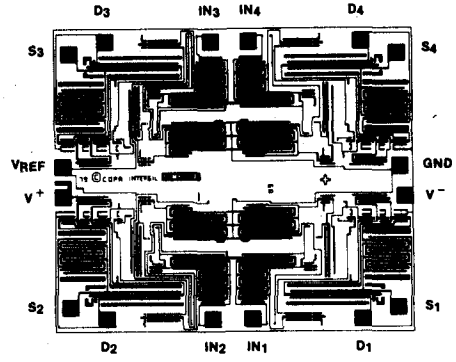
SCHEMATIC DIAGRAM (¼ DG201/IH5201)



CHIP TOPOGRAPHY



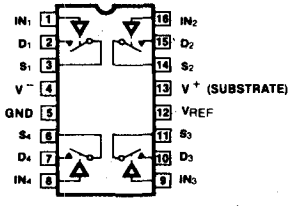
NOTE: Backside of chip common to V+.

ORDERING INFORMATION

INDUSTRY STANDARD PART	IMPROVED SPEC DEVICE	PACKAGE	TEMPERATURE RANGE
DG201AK	IH5201MJE	16-Pin CERDIP	−55°C to +125°C
DG201BK	IH5201IJE	16-Pin CERDIP	−20°C to +85°C
DG201CJ	IH5201CPE	16-Pin Plastic DIP	0°C to +70°C

PIN CONFIGURATIONS (Outline dwgs JE, PE)

DUAL-IN-LINE PACKAGE



SWITCH OPEN FOR LOGIC "1" INPUT

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ ..... <33V
$V^+ - V_D$ ..... <30V
$V_D - V^-$ ..... <30V
$V_D - V_S$ ..... < ±22V
$V_{REF} - V^-$ ..... <33V
$V_{REF} - V_{IN}$ ..... <30V
V_{REF}-GND ..... <20V
V_{IN}-GND ..... <20V

Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Power Dissipation 450mW
Derate 6mW/°C Above 70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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DG201

ELECTRICAL CHARACTERISTICS (@25°C, V^+ = +15V, V^- = −15V)

PER CHANNEL		MIN./MAX. LIMITS							TEST
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0°C	+25°C	+70°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8V
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4V
$r_{DS(ON)}$	Drain-Source On Resistance	80	80	125	100	100	125	Ω	I_S = 1mA, V_{ANALOG} = ± 10V
$r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1mA
V_{ANALOG}	Analog Signal Handling Capability	±14	±14	±14	±14	±14	±14	V	I_S = 10mA
$I_{D(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	100	nA	V_{ANALOG} = −14V to +14V
$I_{S(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	100	nA	V_{ANALOG} = −14V to +14V
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	2	2	200	5	5	200	nA	$V_D = V_S$ = ±14V
t_{on}	Switch "ON" Time		1.0			1.0		μs	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Fig. A
t_{off}	Switch "OFF" Time		0.5			0.5		μs	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF See Fig. C
I_Q^+	+ Power Supply Quiescent Current	2000	1000	2000	2000	1000	2000	μA	V_{IN} = 0V or 5V
I_Q^-	− Power Supply Quiescent Current	2000	1000	2000	2000	1000	2000	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off

TEST CIRCUITS

Figure A

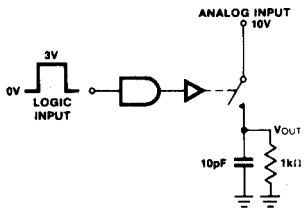


Figure B

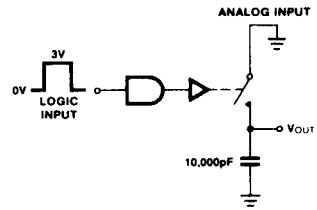
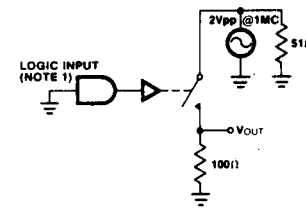


Figure C



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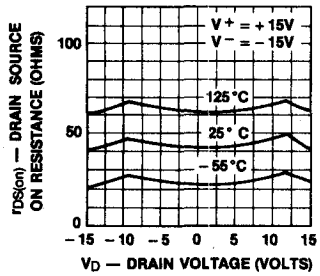
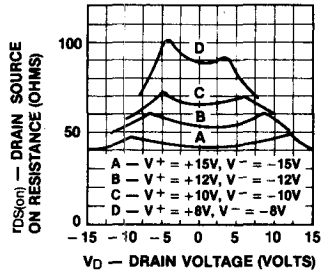
IH5201

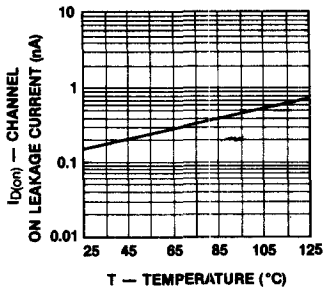
ELECTRICAL CHARACTERISTICS (@25°C, $V^+ = +15V$, $V^- = -15V$)

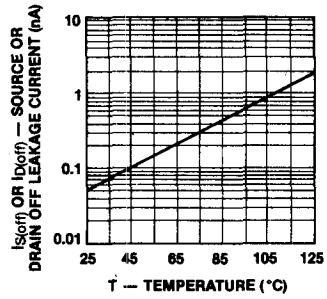
PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0°C	+25°C	+70°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 0.8V$
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	$V_{IN} = 2.4V$
$r_{DS(ON)}$	Drain-Source On Resistance	75	75	100	100	100	125	Ω	$I_S = 1mA$, $V_{ANALOG} = \pm 10V$
$r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1mA
V_{ANALOG}	Analog Signal Handling Capability	±14	±14	±14	±14	±14	±14	V	$I_S = 10mA$
$I_{D(OFF)}$/ $I_{S(OFF)}$	Switch OFF Leakage Current	0.2	0.2	50	1	1	50	nA	$V_{ANALOG} = -14V$ to $+14V$
$I_{D(ON)}$ + $I_{S(ON)}$	Switch ON Leakage Current	0.5	0.5	100	1	1	100	nA	$V_D = V_S = \pm 14V$
t_{on}	Switch "ON" Time		0.5			0.75		μs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. A
t_{off}	Switch "OFF" Time		0.25			0.3		μs	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. A
$Q_{(INJ.)}$	Charge Injection		5			10		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. C
I_Q^+	+ Power Supply Quiescent Current	1000	750	600	1500	1000	1000	μA	$V_{IN} = 0V$ to $5V$
I_Q^-	− Power Supply Quiescent Current	10	10	100	20	20	200	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off

TYPICAL CHARACTERISTICS









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APPLICATIONS

Application Hints

V^+ Positive Supply Voltage (V)	V^- Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
+15	−15	Open	2.4/0.8	−15 to +15
+12	−12	Open or 1.4V	2.4/0.8	−12 to +12
+10	−10	1.4V	2.4/0.8	−10 to +10
+8*	−8	1.4V	2.4/0.8	−8 to +8

*Operation below ±8V is not recommended.

Logic Inputs

Logic input circuitry protects the input MOS gate from transients. A series MOS device shuts off when V_{IN} exceeds the positive power supply; negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike occurring at the transition voltage when the logic goes from V_{INH} to V_{INL}. If a series resistor is used for additional static protection it should be limited to less than 4.7kΩ to ensure switching with worst case current spikes.

The Function of V_{REF}

V_{REF} is an internal connection which allows the user to establish the logic threshold voltage at which the switch changes state. The actual threshold voltage is equal to the voltage on the V_{REF} pin; V_{REF} is internally connected for a 1.4V threshold at $V^+ = +15V$. For other thresholds and/or supply voltages, V_{REF} may be connected to a voltage source or resistive divider whose output voltage is equal to the desired threshold. The internal impedance of V_{REF} is 21kΩ ±30%.

Additionally, to adjust V_{REF}, a single pullup resistor can be used from the V_{REF} pin to a positive supply voltage to shunt the upper internal divider resistor. The equation below shows the calculation of the shunt resistor for the desired logic threshold voltage — this calculation is based on nominal internal resistor values, which are ±30% in absolute magnitude. The adjusted trip point voltage (V_{REF}) should be limited to an upper level of 5V to avoid input logic switching transition hysteresis.

$$R_{SHUNT} = \frac{R1 \times R2\left(\frac{V^+}{V_{tr}} - 1\right)}{R1 - R2\left(\frac{V^+}{V_{tr}} - 1\right)}$$

Calculation of R_{SHUNT}

Where $R1 \cong 220k\Omega$: nominal values,

$R2 \cong 23k\Omega$ ±30% run-to-run

Example: for $V^+ = 15V$, $V_{TRIP} = 5V$, using nominal R1, R2 calculation $R_{SHUNT} = 58k\Omega$.