INTERSIL

AD7520/7530
AD7521/7531
10 & 12 Bit Monolithic Multiplying D/A Converters

FEATURES

- **AD7520/AD7530: 10 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **AD7521/AD7531: 12 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **Low Power Dissipation: 20 mW (Max)**
- **Low Nonlinearity Tempco: 2 PPM of FSR/° C (Max)**
- **Current Settling Time: 500 ns to 0.05% of FSR**
- **Supply Voltage Range: +5V to +15V**
- **DTL/TTL/CMOS Compatible**
- **Full Input Static Protection**
- **883B Processed Versions Available**

GENERAL DESCRIPTION

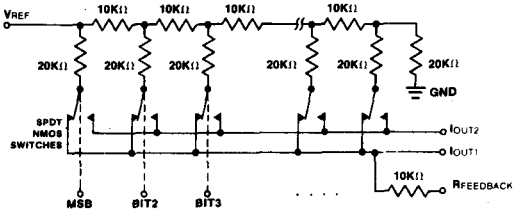
The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). INTERSIL thin-film on CMOS processing gives up to 10-bit accuracy with DTL/TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

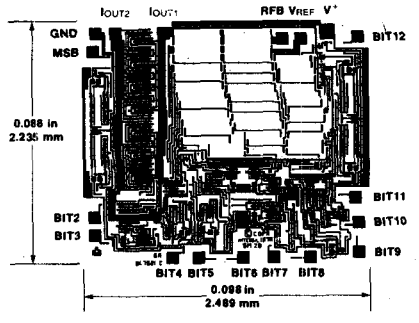
4

FUNCTIONAL DIAGRAM



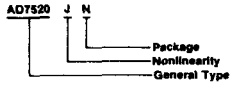
(Switches shown for Digital Inputs "High")
(Resistor values are nominal)

CHIP TOPOGRAPHY



PACKAGE IDENTIFICATION

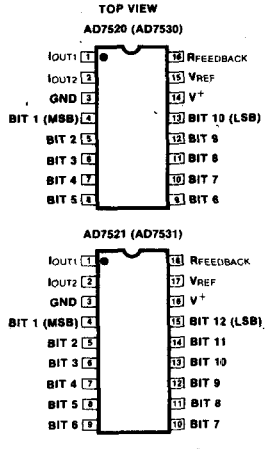
Suffix D: Cerdip package
Suffix N: Plastic DIP package



ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7520JN AD7530JN AD7521JN AD7531JN	AD7520JD AD7530JD AD7521JD AD7531JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7530KN AD7521KN AD7531KN	AD7520KD AD7530KD AD7521KD AD7531KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7530LN AD7521LN AD7531LN	AD7520LD AD7530LD AD7521LD AD7531LD	AD7520UD AD7521UD

PIN CONFIGURATION (Outline dwgs DE, PE)



ABSOLUTE MAXIMUM RATINGS (T_A = 25° C unless otherwise noted)

V^+ ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V^+ to GND
Output Voltage Compliance ..... −100mV to V^+
Power Dissipation (package)
up to +75°C ..... 450 mW
derate above +75°C @ ..... 6 mW/°C

Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
JD, KD, LD Versions ..... −25°C to 85°C
SD, TD, UD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C

CAUTION: 1) The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2) Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{fb}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V, TA = 25°C unless otherwise specified)

PARAMETER	AD7520 (AD7530)	AD7521 (AD7531)	UNITS	LIMIT	TEST CONDITIONS	FIG.
DC ACCURACY (Note 1) Resolution	10	12	Bits			
Nonlinearity J S	0.2 (8-Bit)		% of FSR	Max	S, T, U: over −55°C to =125°C	1
K T	0.1 (9-Bit)		% of FSR	Max		1
L U	0.05 (10-Bit)		% of FSR	Max	$-10V \le V_{REF} \le +10V$	1
Nonlinearity Tempco	2		PPM of FSR/°C	Max	$-10V \le V_{REF} \le +10V$	
Gain Error (Note 2)	0.3		% of FSR	Typ		
Gain Error Tempco (Note 2)	10		PPM of FSR/°C	Max		
Output Leakage Current (*either output*)	200 (300)		nA	Max	Over the specified temperature range	
Power Supply Rejection	±0.005		% of FSR/%	Typ		2
AC ACCURACY Output Current Settling Time	500		nS	Typ	To 0.05% of FSR (All digital inputs low to high and high to low)	6
Feedthrough Error	10		mV pp	Max	V_{REF} = 20V pp, 100kHz (50kHz) All digital inputs low	5
REFERENCE INPUT Input Resistance (Note 3)	5k 10k 20k		Ω	Min Typ Max	All digital inputs high. I_{OUT1} at ground.	
ANALOG OUTPUT Voltage Compliance (both outputs)	See absolute max. ratings					
Output Capacitance	I_{OUT1} 120 I_{OUT2} 37		pF pF	Typ Typ	All digital inputs high	4
	I_{OUT1} 37 I_{OUT2} 120		pF pF	Typ Typ	All digital inputs low	4
Output Noise (both outputs)	Equivalent to 10kΩ Johnson noise			Typ		3
DIGITAL INPUTS Low State Threshold	0.8		V	Max	Over the specified temp range	
High State Threshold	2.4		V	Min		
Input Current (low to high state)	1		μA	Typ		
Input Coding	Binary/Offset Binary				See Tables 1 & 2 on pages 4 and 5	
POWER REQUIREMENTS Power Supply Voltage Range	+5 to +15		V			
I^+	5		nA	Typ	All digital inputs at GND	
	2		mA	Max	All digital inputs high or low	
Total Power Dissipation (Including the ladder)	20		mW	Typ		

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Ladder and feedback resistor Tempco is approximately −150ppm/°C.

TEST CIRCUITS

NOTE: The following test circuits apply for the AD7520. Similar circuits can be used for the AD7530, AD7521 and AD7531.

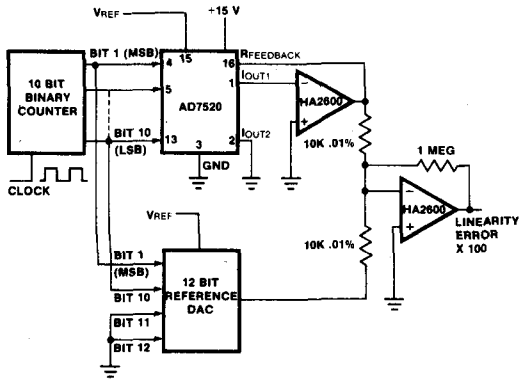


Figure 1. Nonlinearity

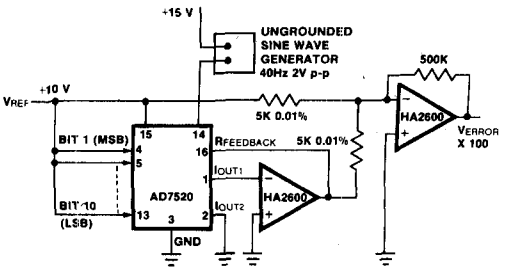


Figure 2. Power Supply Rejection

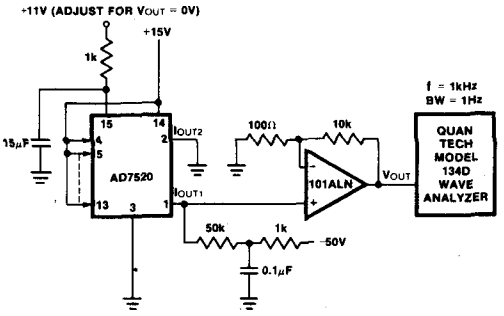


Figure 3. Noise

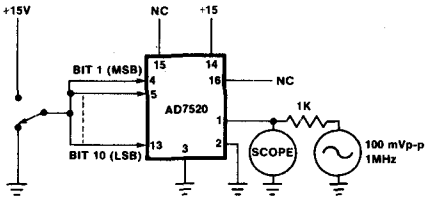


Figure 4. Output Capacitance

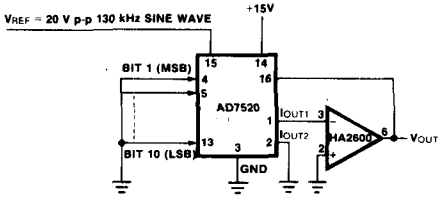


Figure 5. Feedthrough Error

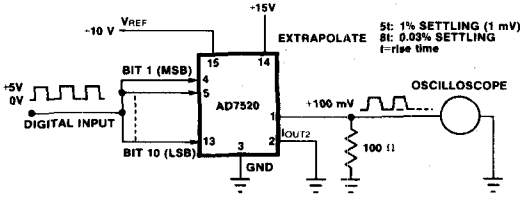


Figure 6. Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

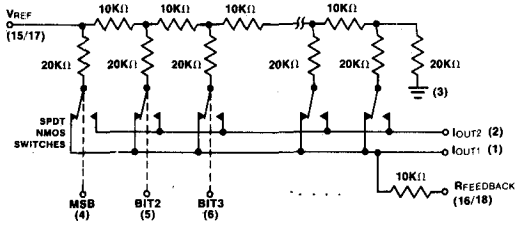
OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The AD7520 (AD7530) and AD7521 (AD7531) are monolithic, multiplying D/A converters. Highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 7. The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} busses which must be held either at ground or virtual ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



(Switches shown for Digital Inputs "High")

Figure 7. 7520/7521 Functional Diagram

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 8). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.

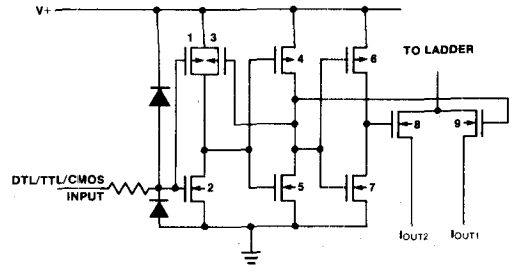


Figure 8. CMOS Switch

4

APPLICATIONS

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7520 (AD7530) and AD7521 (AD7531) in unipolar mode is shown in Figure 9. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

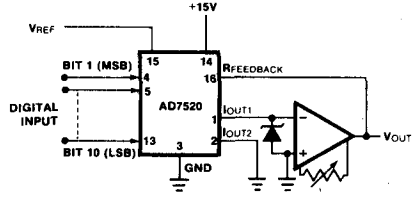


Figure 9. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±1 mV at V_{OUT}.

Gain Adjustment

1. Connect all AD7520 (AD7530) or AD7521 (AD7531) digital inputs to V^+.
2. Monitor V_{OUT} for a $-V_{REF}(1-2^{-n})$ reading. (n = 10 for AD7520 (AD7530) and n = 12 for AD7521 (AD7531)).
3. To decrease V_{OUT}, connect a series resistor (0 to 500 ohms) between the reference voltage and the V_{REF} terminal.
4. To increase V_{OUT}, connect a series resistor (0 to 500) ohms) in the I_{OUT_1} amplifier feedback loop.

TABLE 1

CODE TABLE — UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-n})$
1000000001	$-V_{REF}(1/2+2^{-n})$
1000000000	$-V_{REF} / 2$
0111111111	$-V_{REF}(1/2-2^{-n})$
0000000001	$-V_{REF}(2^{-n})$
0000000000	0

NOTE: 1. LSB = 2^{-n} V_{REF} 2. n = 10 for 7520, 7521; n = 12 for 7530, 7531

(APPLICATIONS, Cont'd.)

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7520 (AD7530) or AD7521 (AD7531) in the bipolar mode is given in Figure 10. Using offset binary digital input codes and positive and negative reference voltage values 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

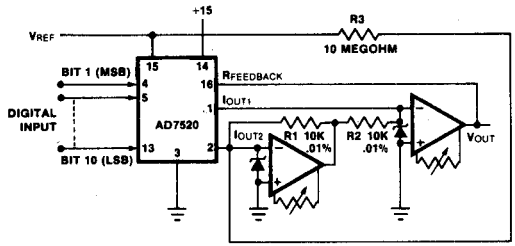


Figure 10. Bipolar Operation (4-Quadant Multiplication)

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10 Megohm), from V_{REF} to I_{OUT2}.

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±1mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset zero adjust trimpot for 0V ±1 mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V^+.
2. Monitor V_{OUT} for a $-V_{REF}(1-2^{-(n-1)})$ volts reading. (n = 10 for AD7520 and AD7530, and n = 12 for AD7521 and AD7531).
3. To increase V_{OUT}, connect a series resistor of up to 500Ω between V_{OUT} and R_{fb}.
4. To decrease V_{OUT}, connect a series resistor of up to 500Ω between the reference voltage and the V_{REF} terminal.

TABLE 2
CODE TABLE — BIPOLAR (OFFSET BINARY) OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-(n-1)})$
1000000001	$-V_{REF}(2^{-(n-1)})$
1000000000	0
0111111111	$V_{REF}(2^{-(n-1)})$
0000000001	$V_{REF}(1-2^{-(n-1)})$
0000000000	V_{REF}

NOTE: 1. LSB = $2^{-(n-1)}$ V_{REF} 2. n = 10 for 7520 and 7521; n = 12 for 7530 and 7531

POWER DAC DESIGN USING AD7520

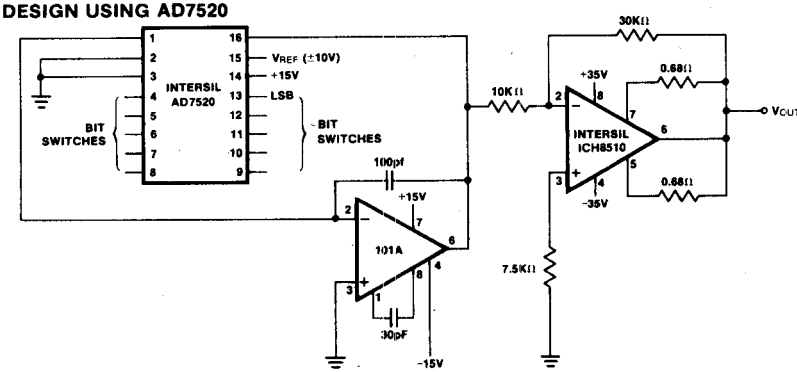


Figure 11. The Basic Power DAC

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 11. An INTERSIL IH8510 power amplifier (1 Amp continuous output at up to ±25 V) is driven by the AD7520.

A summing amplifier between the AD7520 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise the AD7520 can be directly connected to the IH8510, by using a 25 V reference for the DAC.

An important note on the AD7520/101A interface concerns the connection of pin 1 of the DAC and pin 2 of the 101A. Since this point is the summing junction of an amplifier with an AC gain of 50,000 or better, stray capacitance should be minimized; otherwise instabilities and poor noise performance will result. Note that the output of the 101A is fed into an inverting amplifier with a gain of -3, which can be easily changed to a non-inverting configuration. (For more information see: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)

(APPLICATIONS, Cont'd.)

ANALOG/DIGITAL DIVISION

With the AD7520 connected in its normal multiplying configuration as shown in figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_x assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 12, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit-10) ON, the gain is 1023. With all bits ON, the gain is 1 (±1 LSB).

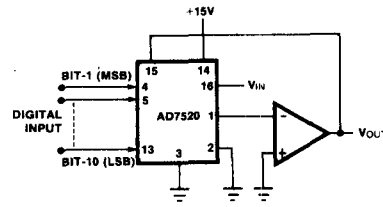


Figure 12. Analog/Digital Divider

4