INTERSIL

AD7533
10 Bit Monolithic Multiplying D/A Converters

FEATURES

- **Lowest cost 10-bit DAC**
- **8, 9 and 10 bit linearity**
- **Low gain and linearity Tempcos**
- **Full temperature range operation**
- **Full input static protection**
- **DTL/TTL/CMOS direct interface**
- **+5 to +15 volts supply range**
- **Low power dissipation**
- **Fast settling time**
- **Four quadrant multiplication**
- **Direct AD7520 equivalent**
- **883B Processed versions available**

GENERAL DESCRIPTION

The Intersil AD7533 is a low cost, monolithic 10-bit, four-quadrant multiplying digital-to-analog converter (DAC).

Intersil's thin-film resistors on CMOS circuitry provide 10, 9 and 8 bit accuracy, full temperature range operation, +5V to +15V power range, full input protection from damage due to static discharge by clamps to V+ and ground and very low power dissipation.

Pin and function equivalent to Industry Standard AD7520, the AD7533 is recommended as a lower cost alternative for old or new 10-bit DAC designs.

Application of AD7533 includes programmable gain amplifiers, digitally controlled attenuators, function generators and control systems.

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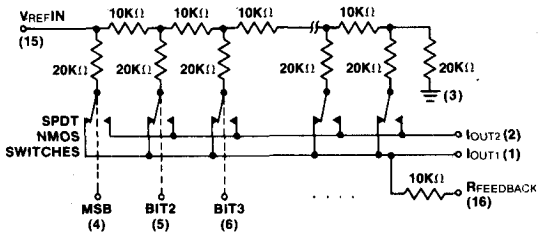
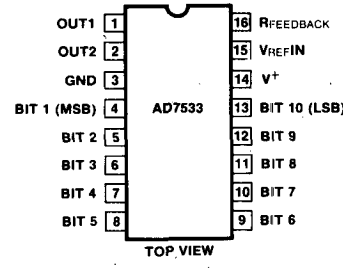
FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High")

PIN CONFIGURATION

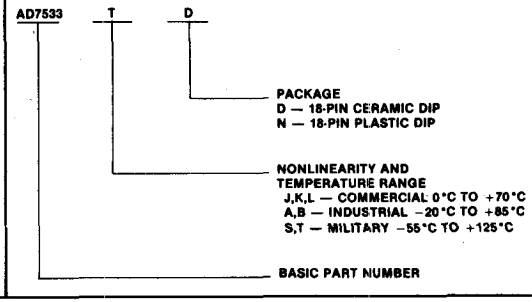


(Outline dwg DE, PE)

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	-20°C to +85°C	-55°C to +125°C
±0.2% (8-bit)	AD7533JN	AD7533AD	AD7533SD
±0.1% (9-bit)	AD7533KN	AD7533BD	AD7533TD
±0.05% (10-bit)	AD7533LN	AD7533CD	AD7533UD

PACKAGE IDENTIFICATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V^+ ..... −0.3V, +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... −0.3V to V^+
Output Voltage Compliance ..... −0.3 to V^+
Power Dissipation (package)
Ceramic
up to +75°C 450mW
derates above +75°C by ..... 6mW/°C
Plastic
up to 70°C 670mW
derates above 70°C by ..... 8.3mW/°C
Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD, CD Versions ..... −25°C to +85°C
SD, TD, UD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

CAUTION: 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages lower than ground or higher than V^+ to any pin except V_{REF} and R_{FB}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V^+ = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0 unless otherwise specified.)

PARAMETER		T_A +25°C	T_A MIN-MAX	UNITS	LIMIT	TEST CONDITIONS
DC ACCURACY (Note 1)						
Resolution		10	10	Bits	Min	
Nonlinearity (Note 2)		±0.2	±0.2	% of FSR	Max	
		±0.1	±0.1	% of FSR	Max	$-10V \le V_{REF} \le +10V$
		±0.05	±0.05	% of FSR	Max	$V_{OUT1} = V_{OUT2} = 0V$
Gain Error (Note 2 and 5)		±1.4	±1.5	% of FS	Max	Digital Inputs = V_{INH}
Output Leakage Current (either output)		±50	±200	nA	Max	V_{REF} = ±10V
AC ACCURACY						
Power Supply Rejection (Note 2 and 3)		0.005	0.008	% of FSR/%	Max	V^+ = 14.0 to 17.0V
Output Current Settling Time		600 (Note 6)	800 (Note 3)	nS	Max	To 0.05% of FSR, R_L = 100Ω
Feedthrough Error (Note 3)		±0.05	±0.1	% FSR	Max	V_{REF} = ±10V, 100kHz sine wave. Digital inputs low.
REFERENCE INPUT		5K			Min	
Input Resistance (Pin 15)		20K		Ω	Max	All digital inputs high.
Temperature Coefficient		−300		ppm/°C	Typ	
ANALOG OUTPUT						Both outputs.
Voltage Compliance (Note 4)		−100mV to V^+				See maximum ratings.
Output Capacitance (Note 3)	C_{OUT1}	100		pF	Max	All digital inputs high (V_{INH})
	C_{OUT2}	35		pF	Max	
	C_{OUT1}	35		pF	Max	All digital inputs low (V_{INL})
	C_{OUT2}	100		pF	Max	
DIGITAL INPUTS						
Low State Threshold (VINL)		0.8		V	Max	
High State Threshold (VINH)		2.4		V	Min	
Input Current (I_{IN})		±1		μA	Max	V_{IN} = 0V and V^+
Input Coding		Binary/Offset Binary				See Tables 1 & 2
Input Capacitance (Note 3)		5		pF	Max	
POWER REQUIREMENTS						
V_{DD}		+15 ±10%		V		Rated Accuracy
Power Supply Voltage Range		+5 to +16		V		
I^+		2		mA	Max	Digital Inputs = V_{INL} to V_{INH}
		100	150	μA	Max	Digital Inputs = 0V or V^+

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.
5. Full scale (FS) = − (V_{REF}) • (1023/1024)
6. Sample tested to ensure specification compliance.
7. 100% screened to MIL-STD-883, method 5004, para. 3.1.1. through 3.1.12 for class B device. Final electrical tests are: Nonlinearity, Gain Error, Output Leakage Current, V_{INH}, V_{INL}, I_{IN} and I^+ @ +25°C and +125°C (SD, TD, UD) or +25°C and +85°C (AD, BD, CD).

Specifications subject to change without notice.

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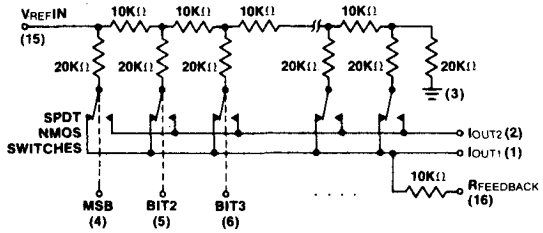
GENERAL CIRCUIT INFORMATION

The Intersil AD7533 is a 10 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 1. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



(Switches shown for Digital Inputs "High")

Figure 1

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 2). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors resulting in accurate leg currents.

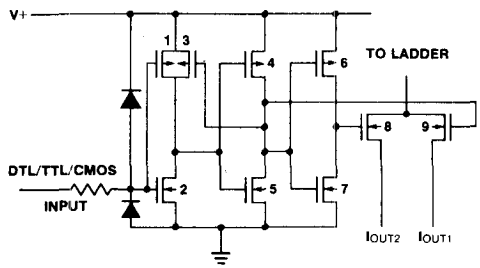


Figure 2

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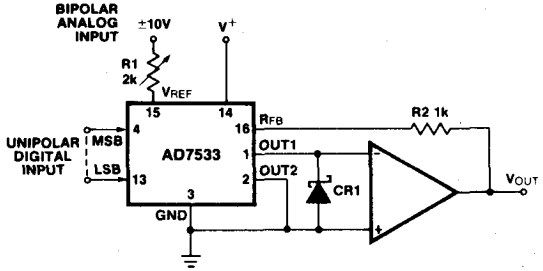
APPLICATIONS

UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. SCHOTTKY DIODE CR1 (HP5082-2811 OR EQUIV) PROTECTS OUT1 TERMINAL AGAINST NEGATIVE TRANSIENTS.

Figure 3. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 3)
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001	$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000	$-V_{REF}\left(\frac{512}{1024}\right) = -\frac{V_{REF}}{2}$
0111111111	$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	$-V_{REF}\left(\frac{0}{1024}\right) = 0$

NOTES:

1. Nominal Full Scale for the circuit of Figure 3 is given by

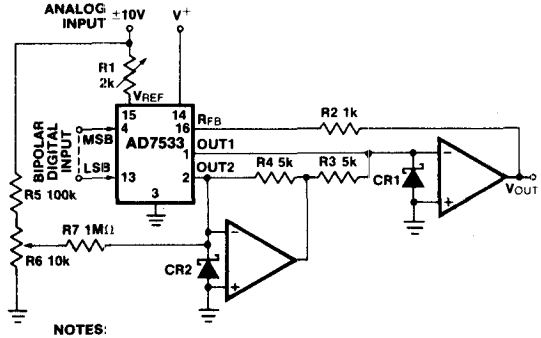
$$FS = -V_{REF}\left(\frac{1023}{1024}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 3 is given by

$$LSB = V_{REF}\left(\frac{1}{1024}\right)$$

Table 1. Unipolar Binary Code

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. SCHOTTKY DIODES CR1 AND CR2 (HP5082-2811 OR EQUIV) PROTECT OUT1 AND OUT2 TERMINALS FROM NEGATIVE TRANSIENTS

Figure 4. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 4)
1111111111	$-V_{REF}\left(\frac{511}{512}\right)$
1000000001	$-V_{REF}\left(\frac{1}{512}\right)$
1000000000	0
0111111111	$+V_{REF}\left(\frac{1}{512}\right)$
0000000001	$+V_{REF}\left(\frac{511}{512}\right)$
0000000000	$+V_{REF}\left(\frac{512}{512}\right)$

NOTES:

1. Nominal Full Scale Range for the circuit of Figure 4 is given by

$$FSR = V_{REF}\left(\frac{1023}{512}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 4 is given by

$$LSB = V_{REF}\left(\frac{1}{512}\right)$$

Table 2. Bipolar (Offset Binary) Code Table

POWER DAC DESIGN USING AD7533

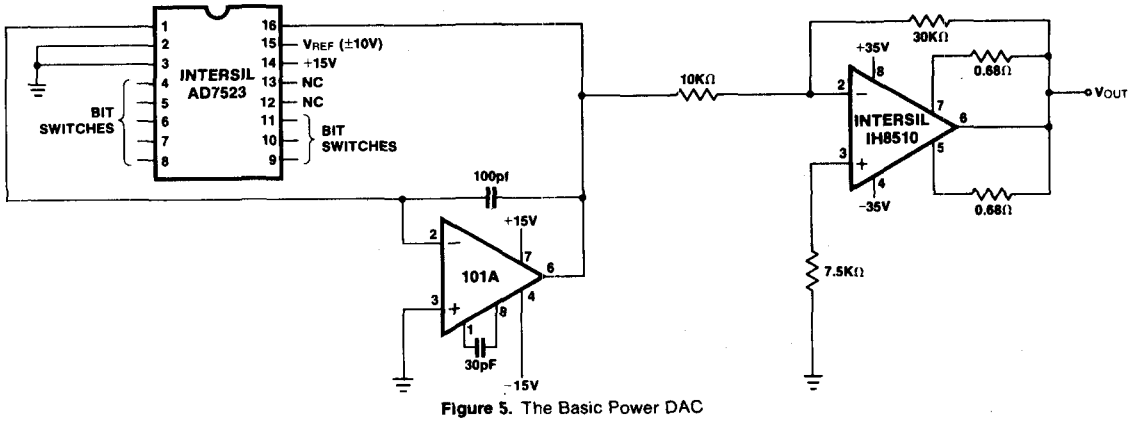


Figure 5. The Basic Power DAC

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 5. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to +25V) is driven by the AD7533.

A summing amplifier between the AD7533 and the IH8510 is used to separate the gain block containing the AD7533 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7533 can be directly connected to the IH8510, by using a 25 volts reference for the DAC. Notice that the output of the 101A is fed into an inverting amplifier with a gain of -3, which can be easily changed to a non-inverting configuration. (For more information write for: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)

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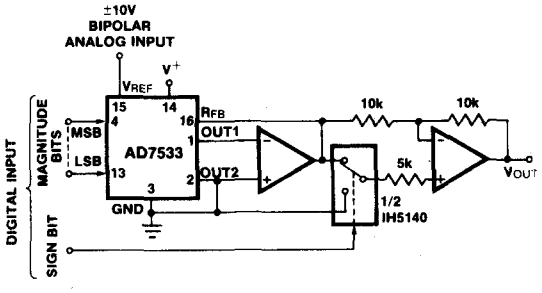
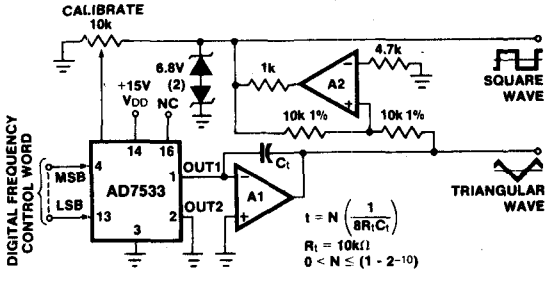
10-BIT AND SIGN MULTIPLYING DAC



PROGRAMMABLE FUNCTION GENERATOR



INPUT SIGNAL WARNING

Because of the input protection diodes on the logic inputs, it is important that no voltage greater than 4V outside the logic supply rails be applied to these inputs at any time, including power-up and other transients. To do so could cause destructive SCR latch-up.